VHDL-AMS Design of a MOST Model Including Deep Submicron and Thermal-Electronic Effects

Christophe Lallement, François Pêcheux, Yannick Hervé

ERM-PHASE/ENSPS
Pôle API, Parc d'Innovations
Bld S. Brant
67400 Ilkirch, FRANCE
{lallem,pecheux,herve}@erm1.u-strasbg.fr

Abstract

The paper presents an application of the VHDL-AMS formalism to the model of a n-MOS transistor named EKV. Our model takes into account several new features specific to deep submicron technology (parasitic resistors and overlap capacitors induced by LDD), and thermal-electronic interactions. We then give some examples of application of this innovative EKV MOS model (inverter, thermal-opto-electronic coupling).

Keywords

Thermo-electrical effect, Deep submicron effect, MOST, EKV MOST model, VHDL-AMS

1 Introduction

The design of innovative integrated devices, like MOEMS, involves strong interaction of pluri-disciplinary objects on the same chip. These objects are tightly coupled by physical effects, and the corresponding exchanges can be modeled at various abstraction levels.

Our paper is an application of the innovative VHDL-AMS concepts to state-of-the-art MOS thermal-electronic simulation models. First, we present the principles, techniques and methodology used to achieve the design of an analytical third generation Spice transistor MOS model named EKV with VHDL-AMS, with relevant parameters set [1] to match a deep submicron technology (gate length=0.15 µm). Second, we give several examples with accompanying results (a CMOS inverter, and a n-MOST laser-diode system with thermal-electronic coupling).

2 The EKV MOSFET model version 2.6

The EPFL-EKV MOSFET [2] is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

The EPFL-EKV MOSFET model is in principle formulated as a "single expression", which preserves continuity of first-order derivatives with respect to any terminal voltage, in the entire range of validity of the model. The EPFL EKV version 2.6 MOST model is a charge-based compact model. It consistently describes effects on charges, trans-capacitances, drain current and tranconductances in all regions of operation of the MOSFET transistor (weak, moderate, strong inversion) as well as conduction to saturation. It has less than twenty parameters, as depicted in Table 1.

Purpose	Parameters number
Process parameters	4
Doping & mobility related parameters	6
Short- & narrow- channel effect parameters	5
Substrate current related parameters	3

Table 1: Intrinsic parameters number for the EKV MOST Model (v. 2.6).

The effects modeled in this EKV MOSFET model v. 2.6 include all the essential effects present in deep submicron technologies.

All aspects regarding the static, the quasi-static and non-quasi static dynamic and noise models are all derived in a consistent way from a single characteristic, the normalized tranconductance-to-current ratio [2]. Symmetric normalized forward and reverse currents are used throughout all these expressions. For quasi-static dynamic operation, both a charge-based model for the node charges and transcapacitances, and a simpler capacitances model (Fig 1) are available .

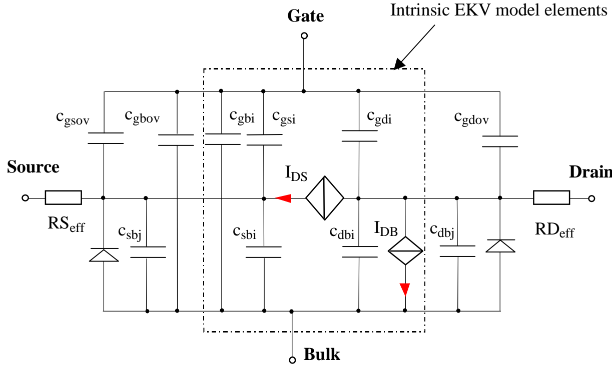

Fig. 1 : The intrinsic and extrinsic elements of the EKV transistor simpler capacitances model.

In the case of the trans-capacitances model, these trans-capacitances are obtained from the derivation of the charges at the different nodes with respect to the terminal voltage, as stated in equation (1):

$$C_{MN} = \pm \frac{\partial}{\partial V_N}(Q_M), \quad with\ M, N = G, D, S, B \qquad (1)$$

These trans-capacitances are accurate through all inversion levels.

Unlike other "SPICE" TMOS Models, the EKV MOST model has all voltages defined to the local substrate (Fig. 2).

V_D (= V_{DB}) is the electrical drain voltage, and is chosen such that $V_D > V_S$. Bulk reference allows the model to be handled symmetrically with respect to source and drain, symmetry that is inherent in common MOS technologies.

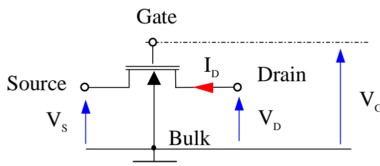

Fig. 2 : Schematic structure of the EKV n-MOST model (the bulk is the reference).

P-channel MOSFETs are dealt with as pseudo-N-channel, i.e. the polarity of the voltages (V_G, V_S, V_D, as well as the flat band voltage (optional parameters), the long-channel threshold voltage and the threshold voltage temperature coefficient) is inverted prior to computing the current for P-channel, which is given a negative sign. No others distinctions are made between N-channel and P-channel, with the exception of a factor for effective mobility calculation.

In the EKV model, the parameters strongly concerned by temperature are the long-channel threshold voltage, the mobility, the longitudinal critical field, the second impact ionization coefficient and the extrinsic sheet resistance. Their respective temperature variation are taken into account by appropriate coefficients.

3 The VHDL-AMS implementation

VHDL-AMS [3][4] is a language that supports the simultaneous description of both analog and discrete-event systems. The recent approval of VHDL-AMS as the IEEE standard for describing and simulating mixed systems is further evidence of the need for an integrated tool allowing the modeling, the simulation, or the virtual prototyping of heterogeneous systems on a chip.

For now, one of the major trends in the VHDL-AMS community is the modeling of elementary objects in the relevant physical domains involved (electronical, optical, mechanical, etc), and how these objects can simply be interconnected by the design engineer. Along with the ability to describe hierarchical/multi-abstraction models, the power of VHDL-AMS relies on the fact that it allows the model designer to only detail the constitutive equations of the inner submodels. VHDL-AMS takes advantage of a graph-based conceptual description to automatically compute the equations describing the conservative laws of the global model. The vertices of the graph represent effort nodes (`across` quantities like voltage, temperature or pressure) in the circuit, and the edges represent branches of the circuit through which information flows (`through` quantities like current, heat/liquid flow rate). Thus, the assembling of complex systems is nothing more than connecting elementary objects through terminals capable of exchanging informations, in such a way that the conservative semantics of the generalized Kirchoff laws are preserved.

Listing 1 shows the complete VHDL-AMS code for a simplified version of the EKV model, named EKV0. Following figures (e.g. ❶) reference various parts of the listing, with respect to text explanations.

For the end-user (circuit designer), the most important part is the interface ❶, known as an entity in VHDL-AMS. One can see that the n-MOST EKV0 entity only contains the traditional 4 terminals, all of electrical type. In section 4, we introduce a fifth thermal terminal which allows heat exchanges between the transistor and its environment. The architecture part ❷ contains the characteristic equations of the EKV0 model, and links

terminals to these equations. Quantities represent the static behavior of the resulting continuous system.

```
library disciplines;
use disciplines.electromagnetic_system.all;
library ieee;
use ieee.math_real.all;

entity ekv0 is ❶
 port (terminal d,g,s,b : electrical);
end;

architecture equ of ekv0 is ❷
 quantity vg across g to b; ❸
 quantity vd across id through d to s;
 quantity vs across s to b;
 quantity isource through s;

 constant vt : real := 26.0e-3;
 -- thermodynamic voltage
 constant weff : real := 10.0e-6;
 -- effective channel width
 constant leff : real := 10.0e-6;
 -- effective channel length
 constant phi : real := 0.6;
 -- Bulk Fermi potential
 constant gamma : real := 0.6;
 -- Body effect parameter
 constant kp : real := 20.0e-6;
 -- transconductance parameter
 constant theta : real := 50.0e-3;
 -- Mobility reduction coefficient
 constant vto : real := 0.6;
 -- Long channel threshold voltage

quantity VGprime,VP,iff,ir,beta,n,iss : real; ❹

 function F(v:real) return real is
 begin
  return (log(1.0+exp(v/2.0)))**2;
 end;

 begin ❺
   VGprime == vg - vto+phi+gamma*sqrt(phi) ;
   VP == VGprime - phi - gamma*
     (sqrt(VGprime+(gamma/2.0)**2)
     -(gamma/2.0));
   iff == F((VP-vs)/vt);
   ir == F((VP-vd)/vt);
   beta == kp * (weff/leff)*
      (1.0/(1.0+theta*vp));
   n==1.0+(gamma/(2.0*sqrt(VP+phi+4.0*vt)));
   iss == 2.0*n*beta*vt*vt ;
   id == iss*(iff-ir) ;
   isource == -id ;
end ;
```

Listing 1 : The complete VHDL-AMS code for the simplified EKV model (case of a large transistor) .

The former quantities ❸ are bound to terminals (terminals represent the nodes across of through which these quantities are defined), while the latter are free ❹. VHDL-AMS is of great interest as it allows the transistor model designer to enter « as is » the physical equations ❺ of the model as a set of simultaneous statements. The solvability of the model relies on the fact that the total number of constitutive equations matches the total number of free, through and interface quantities.

4 Features specific to submicron

The LDD regions in the sub- and deep sub-micron CMOS technologies introduce additional parasitic resistances between the source/drain electrode and the channel, as well as overlap capacitances; these capacitances become more and more important in regard of the global capacitance (Fig. 3) of the MOST (about 30% for a 0.2µm technology).

A problem with all these parasitic elements is their non-linear and bias dependent behavior.

So, a MOST model dedicated to deep-submicron design must imperatively take into account these elements. Figure 3, and equation (2) show some simple and accurate solutions to the modeling of the LDD region, and this with few parameters (Table 2).

Series parasitic resistance

$$RS/RD = RSH.\left[1-0.5.\left(r+\sqrt{r^2+0.01}\right)\right] \qquad (2.a)$$

$$with \quad r = SVK.\left[(VG-VTO)/VK-1\right] \qquad (2.b)$$

Overlap capacitance

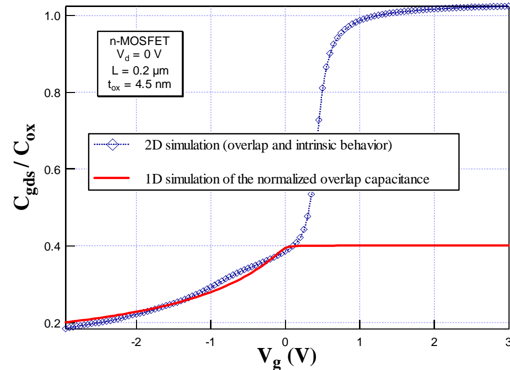

Figure 3 : Simulation and evaluation of the overlap capacitance in a 0.2 µm technology [5].

Purpose	Name	Description
Overlap capacitance	LAMB	Overlap coefficient
	TPOLY	Polysilicon thickness
Series parasitic resistances	RSH0	Sheet resistance at zero bias
	VK	Characteristic voltage
	SVK	LDD coefficient

Table 2 : Parameters for deep submicron technologies.

5 Thermal-electronic modeling

As the transistor size decreases, thermal interactions between devices on the same chip increase. These thermal effects are constantly amplified with the growing power density, and a failure in their estimation at an early development stage of the design often means extra costs and delays.

When simulating circuits, heat diffusion through solid materials can be modeled by different means [6]-[9]. In the model, we do this by sourcing dissipated power into a thermal RC network [6], which represents the material properties of the different layers (thermal resistances and capacitances of ambient, heat sink and package). The temperature profile is the result of heat flow in the thermal network. In such networks, energy conservation states that the sum of all power contributions at a thermal node equals zero, and that the temperature at all terminals connected to a thermal node be identical. Thermal evolution of a system is thus ruled by the very same Kirchoff laws dictating the behavior of conservative systems : voltage becomes the across quantity temperature, and current becomes the through quantity heat flow.

VHDL-AMS provides an elegant solution to thermal-electronic interactions. Among the various packages provided with the simulation environment, the `thermal_system` package simply adds thermal capabilities to electrical models. The principle is to introduce a thermal terminal, with relative `through` and `across` quantities respectively bound to power and temperature.

The final EKV interface then becomes :

```
entity ekv1 is
   port (terminal d,g,s,b : electrical ;
   terminal j : thermal);
end;
```

with the following `quantity` relations :

```
quantity temp across power through j to
thermal_ground ;
```

that define state variable `temp` as an extensive value, and `power` as the corresponding intensive value.

Using this electrical-thermal analogy, a thermal generator can simply be designed to model the ambient with equation (3),

```
constant amb_temp: real := 300.0 ;
...
temp == amb_temp ; (3)
```

while thermal resistance and capacitance can respectively be described by equations (4) and (5).

```
temp == rth * power ;  (4)
power == cth * temp'dot ; (5)
```

Once again, VHDL-AMS makes easier the description of dynamic behavior of components with implicit quantities like `'dot`.

Figure 4 shows how thermal-electronic interactions between n-MOST and its direct environment can be modeled.

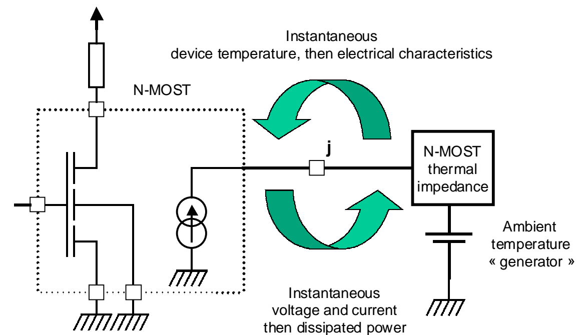

Fig. 4 : Modeling electro-thermal interactions.

Figure 4 puts emphasis on the fact that the instantaneous power dissipated by the EKV model is directly propagated to the thermal node j. The transistor thus acts as a power source in the thermal network. Reciprocally, the instantaneous temperature computed by the RC network and back-propagated to the thermal node of the n-MOST model is the operating temperature of the n-MOST model. This allows the n-MOST model to adjust its characteristic equations as a function of its operating temperature.

6 Experimental results

The thermo-electrical effect applied to the n-MOST and surrounding substrate is a long process, as thermal time constants are several order of magnitude greater than electrical ones. In the following simulations, we have deliberately overstated values of the thermal network, in order to emphasize the downgrading of electrical characteristics.

Figure 5 shows the C_{GG} trans-capacitance characteristic (without thermal effect) of the MOSFET transistor. Figure 6 and 7 show the output characteristic of the MOST with the same electrical bias. The I_d vs. V_d characteristic in Figure 7 is downgraded with temperature variation in the chip (also plotted on the figure) compared to Figure 6.

Figure 8 details the simulation of the chip temperature variation and of the drain voltage versus time during commutation, of the n-channel transistor (in an inverter).

Figures 9 and 10 show the simulations of the laser diode temperature, of the laser diode current and of the light power, during commutation. The laser diode model can be found in [10]. We can observe the electrical and light power downgradings while the laser diode temperature increases.

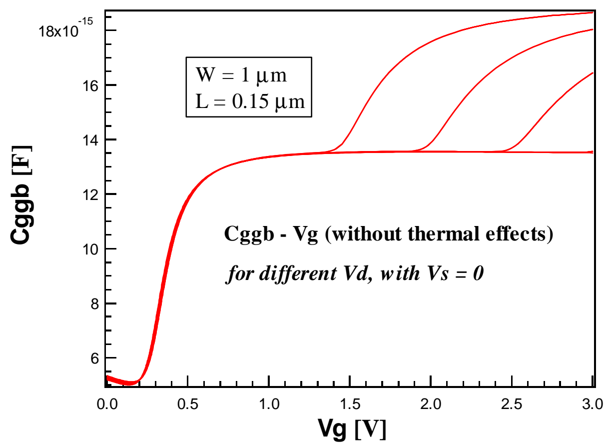

Fig.5 : Simulation in VHDL-AMS of the C_{ggb} transcapacitance.

Figure 11 presents a complete design that validates the methodology. The system details thermal coupling between an n-MOST and a laser-diode. Each component is excited by a squarewave stimulus (the laser-diode stimulus period is twice the n-MOST period), and connected to a local thermal RC network. The two thermal networks represent the thermal constants of the various material layers, and the effective coupling is realized thanks to `Rcoupling`.

Figure 12 shows two cycles of temperature evolution in the global system. At time 0, with no stimulus, temperature is given by the ambient temperature generator and propagated to both devices (300° K). At time 0.5s, the n-MOST is stimulated and its temperature reaches 315° K, while the laser-diode slightly reacts to this change (310° K). At time 1s, the laser-diode is activated, its temperature rapidly rises to 335° K, and n-MOST temperature jumps to 326° K. At time 1.5s, both devices are stimulated, and temperature effects are stacked up.

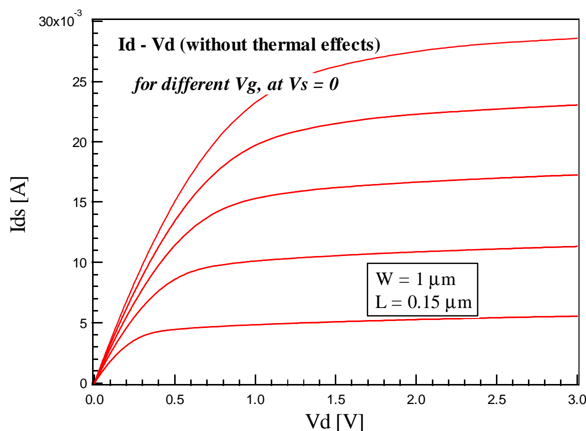

Fig. 6 : Simulation in VHDL-AMS of the Id versus Vd characteristic (without thermal effects).

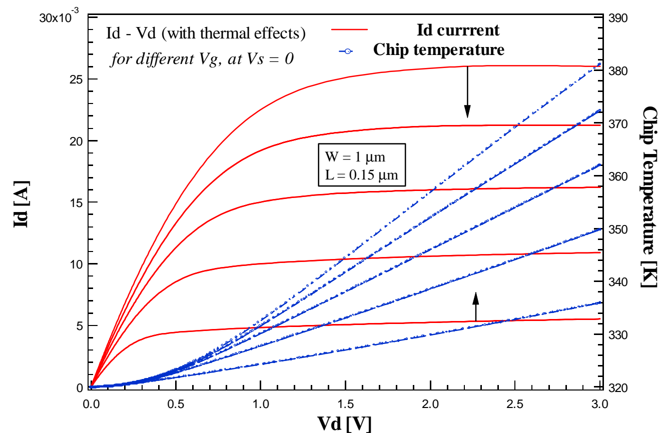

Fig. 7 : Simulation in VHDL-AMS of the I_d / chip temperature vs. V_d characteristics (with thermal effects).

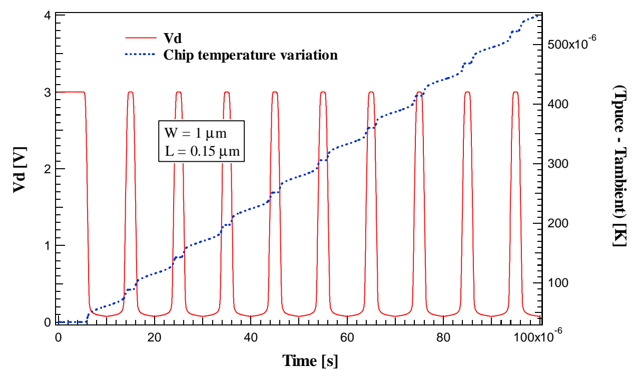

Fig. 8 : Simulation in VHDL-AMS of the n-channel transistor chip temperature variation versus time during commutation (in an inverter).

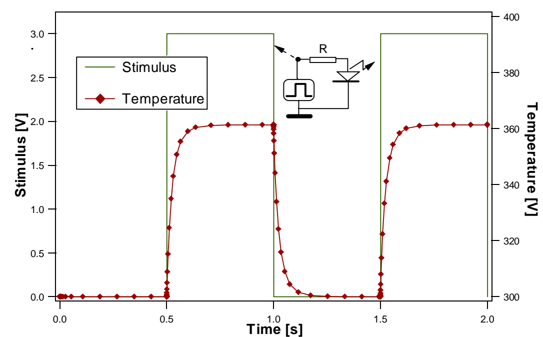

Fig. 9 : Simulation of the laser diode temperature during commutation.

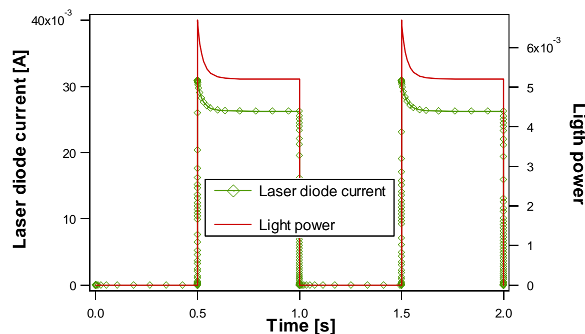

Fig. 10 : Simulation of the laser diode current and light power during commutation.

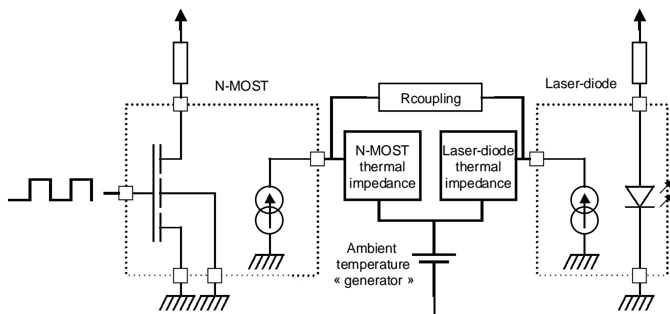

Fig. 11 : Simulation Circuit.

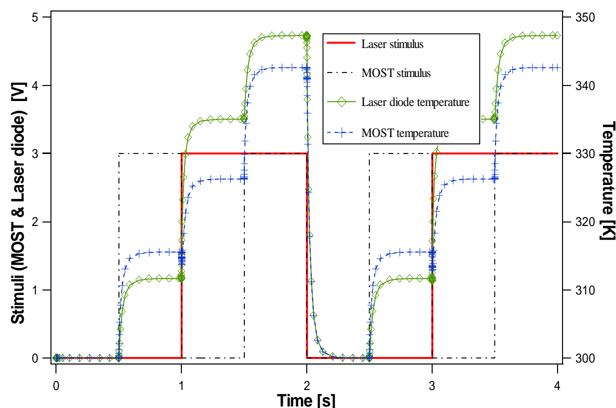

Fig. 12 : Simulation results for circuit of Fig. 11.

7 Conclusions

The EKV VHDL-AMS is about 950 lines of source code. For the moment, its limitations are due to the language itself (ie PDE are not supported, and accurate thermal model for heat diffusion is therefore not available), and to its operating environment (Anacad Advance AMS 1.1-1.1). As soon as the latter supports `procedural` statements, we'll be able to produce much more convenient nMOS models. Nevertheless, it is now possible to imagine the future of MOEMS design as the incremental interconnexion of composite pluri-disciplinary objects. We are currently working on the VHDL-AMS release v.3 of the EKV model. It will notably include the quantum and polydepletion effects, and the NQS behavior [11].

References

[1] R. J. Baker: CMOS: Mixed-signal Circuit Design, Chap. 33. (http://cmosedu.com/cmos2/chap33.pdf). The book will be published this Fall 2001.

[2] M. Bucher, C. Lallement, C. Enz, F. Théodoloz, K. Krummenacher, "The EPFL-EKV MOSFET Model Equations for simulation, Version 2.6", Technical Report, EPFL , 1997, http://legwww.epfl.ch/ekv/.

[3] E. Christen, K. Bakalar, "VHDL-AMS-a hardware description language for analog and mixed-signal applications," *IEEE Trans. on Circuits and Systems, part II*, Vol. 46 Issue: 10, pp. 1263 –1272, Oct. 1999.

[4] 1076.1-1999 IEEE Standard VHDL Analog and Mixed-SignalExtensions [ISBN 0-7381-1640-8], http://www.vhdl.org/analog/

[5] F. Pregaldiny, C. Lallement, D. Mathiot, *Paper Submitted to SSE*

[6] C. Lallement, R. Bouchakour and T. Maurel, "One-dimensional Analytical Modeling of the VDMOS Transistor Taking Into Account the Thermoelectrical Interactions," *IEEE Transactions on Circuits and Systems, Part. I*, Vol. 44, N° 2, pp. 103-111, Feb. 1997.

[7] C. Lallement, R. Bouchakour and T. Maurel, "One-dimensional Analytical Modeling of Power Mosfet and Bipolar Transistors Taking Into Account the Thermoelectrical Interactions," *Modeling in Analog design, Vol. 2*, in series on Current Issues in Electronic Modeling, , Ch. 5, pps 121-143, Eds: Jean-Michel BERGE et al., Kluwer Academic Publishers, 1995.

[8] H.A. Mantooth, E. Christen, "Modeling and simulation of electrical and thermal interaction," *Modeling in Analog design, Vol. 2*, in series on Current Issues in Electronic Modeling, , Ch. 5, pps 93-120, Eds: Jean-Michel BERGE, et al., Kluwer Academic Publishers, 1995.

[9] T. Maurel, R. Bouchakour and C. Lallement," A New Approach for the Electrothermal Modeling of the Power Bipolar Transistor", *PESC '95 Record.*, 26th Annual IEEE, Vol.: 2 , pp. 858 –864, 1995.

[10] W. Uhring, Y. Hervé, F. Pêcheux," Model of an instrumented optoelectronic transmission system in HDL-A and VHDL-AMS ", *SPIE 99*,Australia, 1999.

[11] J. M. Sallese, et al, "Advancements in DC and RF Mosfet modeling with the EPFL-EKV charge based model," *8th Int. Conf. MIXDES*, Poland, pp. 45-52, 21-23 June 2001.