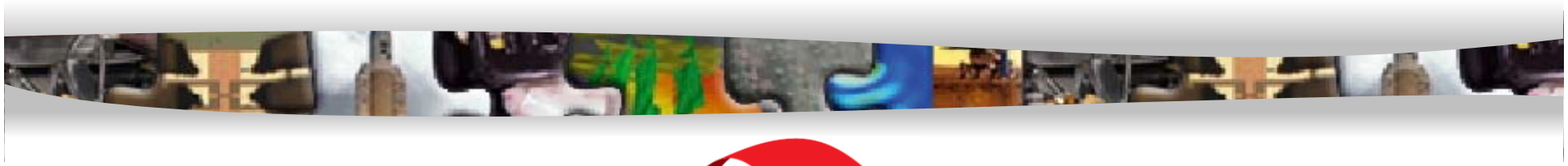


nano-tera.ch

MOSFET Modeling for Ultra Low-Power RF Design

T. Taris, H. Kraïmia, JB. Begueret, Y. Deval

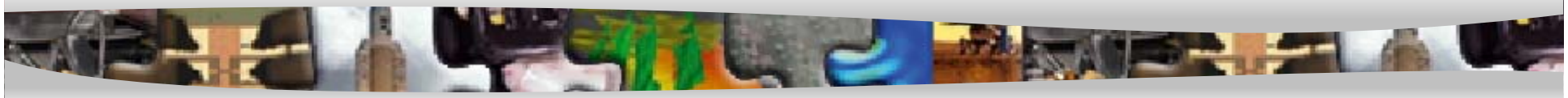
Bordeaux, France

ims

UNIVERSITÉ DE BORDEAUX

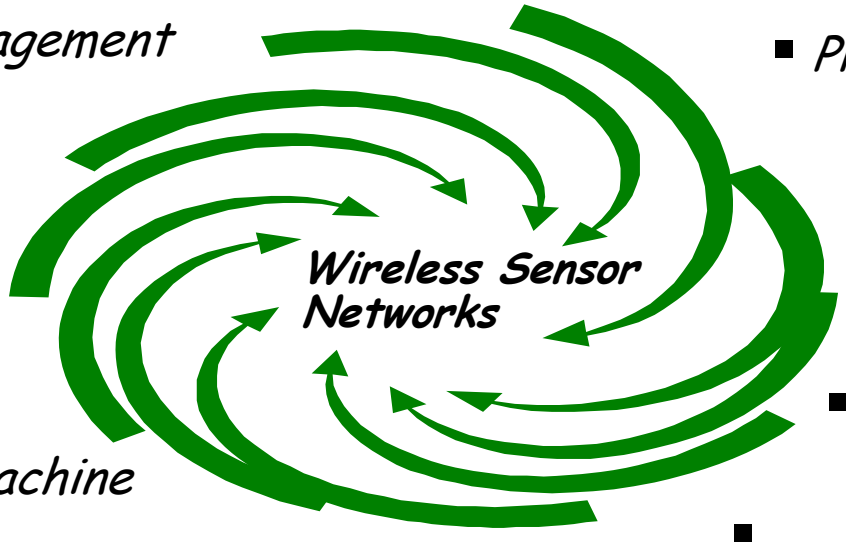
12/15-16, 2011 **– Lauzanne, Switzerland**

Context

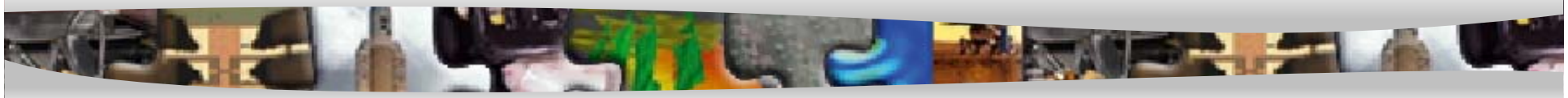


More services in…

- *Environment survey*
- *Energy management*
- *Process optimisation*
- *Aging follow up*
- *Localisation service*
- *Health monitoring*
- *Human to machine interaction*
- *…*
- *Item tracking*



Context



More services in…

Challenges

- *Environment survey*
- *Energy management*
- *Process optimisation*
- *Aging follow up*
- *Localisation service*
- *Health monitoring*
- *Human to machine interaction*
- *…*
- *Item tracking*

Wireless Sensor Networks

➢ **Low cost**

Price/node <1$

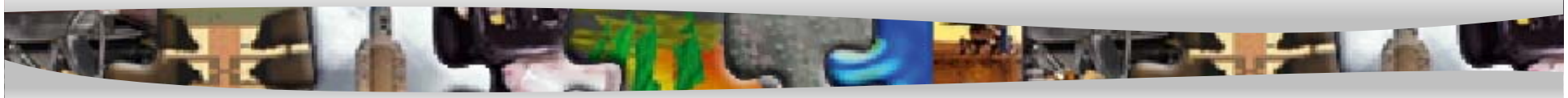
➢ **Small form factor**

1 cm³

➢ **Low power**

Run 10 years!

Context



More services in…

Challenges

- Environment survey
- Energy management
- Process optimisation
- Aging follow up
- Localisation service
- Health monitoring
- Human to machine interaction
- …
- Item tracking

Wireless Sensor Networks

➢ **Low cost**

Price/node <1$

➢ **Small form factor**

1 cm³

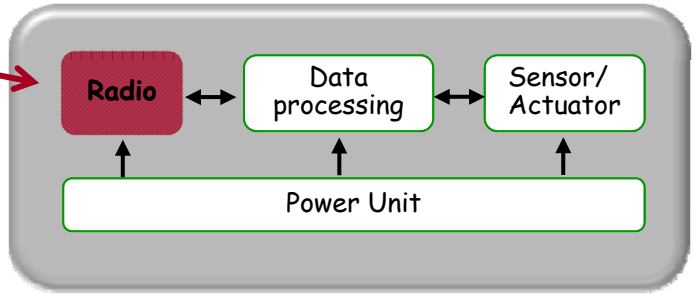
➢ **Low power**

Run 10 years!

Large Power Consumption

- **Radio module**
  - ⇒ *Data broadcasting*
  - ⇒ *Communications*

- ***Data processing***
  - ⇒ *Computation*
  - ⇒ *Memory writing/reading…*



- ***Sensor/Actuator***
  - ⇒ *Environment Interface*

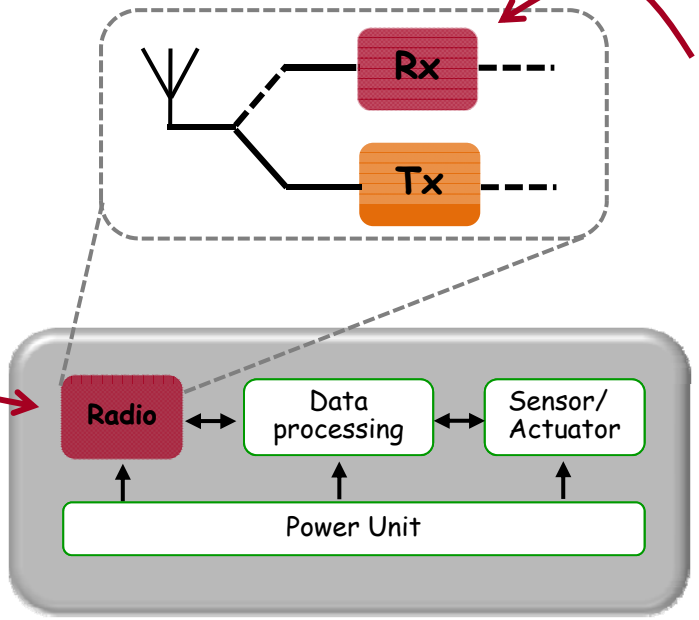
- ***Power Unit***
  - ⇒ *Supply*
  - ⇒ *Energy Management/Storage*

WSN Node Basics

Low Duty Cycle

WSN node in Rx mode most of the time

Large Power Consumption

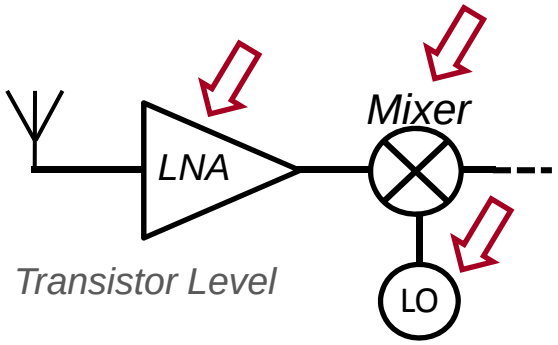


- **Radio module**
  - ⇒ *Data broadcasting*
  - ⇒ *Communications*
- ***Sensor/Actuator***
  - ⇒ *Environment Interface*
- ***Power Unit***
  - ⇒ *Supply*
  - ⇒ *Energy Management/Storage*

Context

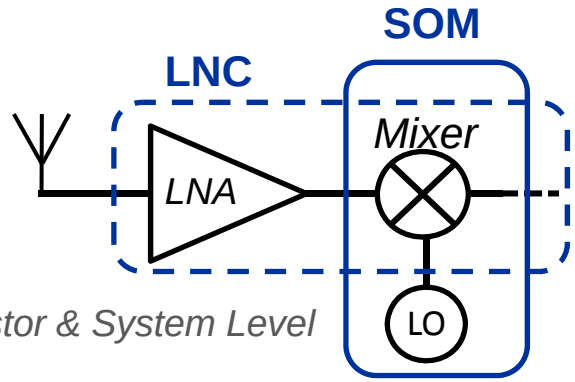
Radio Circuit/System Considerations

Various approaches to improve the power saving in Radio



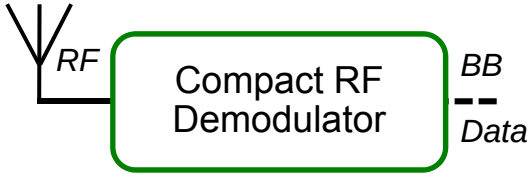
Transistor Level

Standalone Building Blocks



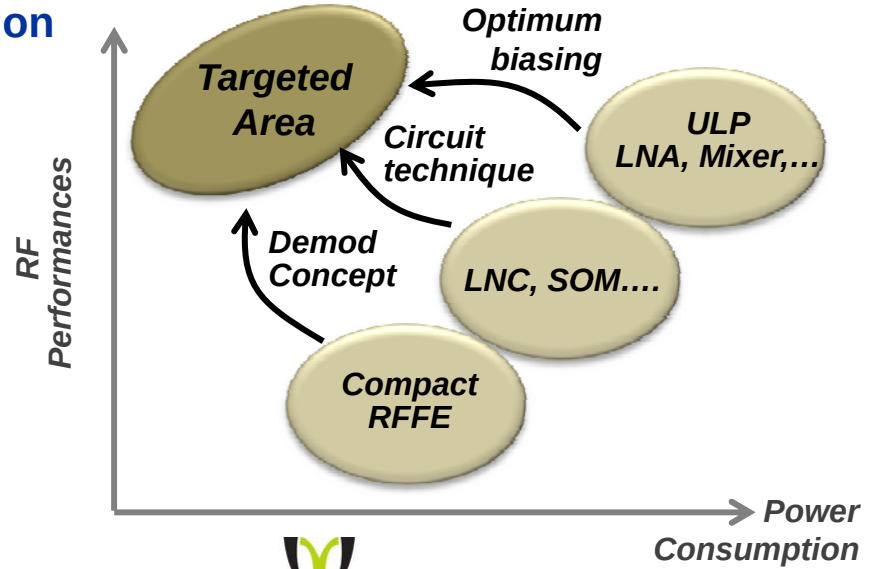
Transistor & System Level

Building Block Combination



Compact RFFE Demodulators

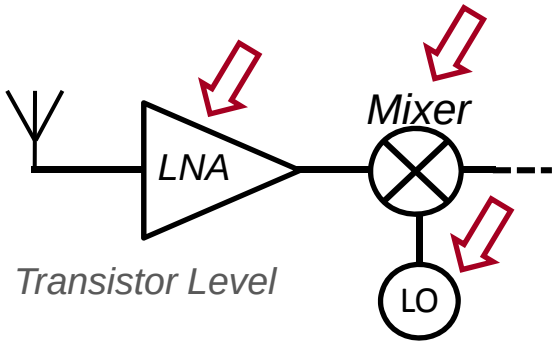
System Level



Context

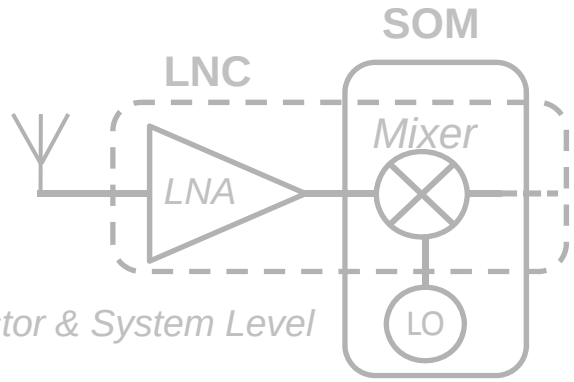
Radio Circuit/System Considerations

Various approaches to improve the power saving in Radio



Transistor Level

Standalone Building Blocks

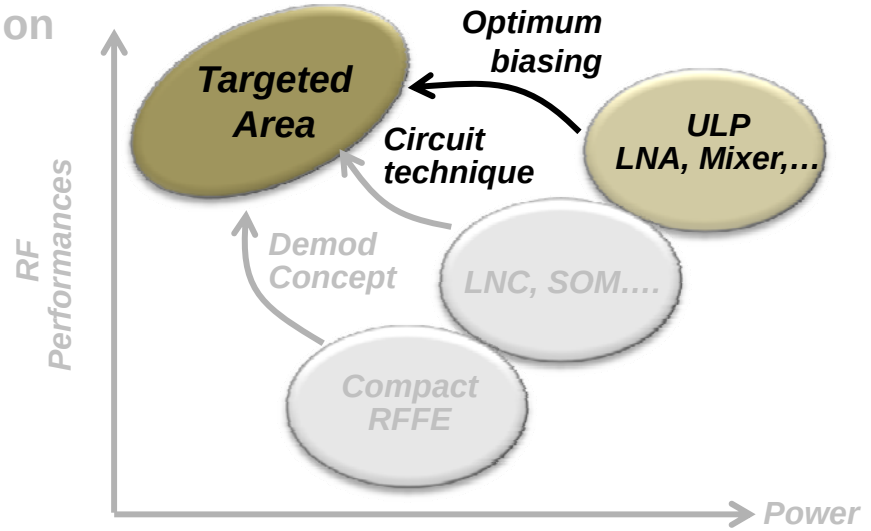


Transistor & System Level

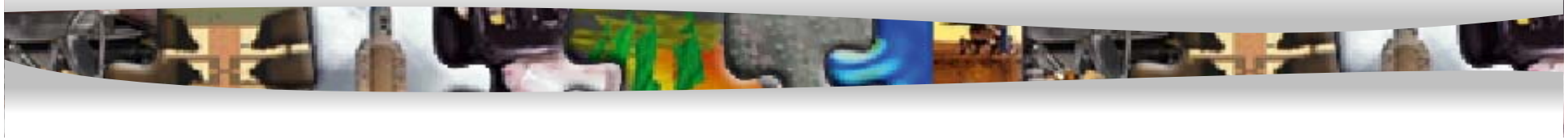
Building Block Combination

System Level

Compact RFFE Demodulators

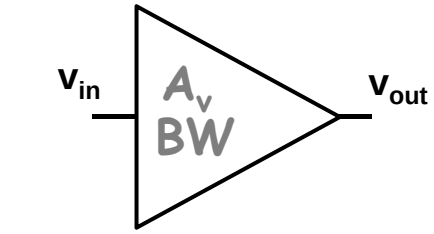


OUTLINE



- Context
- **From analog to RF Metric**
- **Low Noise Amplifier Implementation**
- **Conclusions & Perspectives**

Voltage Amplifier



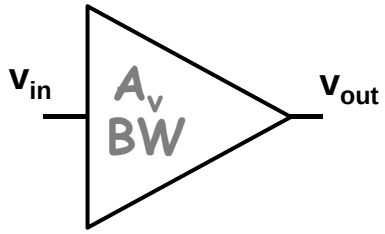
$$GBW = A_v.BW$$

➢ Figure Of Merit for Low Power amplifier

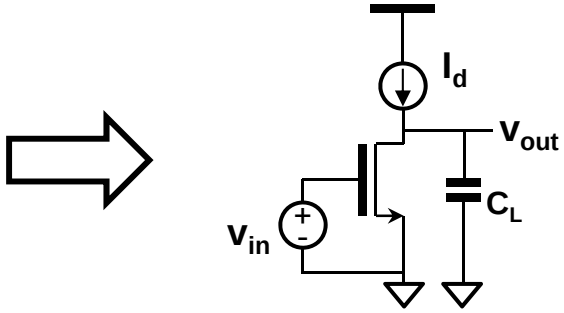
$$FOM_{LPamplifier} = \frac{GBW}{I_D}$$

From analog to RF Metric

Voltage Amplifier



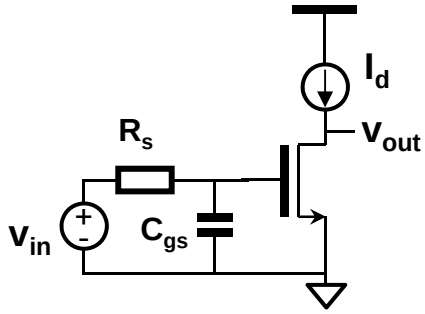
$$GBW = A_v.BW$$



$$GBW = \frac{g_m}{2\pi.C_L}$$

Configurations

or



$$GBW = \frac{g_m}{2\pi.C_{gs}}.\frac{r_{ds}}{R_S}$$

➢ Figure Of Merit for Low Power amplifier

$$FOM_{LPamplifier} = \frac{GBW}{I_D} \propto \frac{g_m}{C.I_D} \Rightarrow \frac{g_m}{I_D}$$

From analog to RF Metric

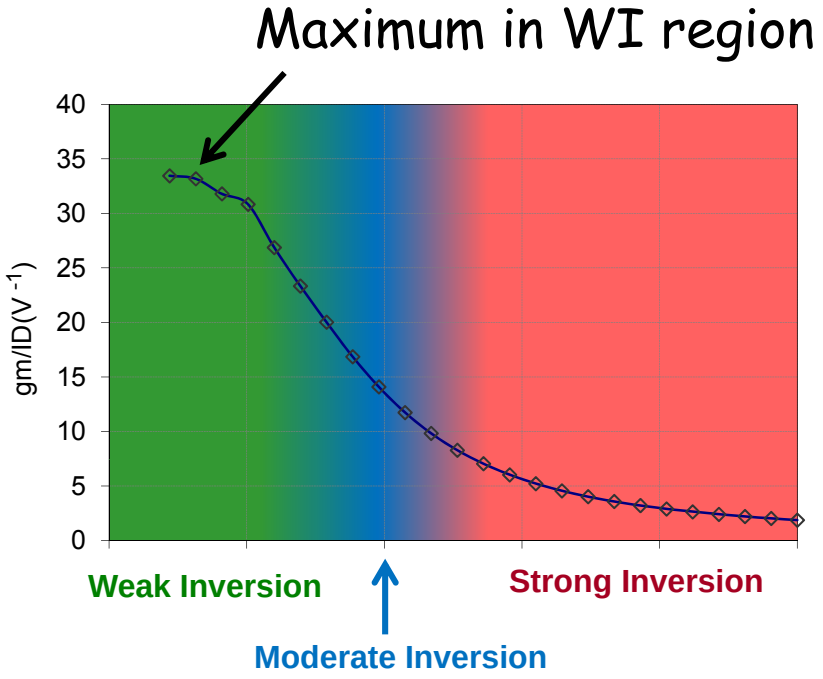
Low Power Analog Metric

❑ Figure Of Merit for Low Power Analog

Transductor gain of the device

$$FOM_{LP_{analog}} = \frac{g_m}{I_D}$$

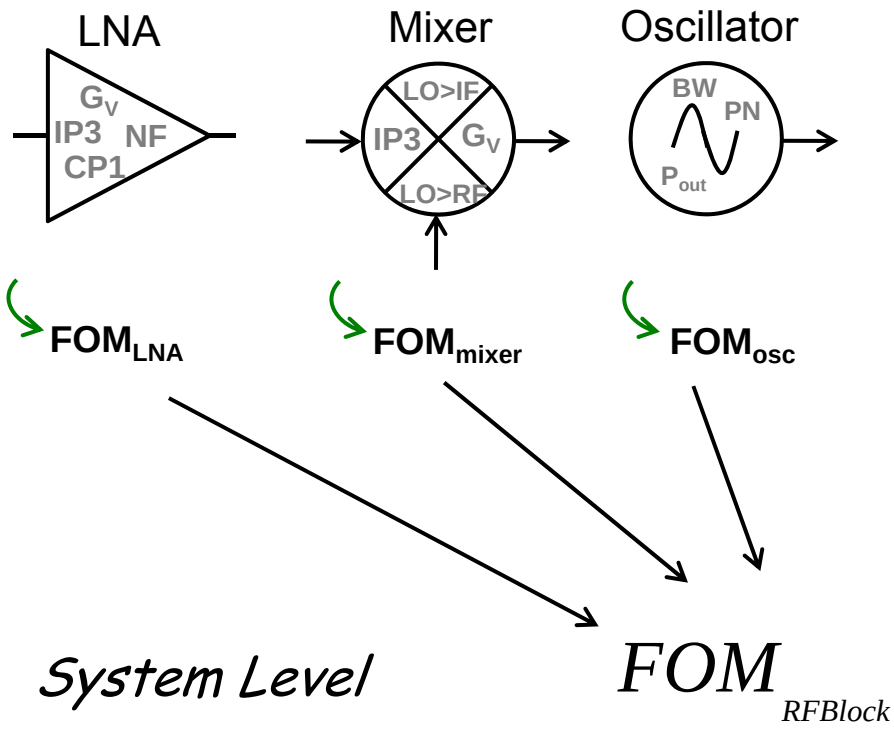
Current consumption



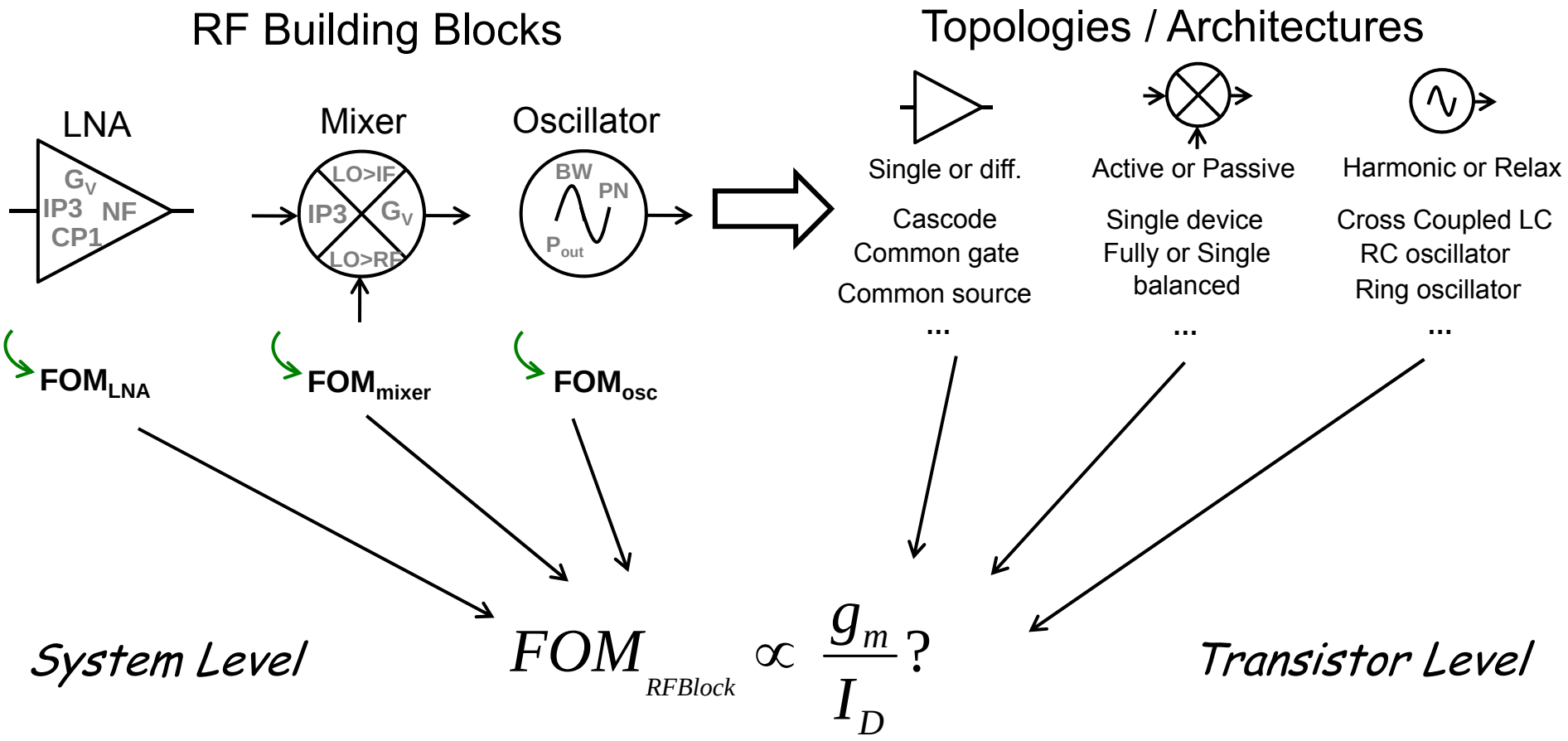
➡ ***$FOM_{LPanalog}$ is maximum in WI region***

From analog to RF Metric

RF Building Blocks

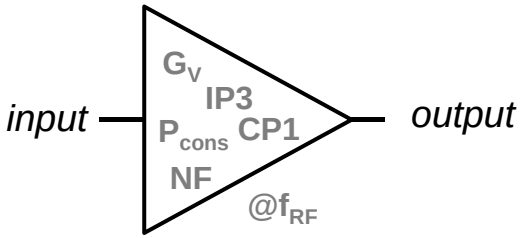


From analog to RF Metric



From analog to RF Metric

Low Noise Amplifier



- Most important characteristics
  - A large voltage gain **G_v** at **f_{RF}**
  - A low noise figure **NF** at **f_{RF}**

Topologies / Architectures

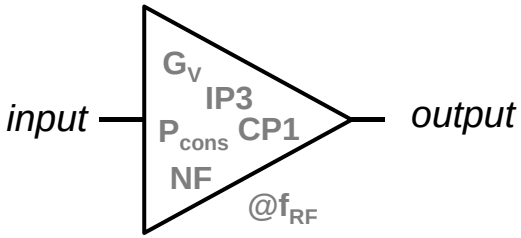
➢ Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_V \cdot f_{RF}}{(F-1).P_{cons}}$$

System Level *Transistor Level*

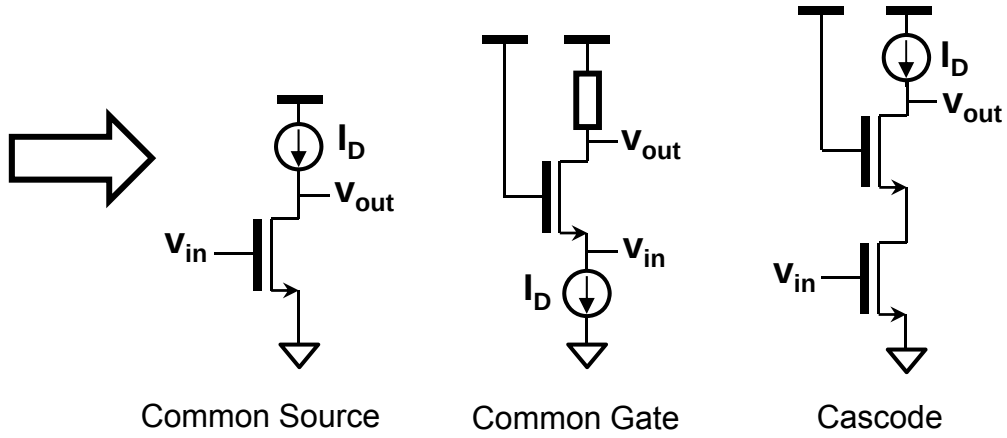
From analog to RF Metric

Low Noise Amplifier



- Most important characteristics
  - A large voltage gain **G_v** at **f_{RF}**
  - A low noise figure **NF** at **f_{RF}**

Topologies / Architectures



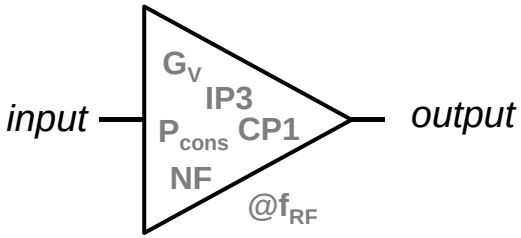
➢ Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_V \cdot f_{RF}}{(F-1).P_{cons}}$$

System Level *Transistor Level*

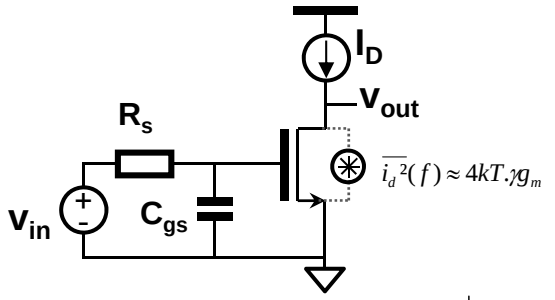
From analog to RF Metric

Low Noise Amplifier



- Most important characteristics
  - A large voltage gain **G_v** at **f_{RF}**
  - A low noise figure **NF** at **f_{RF}**

Common Source Analysis



$$|G_V|_{MOS} \propto \frac{g_m}{|1+jC_{gs}R_s\omega|} \propto \left.\frac{g_m}{C_{gs}R_s\omega}\right|_{@\omega_{RF}}$$

with $f_T = \frac{g_m}{2\pi.C_{gs}}$

$$P_{cons} \propto I_D$$

$$F_{\min}|_{MOS} \propto 1+\frac{1}{g_m.R_s}$$

➢ Figure Of Merit for Low Power LNA

$$FOM_{LPLNA} = \frac{G_V.f_{RF}}{(F-1).P_{cons}}$$

$$FOM_{LPLNA}|_{MOS} \propto \frac{g_m.f_T}{I_D}$$

System Level

Transistor Level

From analog to RF Metric

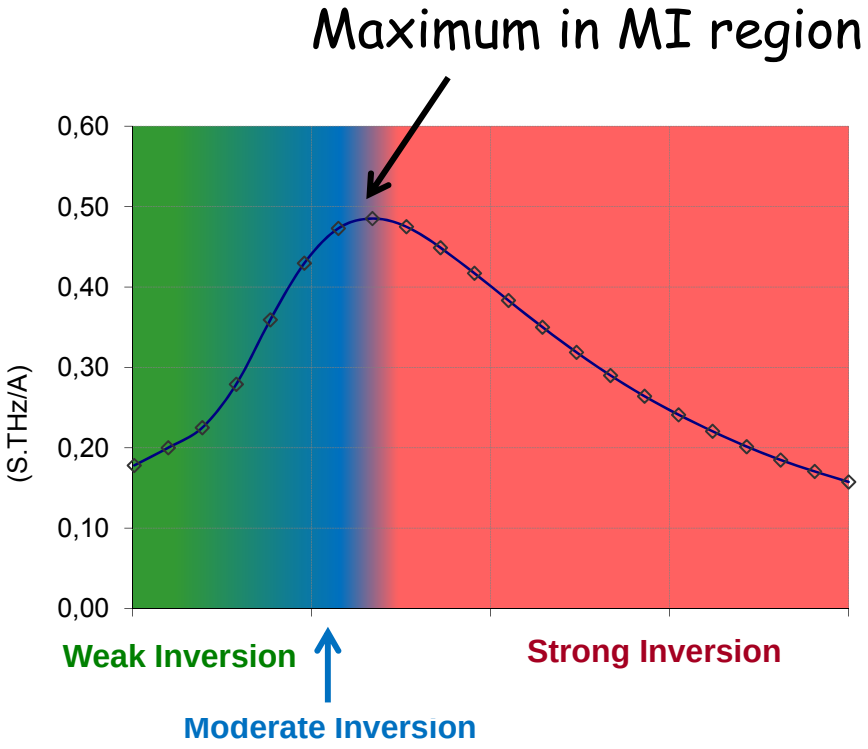
❑ Figure Of Merit for low power LNA

Transductor gain of the device

Cutoff frequency of the device

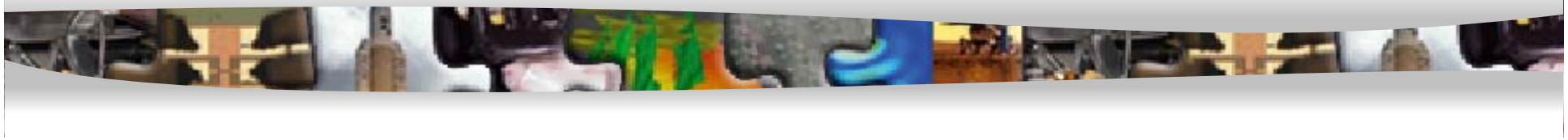
$$FOM_{LP_{LNA}} = \frac{g_m \cdot f_T}{I_D}$$

Current consumption



➡ ***FOM_{LPLNA} is maximum in MI region***

OUTLINE



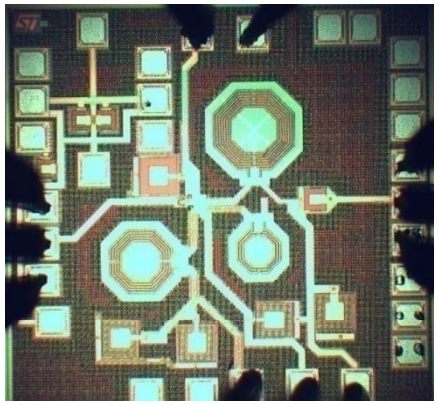
- Context
- From analog to RF Metric
- **Low Noise Amplifier Implementation**
- **Conclusions & Perspectives**

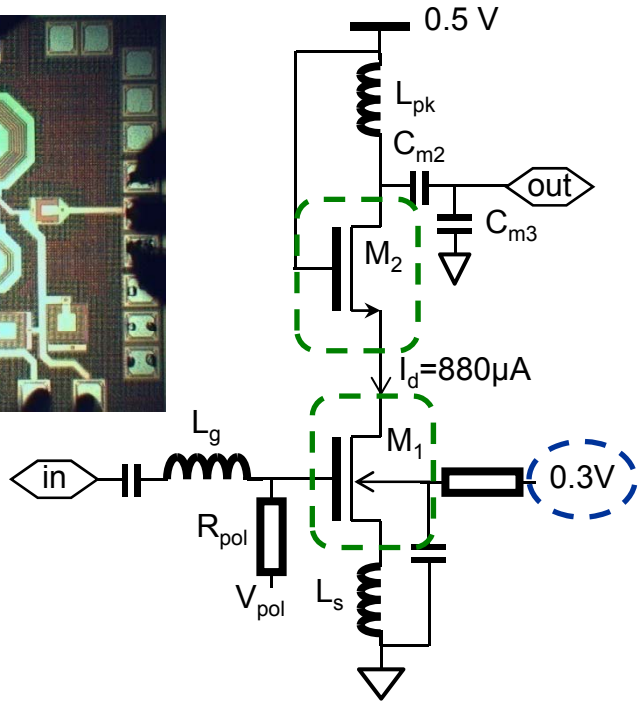
Ultra Low Power LNA

Forward Body Biased Cascode LNA

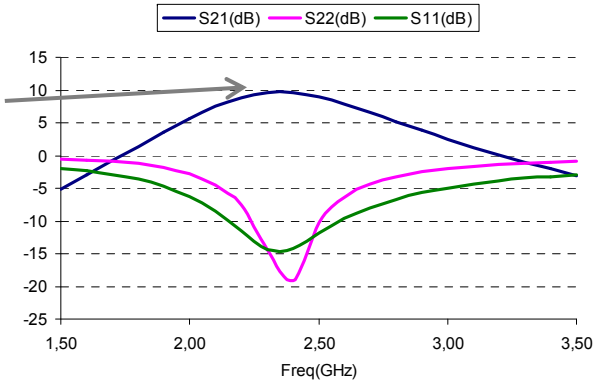
2.4 GHz LNA - CMOS 0.13µm

440µW@0.5V

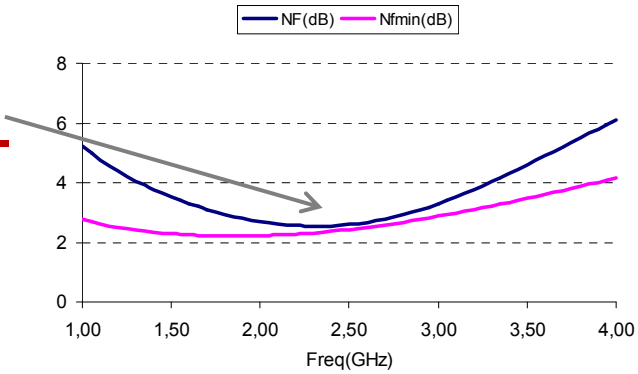




10dB gain



3.4dB NF



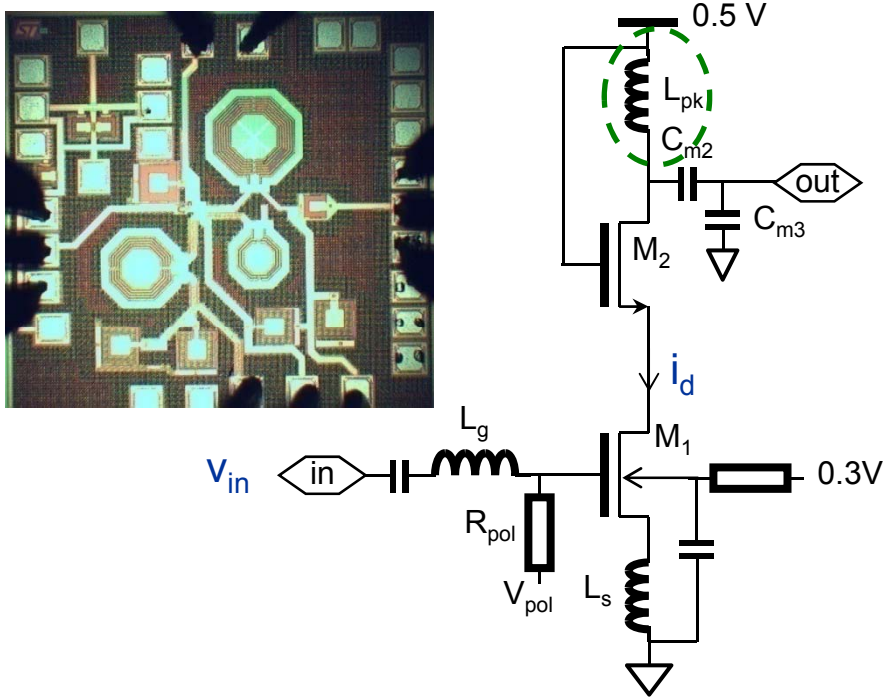
→ **MOS device in MI region to maximise FOM_{LPLNA}**

→ **Bulk forward biasing to reduce V_{th}**

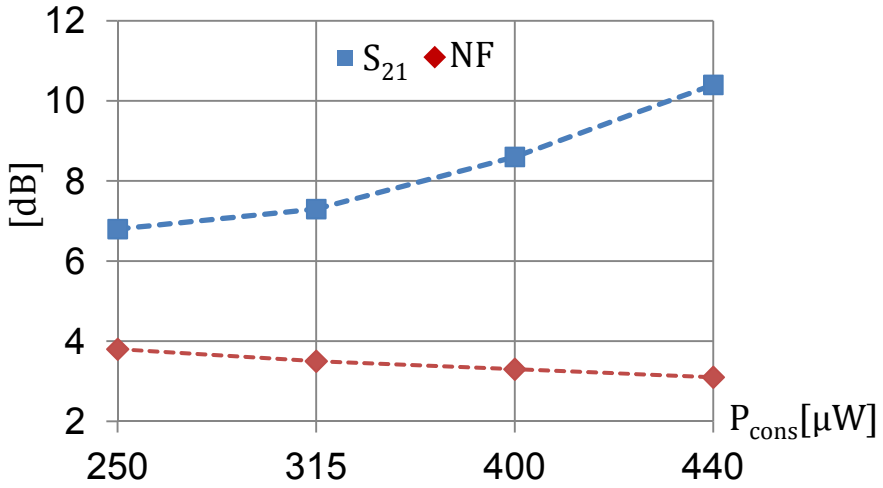
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm



Gain & NF vs Power Consumption



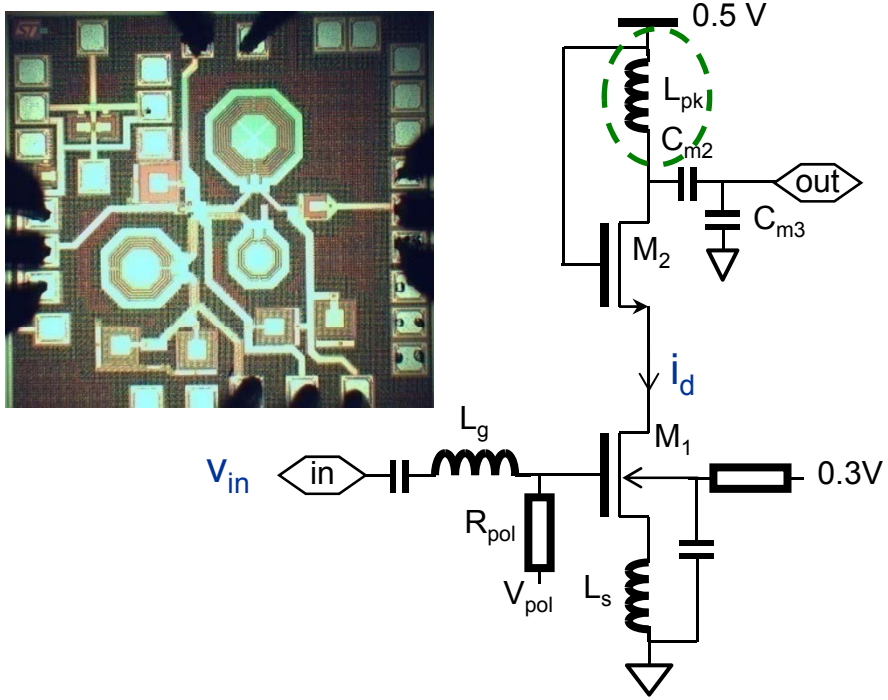
→ Limited value on Si

Peaking Load

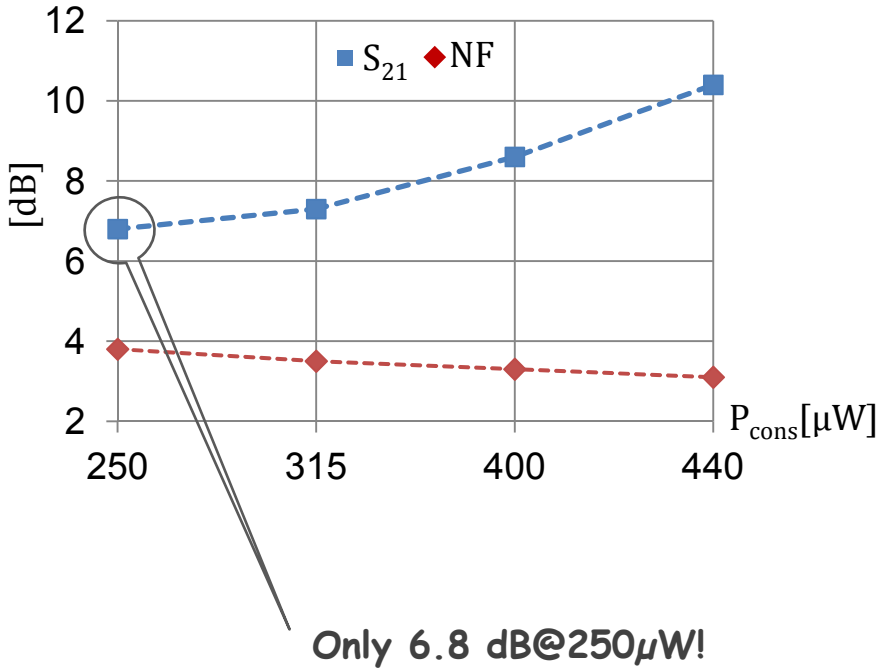
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm



Gain & NF vs Power Consumption



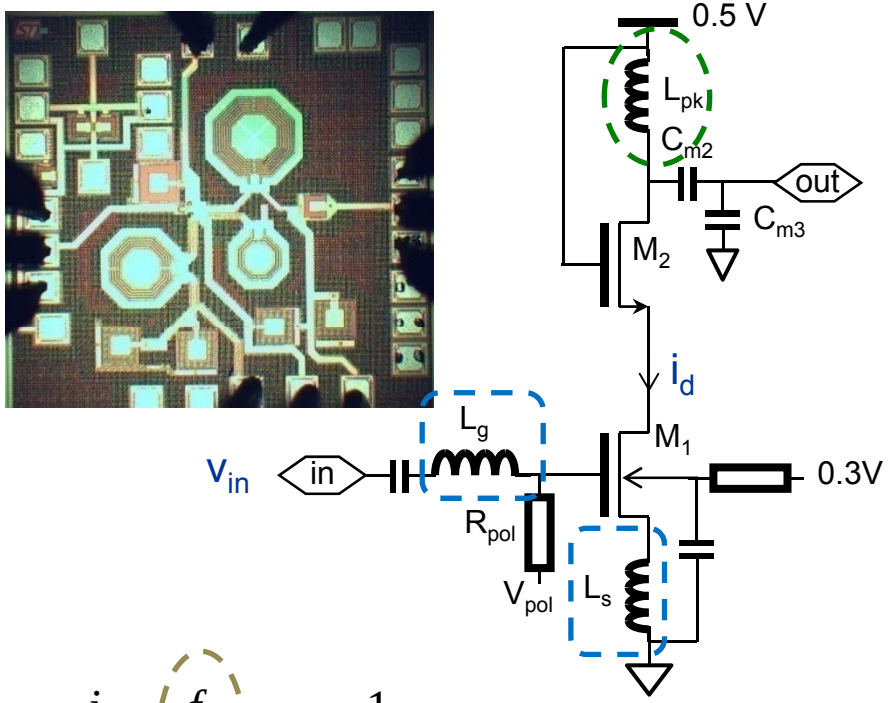
→ Limited value on Si

Peaking Load

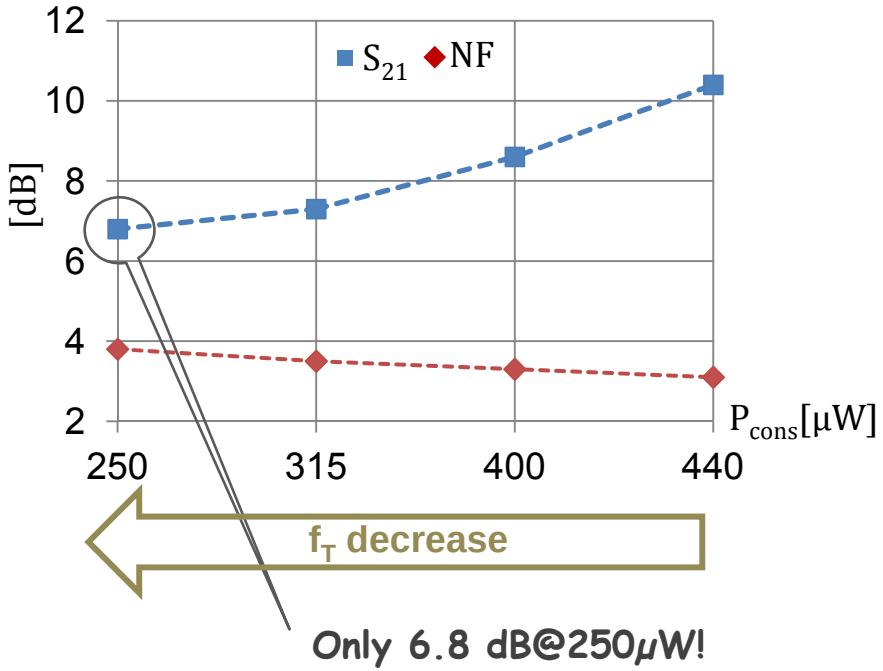
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm



Gain & NF vs Power Consumption



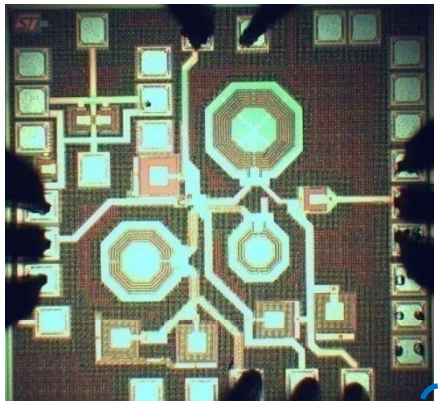
→ $\frac{i_d}{v_{in}} = \frac{f_T}{f}\frac{1}{R_s\sqrt{1+(2\pi f R_s)^2}}$ Inductive Degeneration

→ Limited value on Si Peaking Load

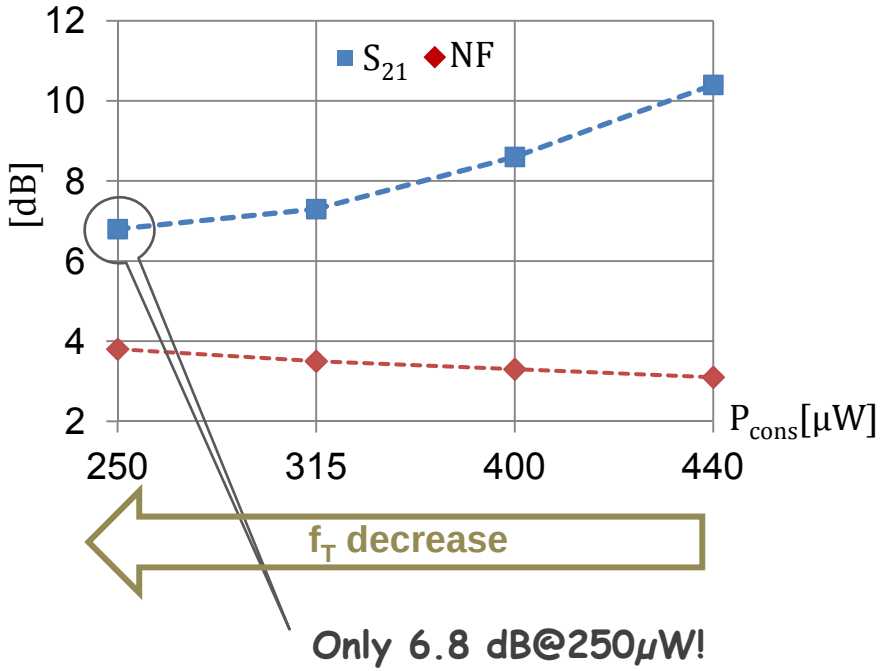
Ultra Low Power LNA

Forward Body Biased Cascode LNA

2.4 GHz LNA - CMOS 0.13µm



Gain & NF vs Power Consumption



→ $\frac{i_d}{v_{in}} = \frac{f_T}{f}\frac{1}{R_s\sqrt{1+(2\pi f R_s)^2}}$ Inductive Degeneration

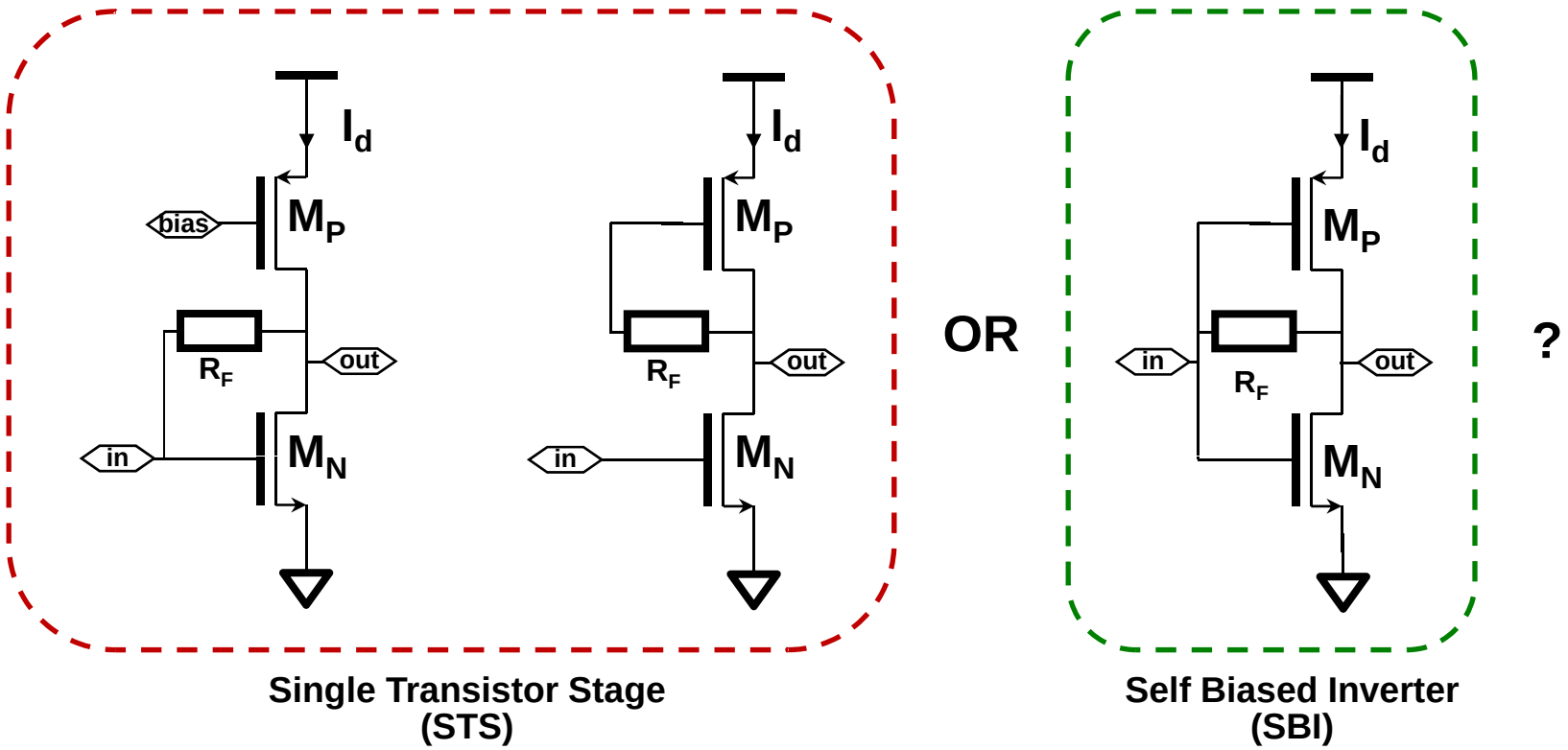
→ Limited value on Si Peaking Load

⇨ ***Strong Inversion Techniques***

Ultra Low Power LNA

Select the best suited topology

- To compensate for the low g_m in MI region…



Single Transistor Stage (STS)

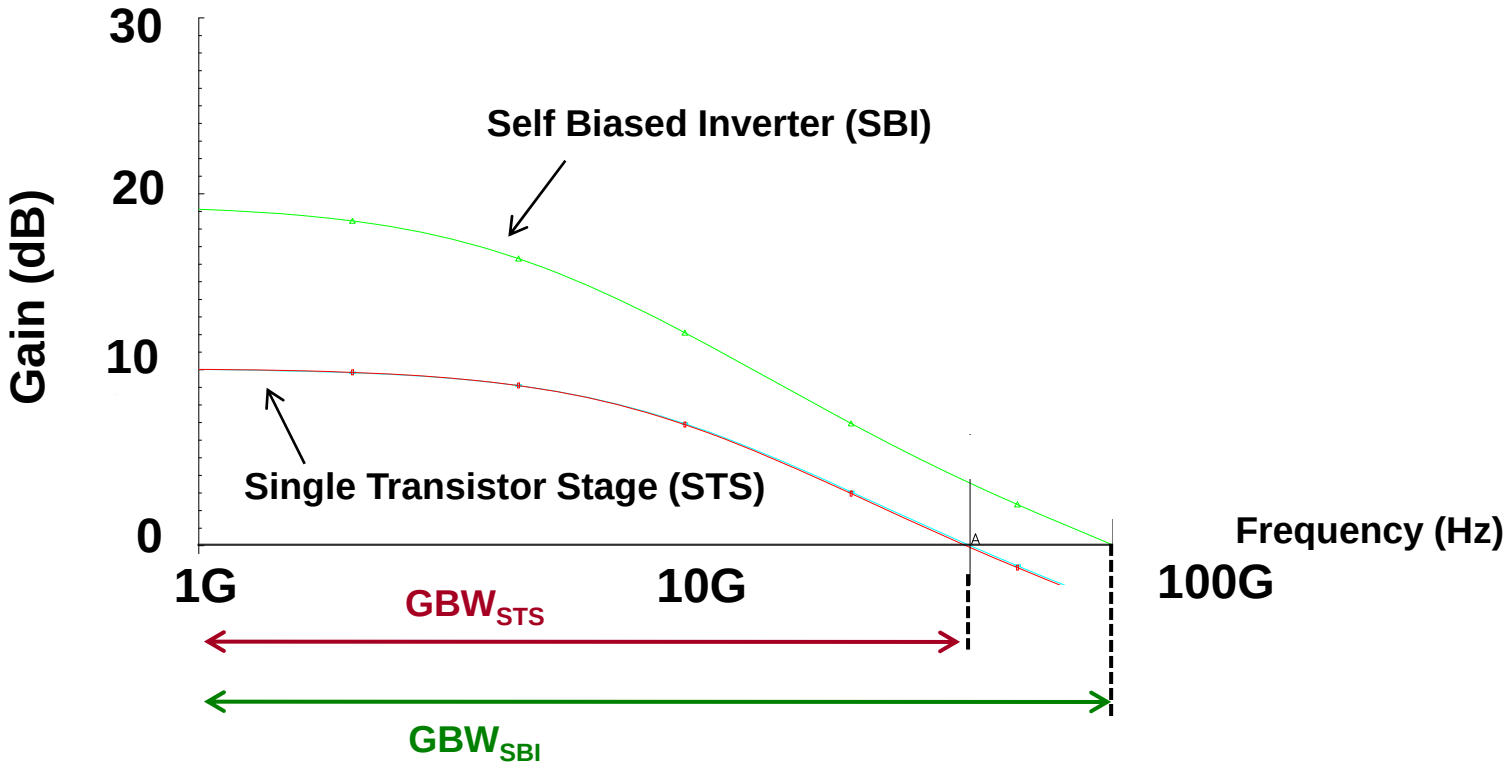
Self Biased Inverter (SBI)

…active load configurations are preferred!

Ultra Low Power LNA

Select the best suited topology

- Comparison of the Gain BandWidth (GBW) product…

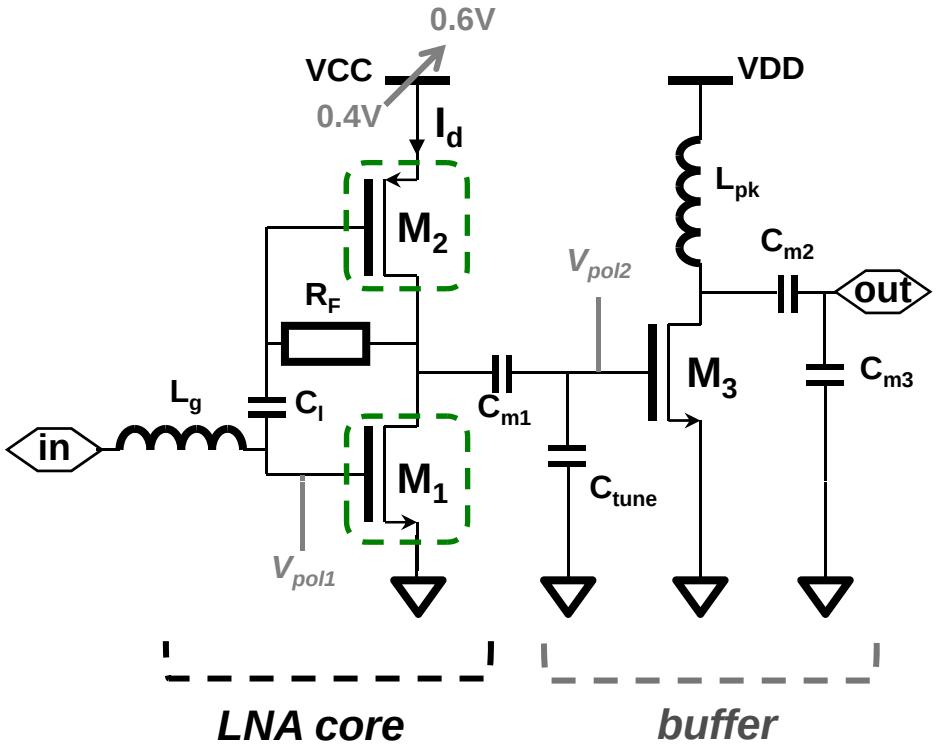


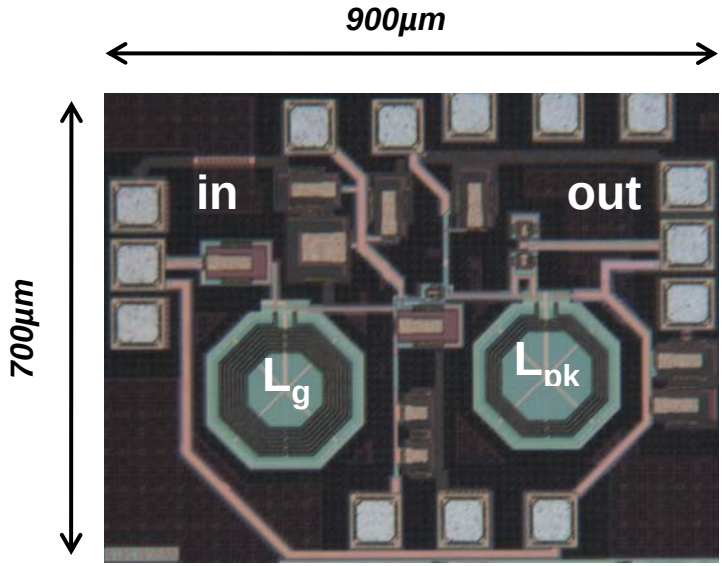
…the one of self biased inverter is the largest !

Ultra Low Power LNA

Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm



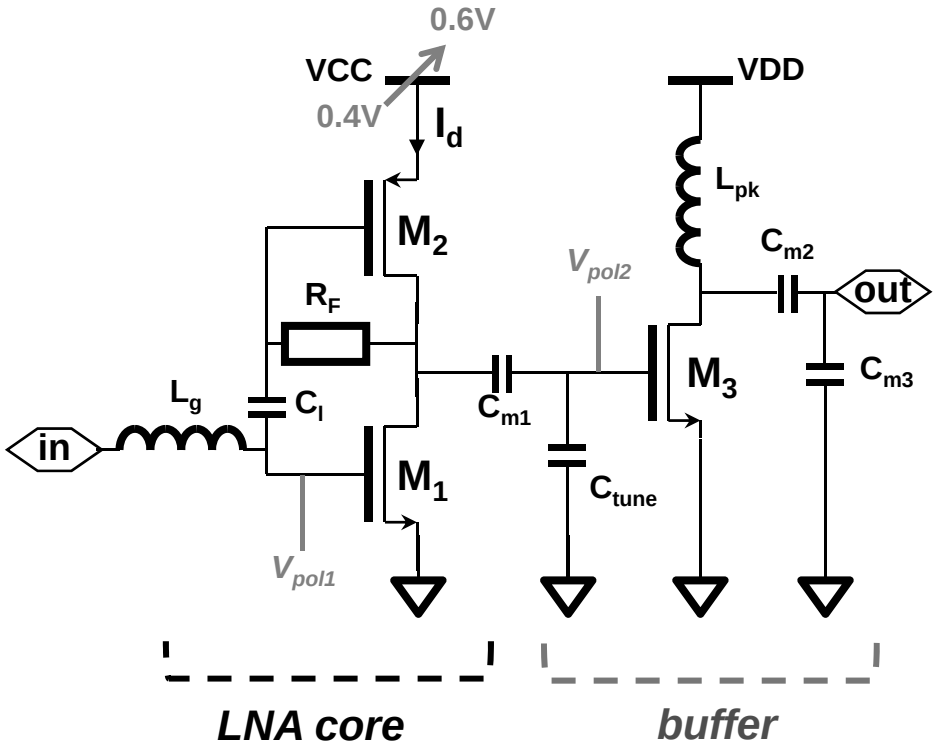


→ **Transistors are in MI region to maximise FOM_{LPLNA}**

Ultra Low Power LNA

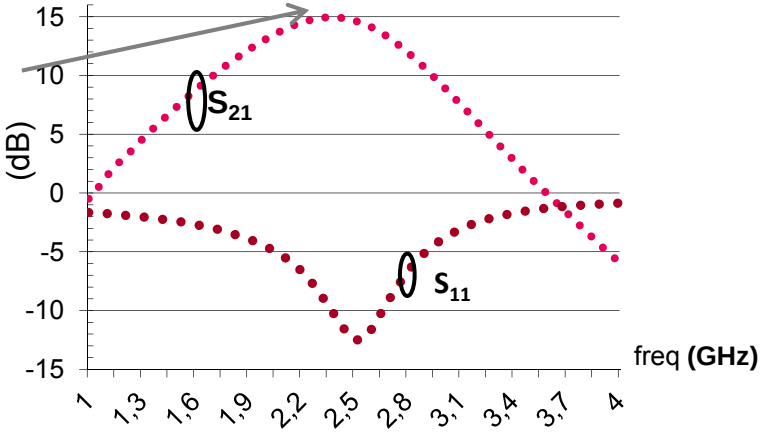
Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm

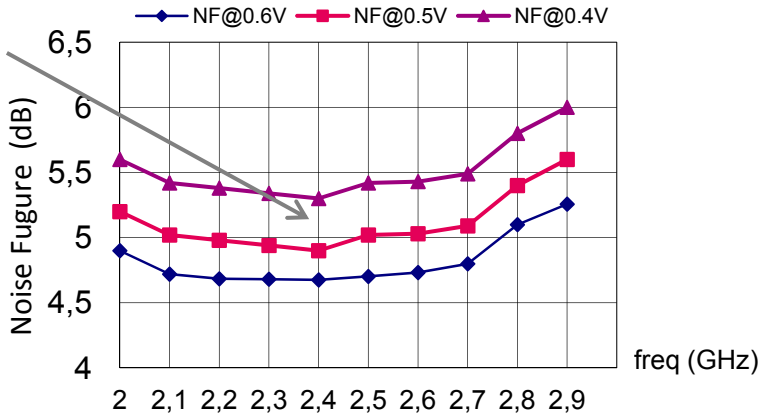


100µW@0.5V

15dB gain



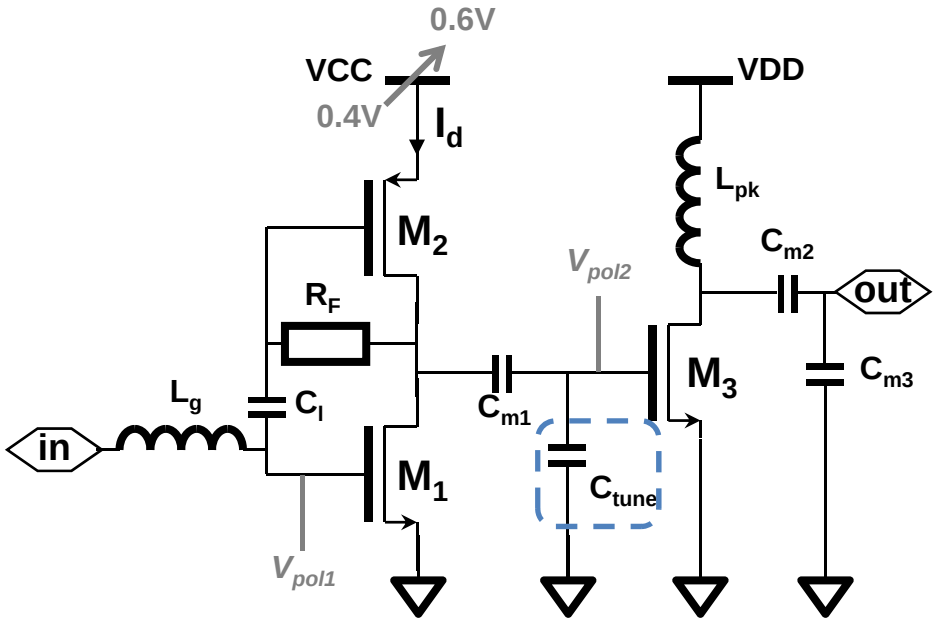
4.8dB NF



Ultra Low Power LNA

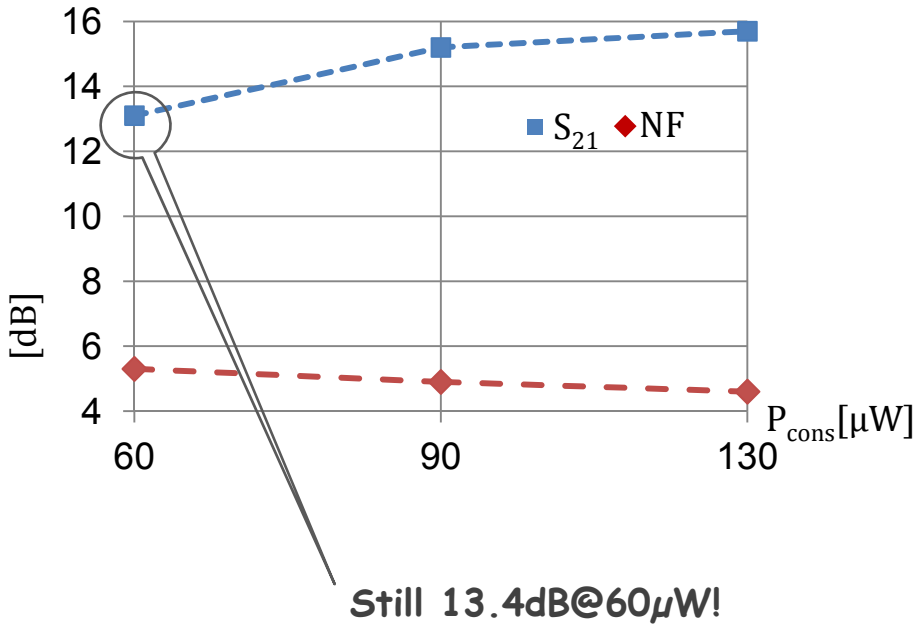
Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm



100µW@0.5V

Gain & NF vs Power Consumption

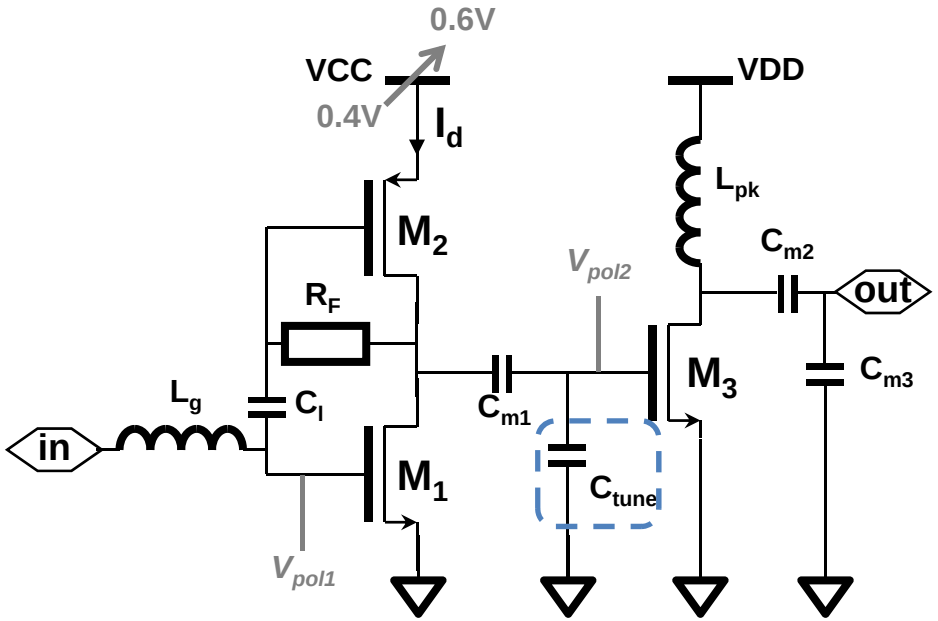


Ultra Low Power LNA

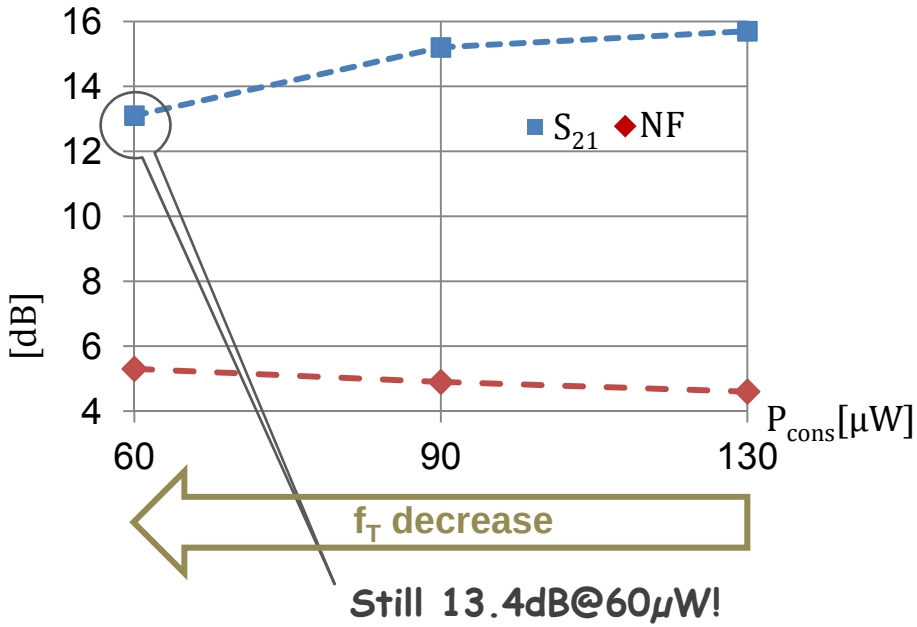
Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm

100µW@0.5V



Gain & NF vs Power Consumption



$$\rightarrow \frac{i_d}{v_{in}} = \frac{C_{tune}}{C_{gdT}} \frac{C_{gsT}.\omega}{2}$$

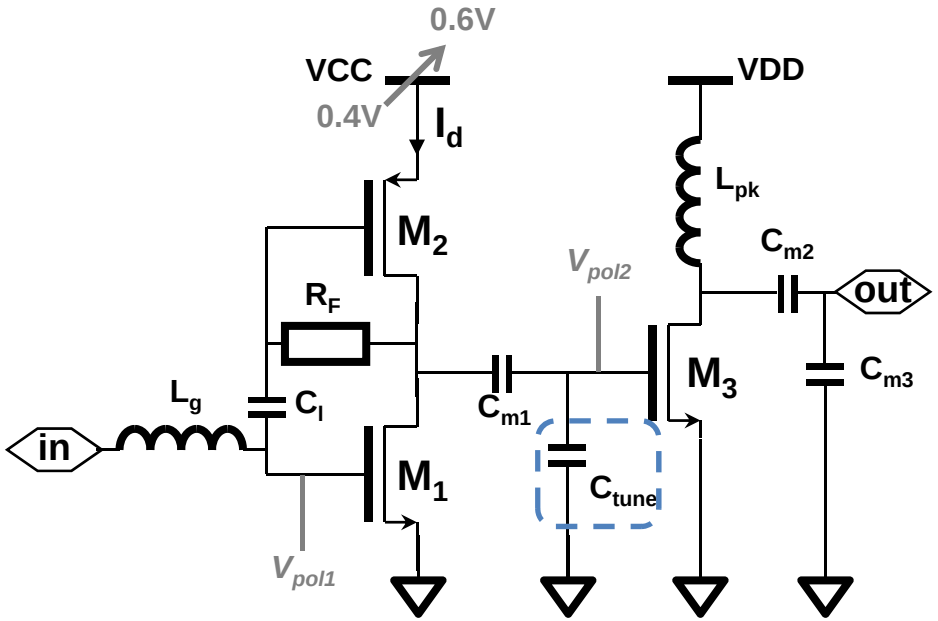
Capacitive feedback

Ultra Low Power LNA

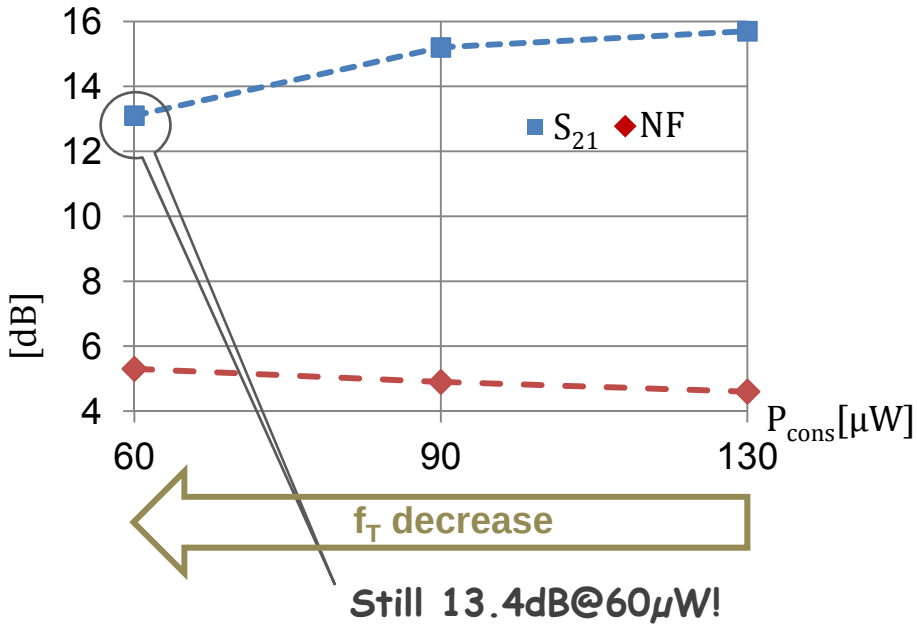
Current reuse LNA

2.4 GHz LNA - CMOS 0.13µm

100µW@0.5V



Gain & NF vs Power Consumption

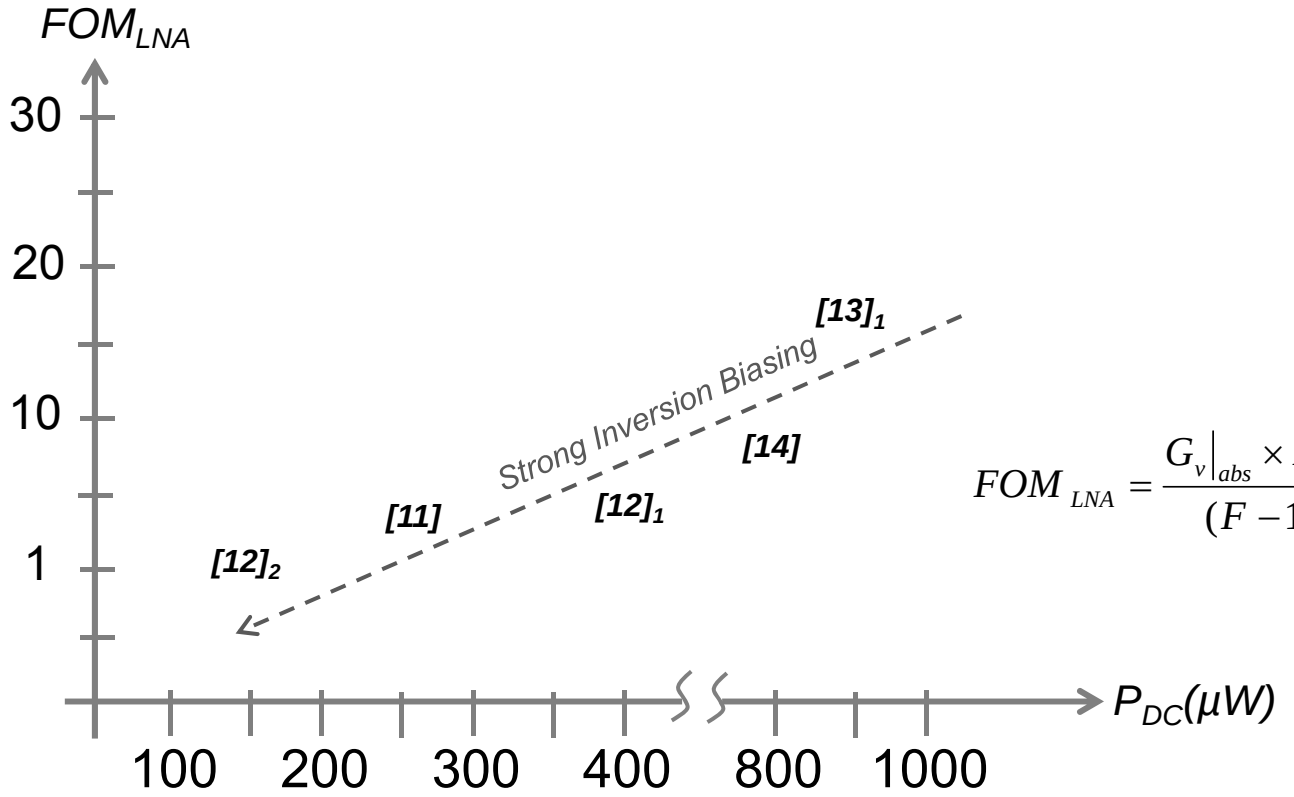


$$\rightarrow \frac{i_d}{v_{in}} = \frac{C_{tune}}{C_{gdT}} \frac{C_{gsT}.\omega}{2}$$

Capacitive feedback ⇨ ***Suited for MI operation***

Ultra Low Power LNA

Comparison with the state of art



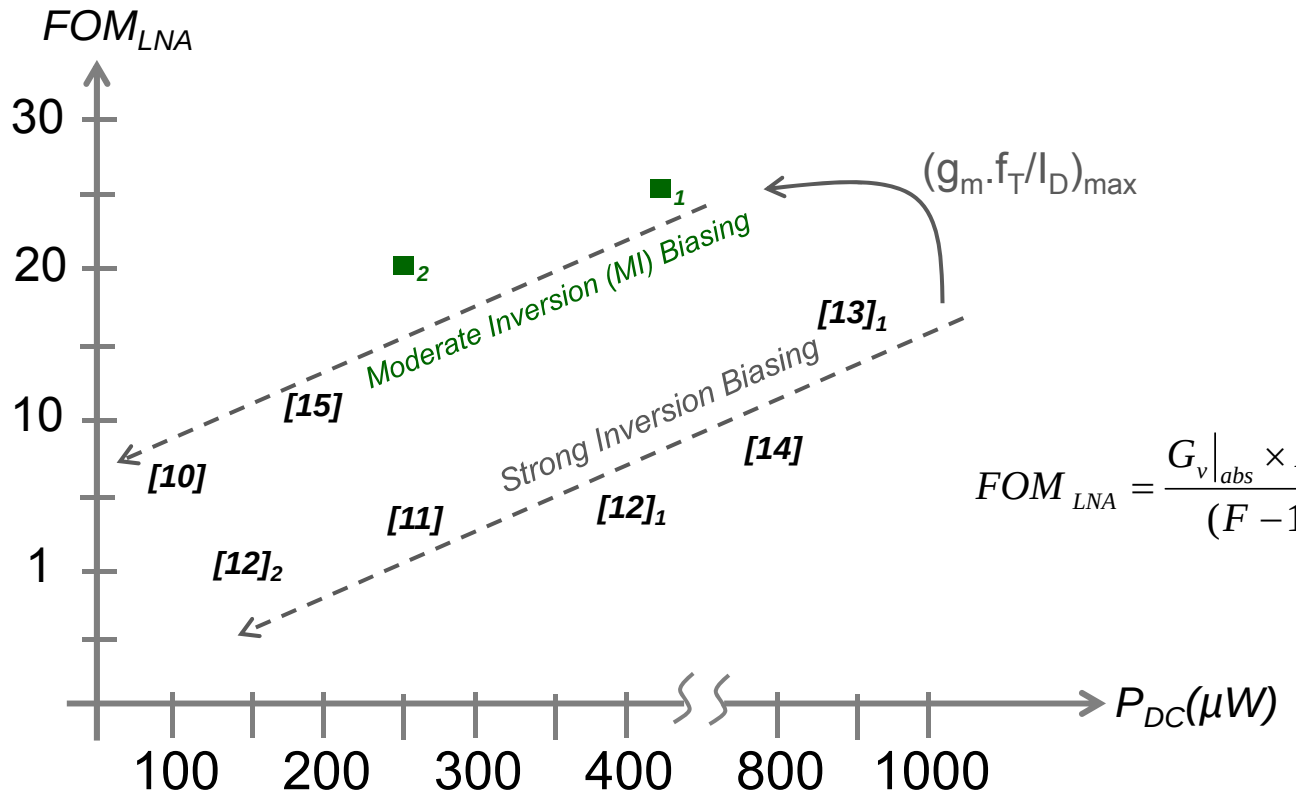
$$FOM_{LNA} = \frac{G_v\big|_{abs} \times IIP_3\big|_{mW} \times f_{RF}\big|_{GHz}}{(F-1)\big|_{abs} \times P_{cons}\big|_{mW}}$$

[10] A. Shameli"A novel Ultra Low Power Low Noise Amplifier using Differential Inductor Feedback", *IEEE ESSCIRC*, Montreux, Switzerland, Sep. 2006, pp.352-355
[11] B. G. Perumana, "A fully monolithic 260-µW, 1-GHz subthreshold low noise amplifier," *IEEE MiWCL*, Vol. 15, N°. 6, pp. 428-430, June 2005.
[12] H. Lee , "A 3 GHz subthreshold CMOS low noise amplifier," *IEEE RFIC Symposium*, San Francisco, CA, USA, June 2006, pp.545-548
[13] V. Aaron, « A subthreshold low-noise amplifier optimized for ultra-low -power applications in the ISM band", *IEEE MTT,* Vol. 56, N°2, pp. 286-292, feb. 2008
[14] J. Li, S. Hassan "A 0.7 V 850µW CMOS LNA for UHF RFID reader", *MOTL*, Vol. 52, N°12, pp. 2780-2782, dec. 2010
[15] C.J. Jeong, W. Qu, Y. Sun, D.Y. Soon, S.K. Han, S.G. Lee "A 1.5 V, 140 µA CMOS Ultra Low Power Common Gate LNA", *IEEE RFIC,* Baltimore, USA, June 2011, pp. 203-206

Ultra Low Power LNA

Comparison with the state of art

- *This work ⇒ Cascode*

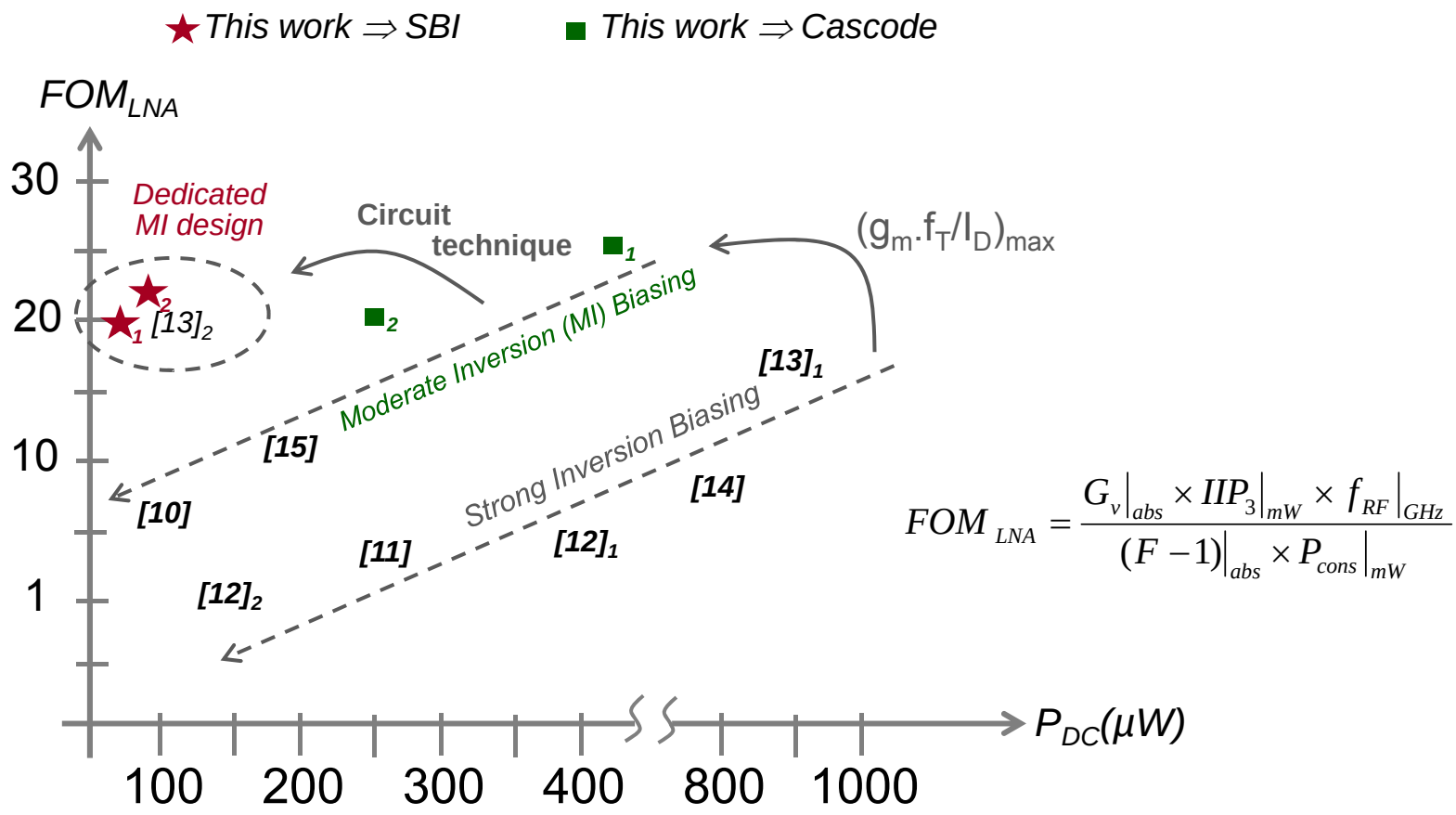


$$FOM_{LNA} = \frac{G_v\big|_{abs} \times IIP_3\big|_{mW} \times f_{RF}\big|_{GHz}}{(F-1)\big|_{abs} \times P_{cons}\big|_{mW}}$$

[10] A. Shameli"A novel Ultra Low Power Low Noise Amplifier using Differential Inductor Feedback", *IEEE ESSCIRC*, Montreux, Switzerland, Sep. 2006, pp.352-355
[11] B. G. Perumana, "A fully monolithic 260-µW, 1-GHz subthreshold low noise amplifier," *IEEE MiWCL*, Vol. 15, N°. 6, pp. 428-430, June 2005.
[12] H. Lee , "A 3 GHz subthreshold CMOS low noise amplifier," *IEEE RFIC Symposium*, San Francisco, CA, USA, June 2006, pp.545-548
[13] V. Aaron, « A subthreshold low-noise amplifier optimized for ultra-low -power applications in the ISM band", *IEEE MTT,* Vol. 56, N°2, pp. 286-292, feb. 2008
[14] J. Li, S. Hassan "A 0.7 V 850µW CMOS LNA for UHF RFID reader", *MOTL*, Vol. 52, N°12, pp. 2780-2782, dec. 2010
[15] C.J. Jeong, W. Qu, Y. Sun, D.Y. Soon, S.K. Han, S.G. Lee "A 1.5 V, 140 µA CMOS Ultra Low Power Common Gate LNA", *IEEE RFIC,* Baltimore, USA, June 2011, pp. 203-206

Ultra Low Power LNA

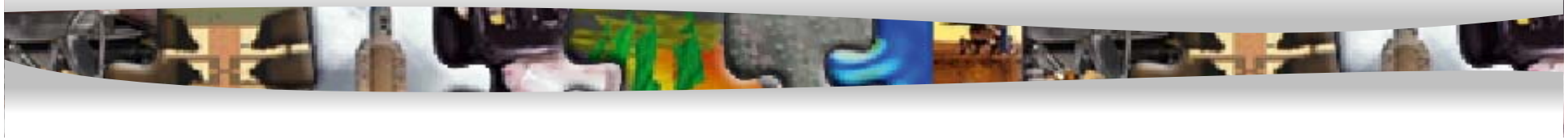
Comparison with the state of art



$$FOM_{LNA} = \frac{G_v\big|_{abs} \times IIP_3\big|_{mW} \times f_{RF}\big|_{GHz}}{(F-1)\big|_{abs} \times P_{cons}\big|_{mW}}$$

[10] A. Shameli"A novel Ultra Low Power Low Noise Amplifier using Differential Inductor Feedback", *IEEE ESSCIRC*, Montreux, Switzerland, Sep. 2006, pp.352-355
[11] B. G. Perumana, "A fully monolithic 260-µW, 1-GHz subthreshold low noise amplifier," *IEEE MiWCL*, Vol. 15, N°. 6, pp. 428-430, June 2005.
[12] H. Lee , "A 3 GHz subthreshold CMOS low noise amplifier," *IEEE RFIC Symposium*, San Francisco, CA, USA, June 2006, pp.545-548
[13] V. Aaron, « A subthreshold low-noise amplifier optimized for ultra-low -power applications in the ISM band", *IEEE MTT,* Vol. 56, N°2, pp. 286-292, feb. 2008
[14] J. Li, S. Hassan "A 0.7 V 850µW CMOS LNA for UHF RFID reader", *MOTL*, Vol. 52, N°12, pp. 2780-2782, dec. 2010
[15] C.J. Jeong, W. Qu, Y. Sun, D.Y. Soon, S.K. Han, S.G. Lee "A 1.5 V, 140 µA CMOS Ultra Low Power Common Gate LNA", *IEEE RFIC,* Baltimore, USA, June 2011, pp. 203-206

OUTLINE

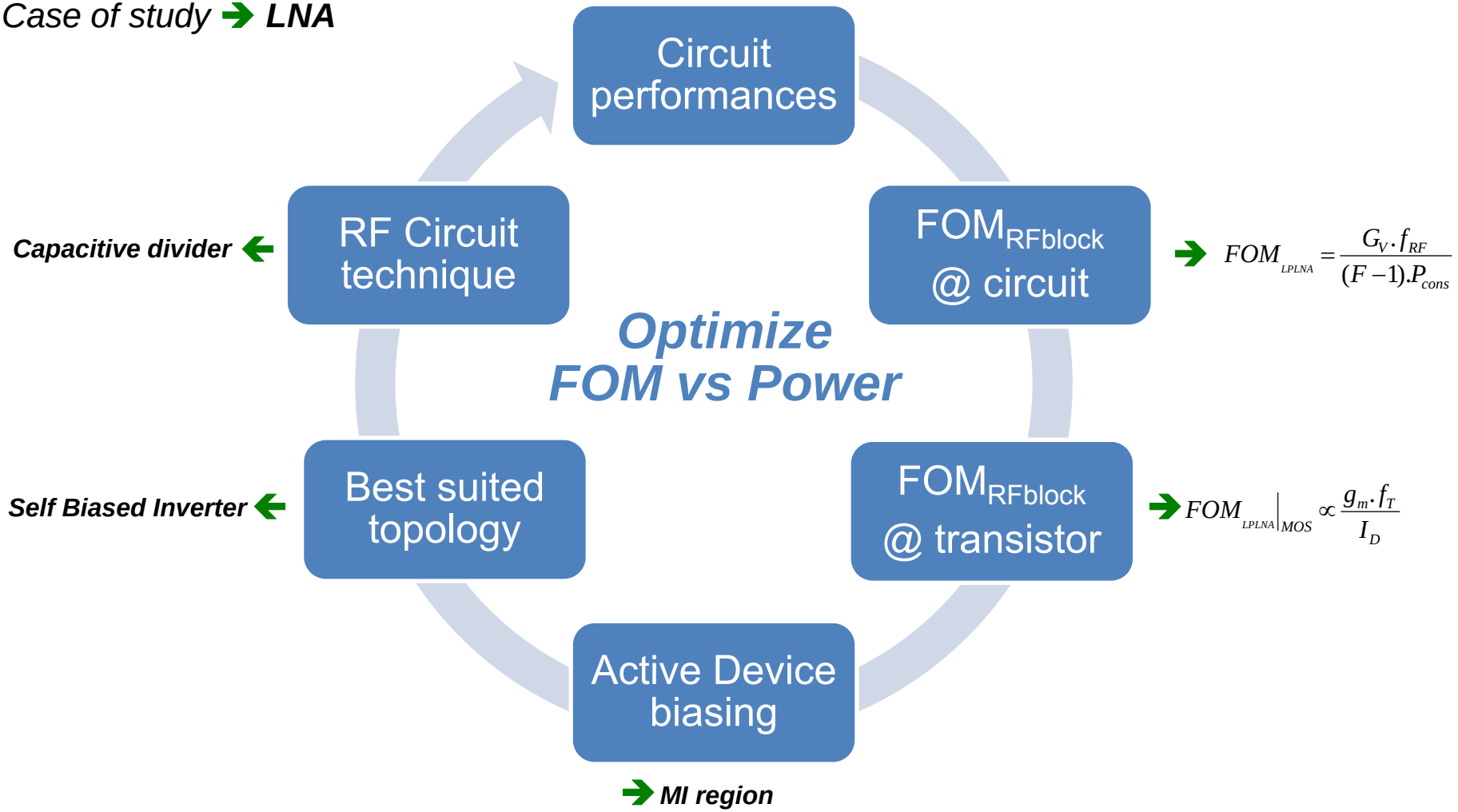


- Context
- From analog to RF Metric
- Low Noise Amplifier Implementation
- **Conclusions & Perspectives**

Conclusions & Perspectives

RF Building Block Design Methodology

Case of study ➔ ***LNA***



$$FOM_{LPLNA} = \frac{G_V \cdot f_{RF}}{(F-1).P_{cons}}$$

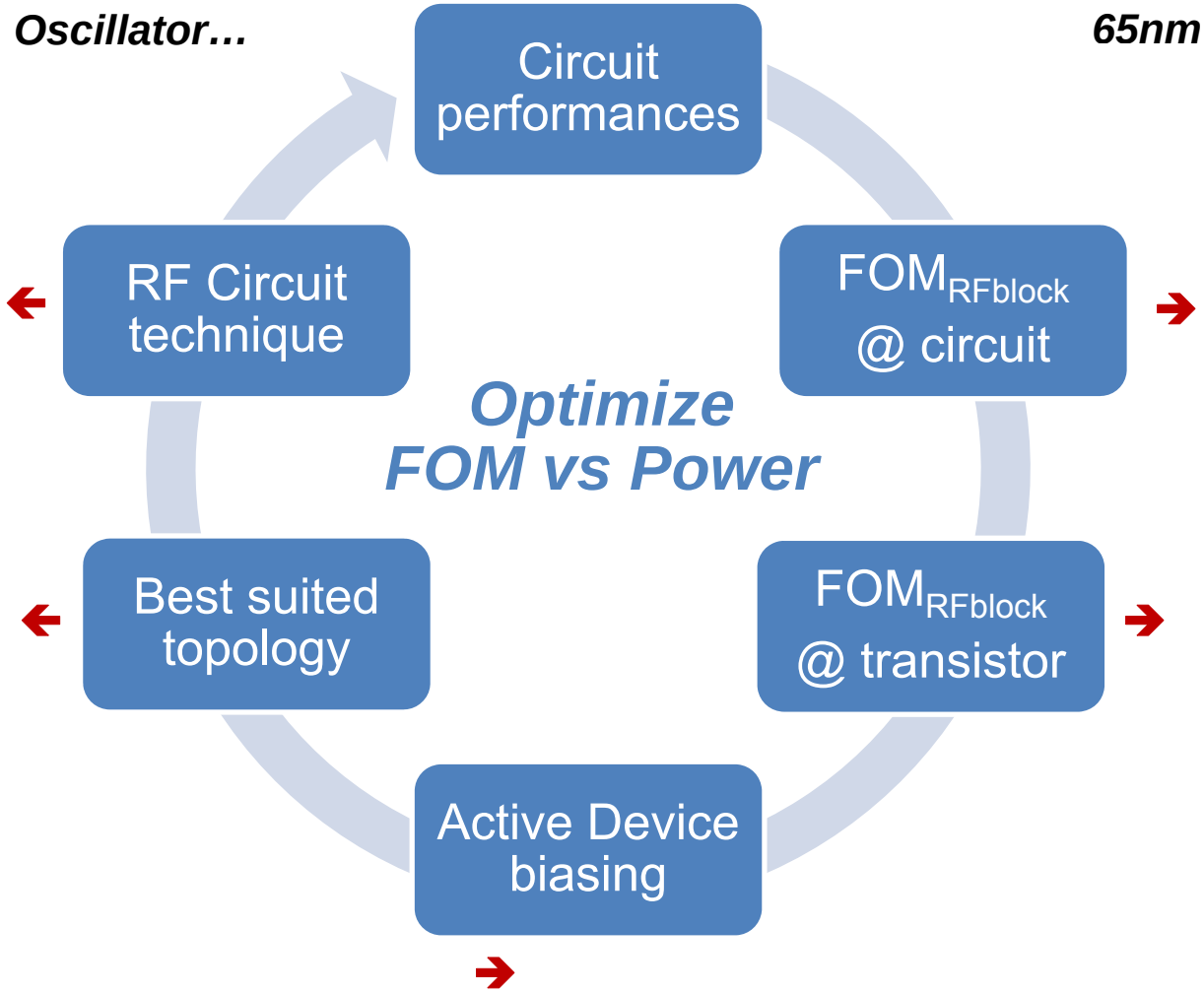
$$FOM_{LPLNA}\Big|_{MOS} \propto \frac{g_m \cdot f_T}{I_D}$$

Conclusions & Perspectives

RF Building Block Design Methodology

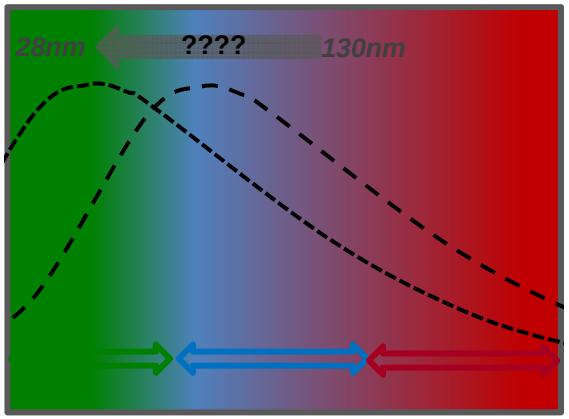
To do ➔ ***Mixer, Oscillator…***

65nm ➔ ***28nm***



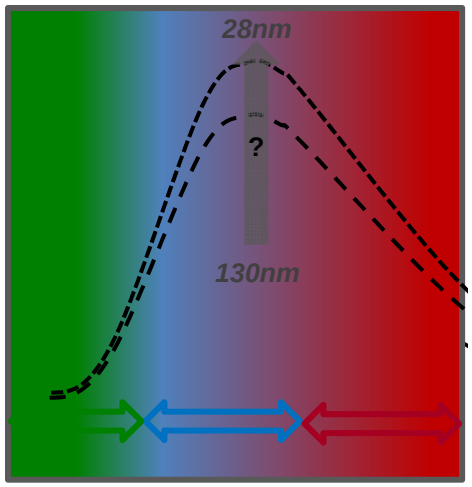
- $FOM_{RFblock@transistor}$ versus technology scaling ?

$FOM_{LPLNA}=g_m.f_T/I_D$



OR

$FOM_{LPLNA}=g_m.f_T/I_D$



?

➡ **A matter of Device Modelling**