BSIM-CMG
A Turnkey Compact Model for Common Multi Gate Devices

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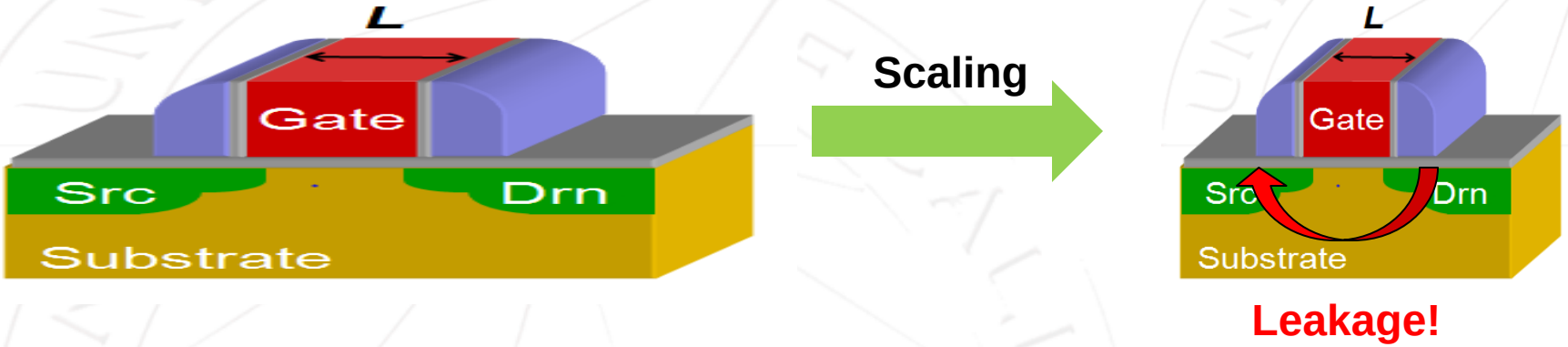
UC Berkeley

Dec. 16, 2011

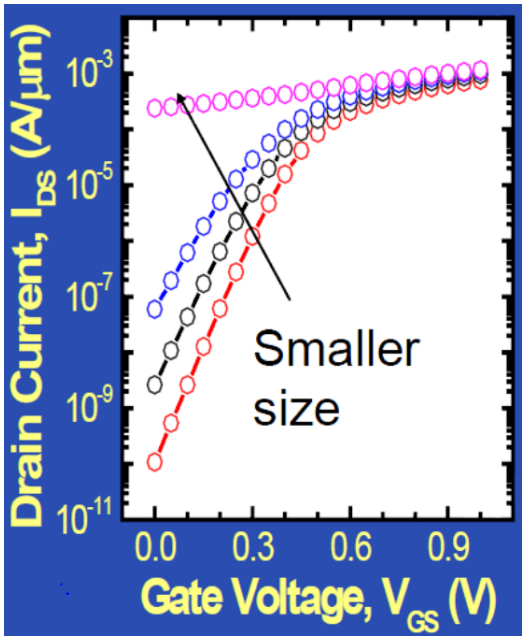
Nano-Tera Workshop, EPFL, Lausanne

Why next generation transistors?



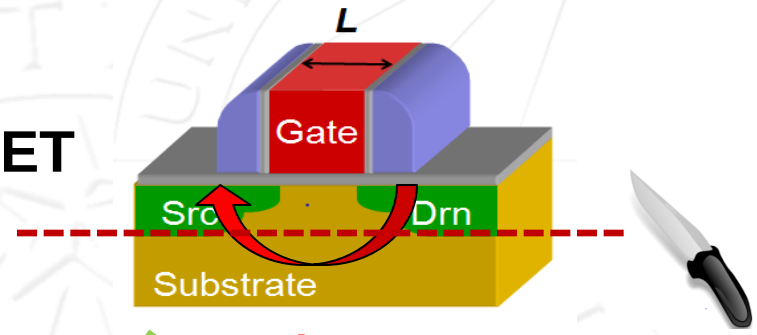
Leakage!

- Gate cannot control the leakage paths <u>far from the gate</u>
- Thinning the oxide down was <u>not</u> enough
- Dopant fluctuations => Increased variability

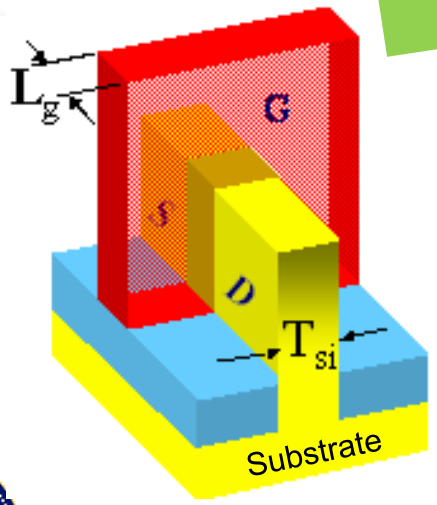


New MOSFET Structures

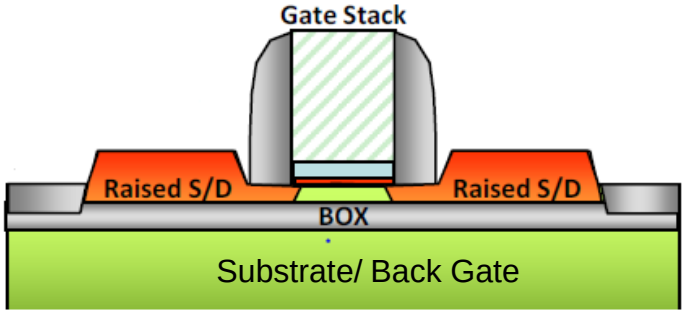
Bulk Planar MOSFET



Leakage!

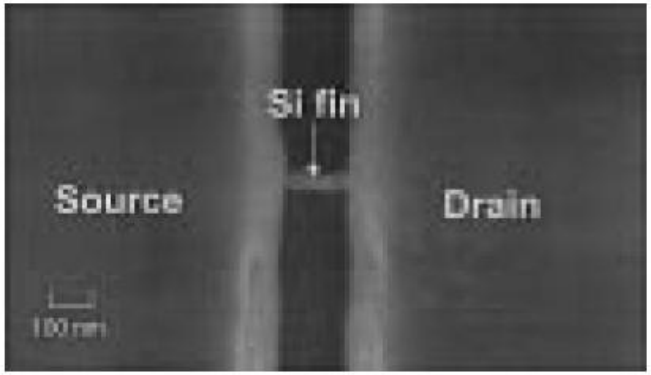


FinFET

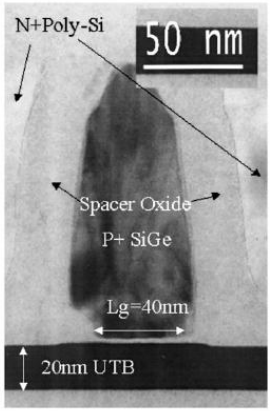


UTBSOI

New MOSFET Structures - Demonstration



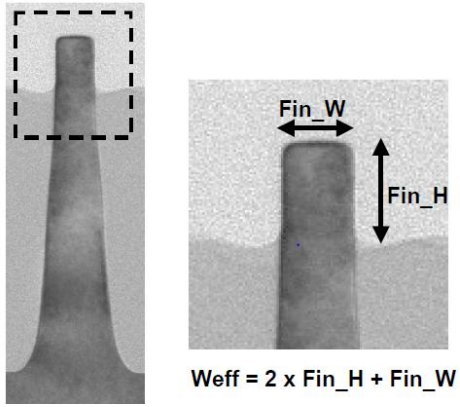
*X. Huang et al. IEDM 1999 (**UC Berkeley**)*



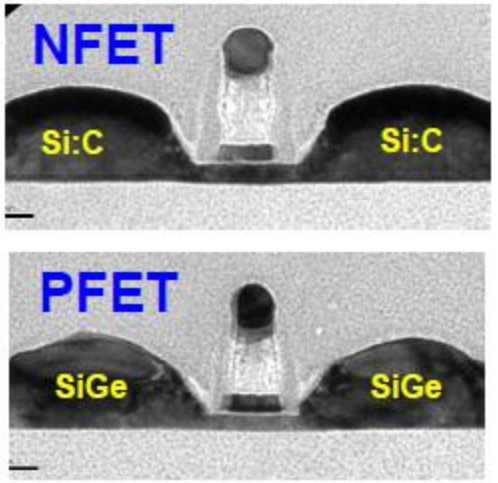
*Y. Choi et al. IEEE EDL 2000- (**UC Berkeley**)*

FinFET

UTBSOI

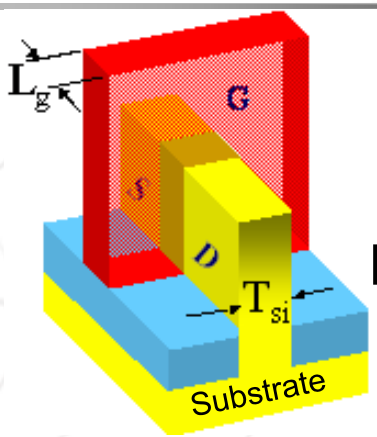


C.C. Wu et al. IEDM 2010 (TSMC)

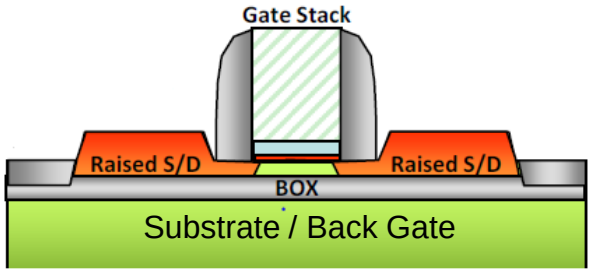


K. Cheng et al. IEDM 2009 - (IBM / ST)

Advantages for SoC Design



FinFET



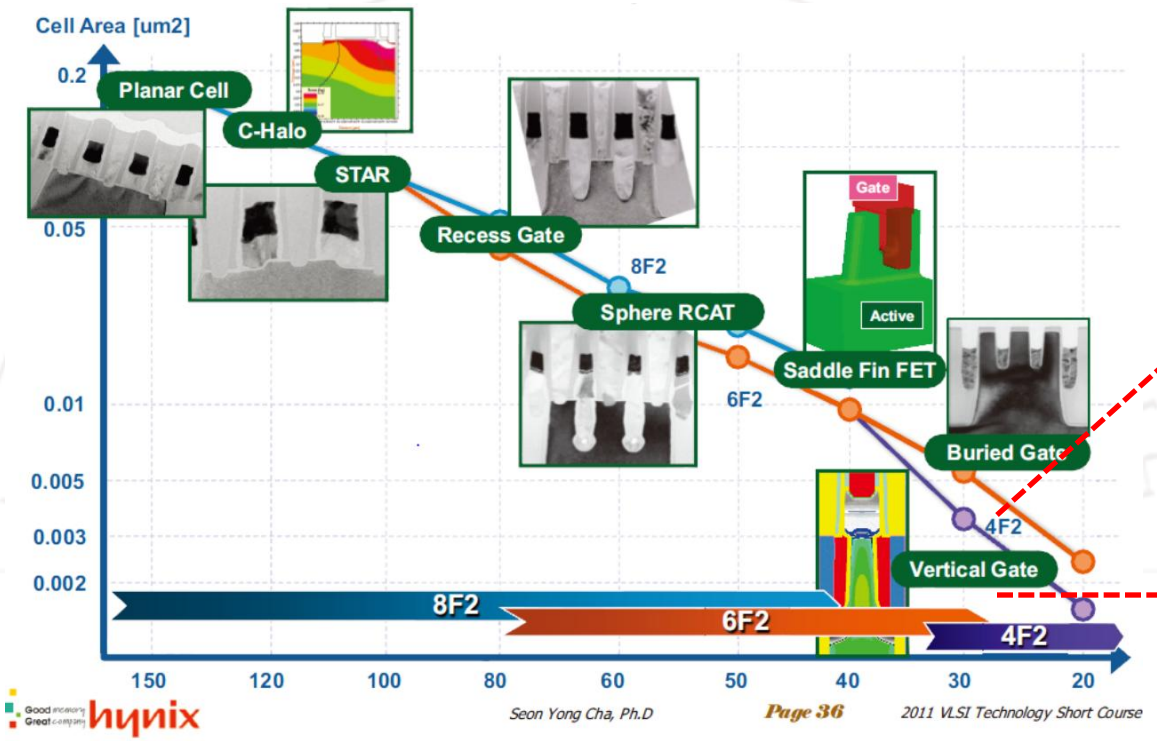
UTBSOI

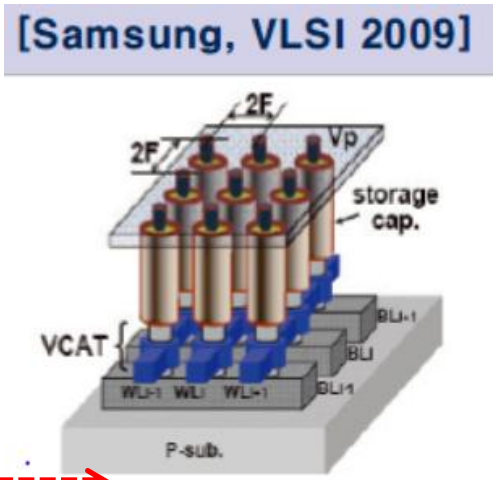
- No doping required in the channel
- Superior short channel control
  - Lower DIBL
  - Steeper on-off
- Improved mobility
  - Lower vertical field needed
  - Less scattering in the channel
- Lower gate-induced drain leakage
- Next Gen.: Scale by thinning body

Improves lower-V_{dd} logic operations

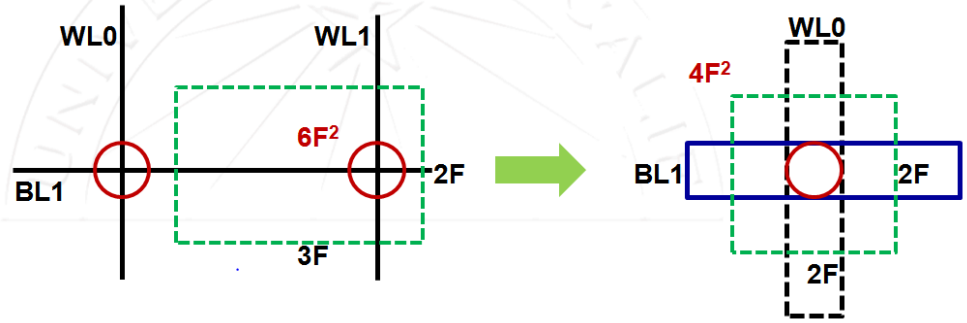
Stand-by power savings in HVT devices

Another MOSFET architecture





- DRAM Cell Transistor – $4F^2$ lavout

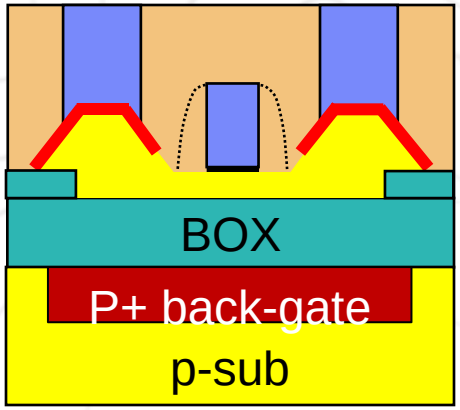


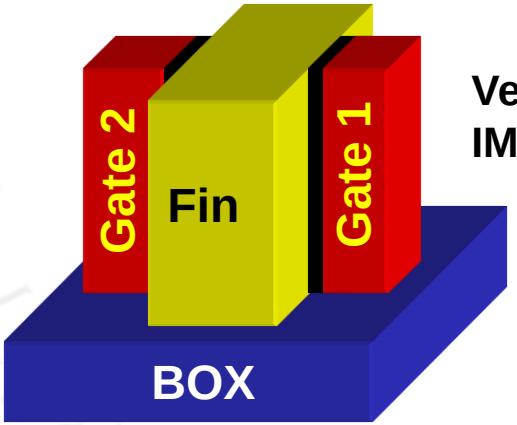
Versatile Multi-Gate Compact Model: BSIM-MG

BSIM-IMG

UTBSOI

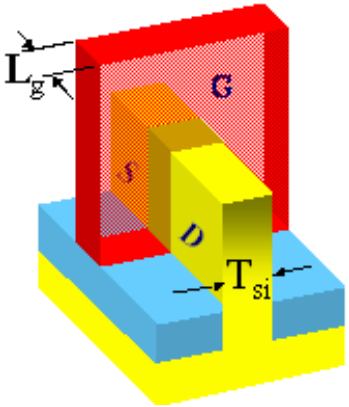
BG-ETSOI

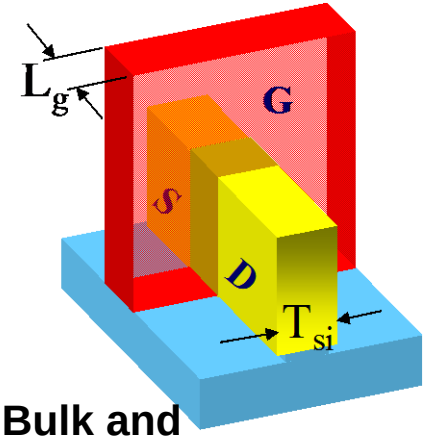




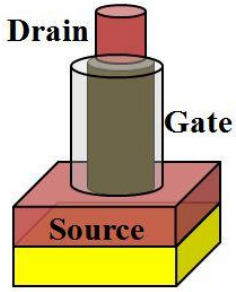
Vertical Fin IMG

BSIM-CMG

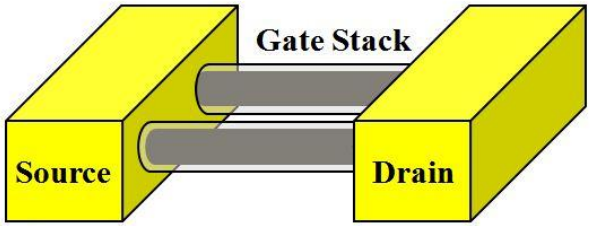




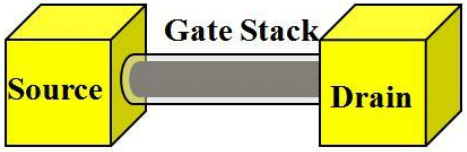
FinFETs on Bulk and SOI Substrates



Vertical CG FET

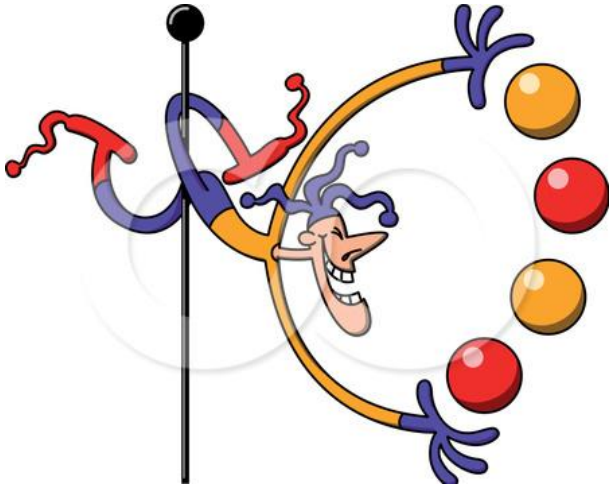


Twin Silicon Nanowire FET



Horizontal Nanowire FET

Challenges in developing a new model



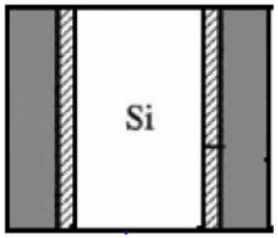
- New Physics
  - Fully depleted channel
  - Quantum confinement etc.
  - When to include them?
- Support Multiple Device architectures
- Inertia with BSIM4
  - Large user base
  - Familiarity with the parameters -> a language in itself
- Speed
- Convergence – Model behavior in extreme cases
- Balance Physics and Flexibility
- Balance Speed and Accuracy

BSIM-CMG

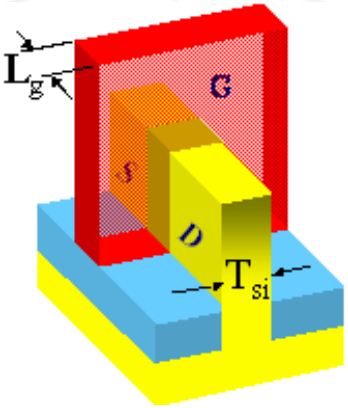
- Introduction
- **Core Model**
  - **Surface Potential Equation**
  - **Drain Current**
  - **Capacitance Model**
- Real Device Effects
- Model Validation & QA
- Conclusion

BSIM-CMG Core Models

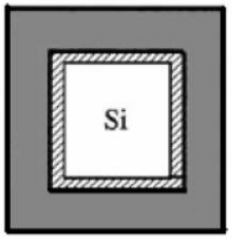
- Four device architectures



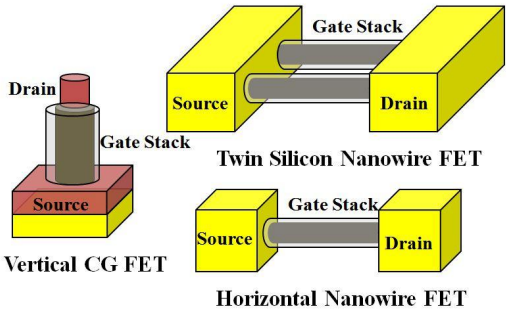
Double Gate



Double Gate / Trigate / FinFET



Quadruple Gate

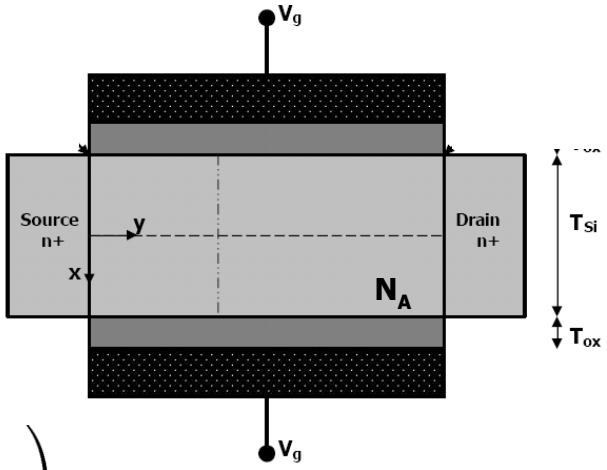


Cylindrical Gate / Nanowire FET

- Three core models
  - Intrinsic Double Gate Core (*Y. Taur et al, IEEE EDL, 2004*)
  - Perturbation based DG Core for high-doping
  - Cylindrical Gate Core
- Bulk and SOI Substrate

Surface Potential Core – Double Gate

- Surface potential is obtained from the solution of Poisson's equation and Gauss's Law.
- Poisson's equation inside the body can be written as (V_{ch} is channel potential)



$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\epsilon_{Si}} \cdot \left(\underbrace{e^{\frac{q\psi}{kT}} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{-\frac{qV_{ch}}{kT}}}_{\text{Inversion Carriers}} + \underbrace{e^{\frac{q\phi_B}{kT}}}_{\text{Body Doping}} \right)$$

$$\text{where } \phi_B = \frac{kT}{q} \ln\left(\frac{N_A}{n_i}\right)$$

- Body doping complicates the solution of the Poisson's equation.
- Perturbation approach is used to solve this problem.

M. Dunga et al., IEEE TED, Vol. 53, No. 9, 2006

M. Dunga et al., VLSI 2007

Mohan Dunga, PhD Dissertation, UC Berkeley

Surface Potential Core – Cylindrical Gate

- Start with a long channel transistor

$$\frac{1}{r}\cdot\frac{d}{dr}\left(r\frac{d\psi}{dr}\right)=\frac{qN_a}{\epsilon_{si}}+\frac{qN_a}{\epsilon_{si}}\exp\left(\frac{\psi-V_{ch}-2\phi_b}{V_t}\right)$$

1-D Poisson's Equation

- Assumptions
  - Gradual Channel Approximation
  - No influence of holes (SOI like structure)
  - Fully Depleted Body
- Gauss Law + Correction for Polysilicon Gate-Depletion
  - Implicit equation in Q_i (channel charge)

$$V_{gs}-V_{fb}-\Delta V_{th}-V_{ch}=c_{poly}\cdot\left(\frac{Q_i+Q_{dep}}{C_{ox}}\right)^2+\frac{Q_i}{C_{ox}}+V_t\cdot ln\frac{Q_i}{V_tC_{ox}}+V_t\cdot ln\left(1+H\cdot\frac{Q_i}{C_{ox}V_t}\right)$$

Surface Potential Equation

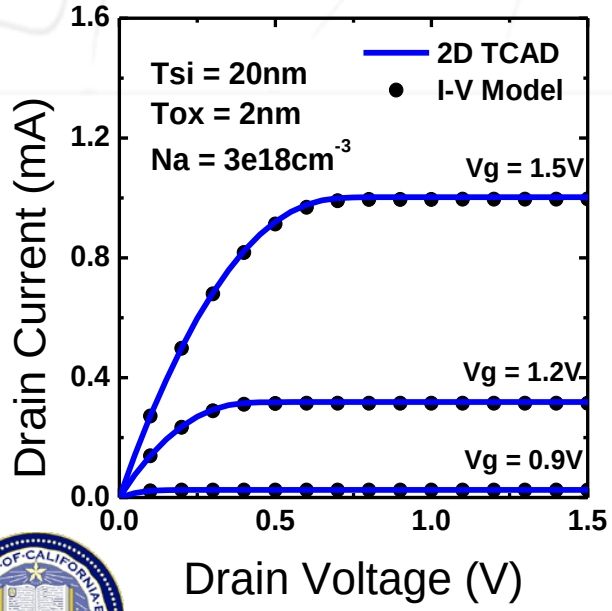
S.Venugopalan et. al., SSE, Vol 67, Issue 1, Jan 2012

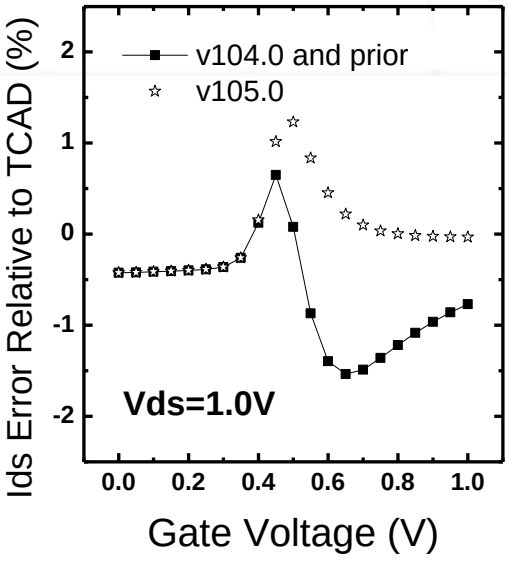
Core Drain Current Model

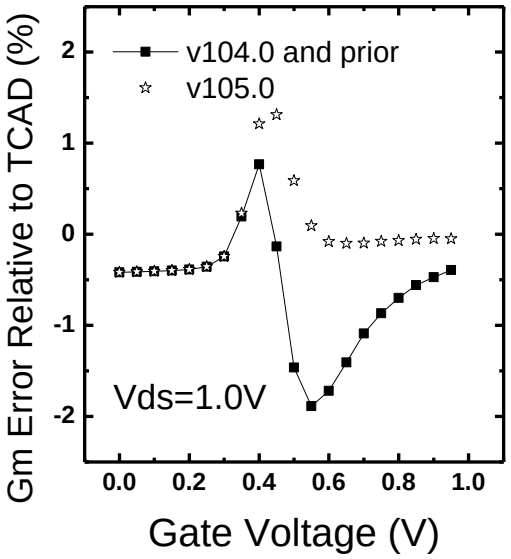
- Drain Current (Pao-Sah, No charge sheet approximation)

$$Id = \mu \cdot \frac{W_{eff}}{L_{eff}} \cdot \left[\frac{Q_{is}^2 - Q_{id}^2}{2\,C_{ox}} + V_t \cdot \left(2 - \frac{2\,Q_0}{2\,Q_0 + Q_{is} + Q_{id}} \right) (Q_{is} - Q_{id}) \right]$$

$$Q_0 = 2Q_B + 5V_t C_{si}$$

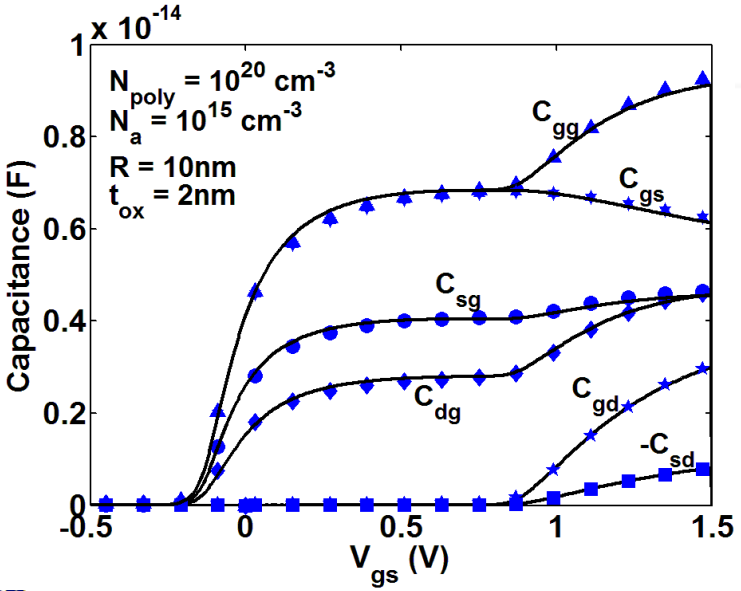


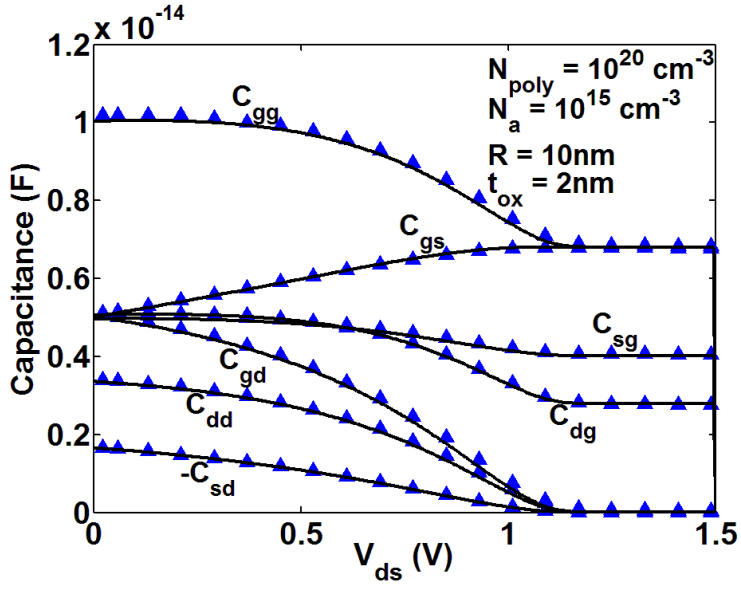




Core Capacitance Model

- Model inherently exhibits symmetry
  - $C_{ij} = C_{ji}$ @ $V_{ds} = 0$ V
- Model overlies TCAD results
  - No tuning parameters used
- Accurate short channel behavior – RF Design
  - Needs additional tuning parameter flexibility





Symbols: TCAD Results; Lines: Model

BSIM-MG

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- **Real Device Effects**
- Model Validation & QA
- Conclusion

Short Channel (2D) Effects

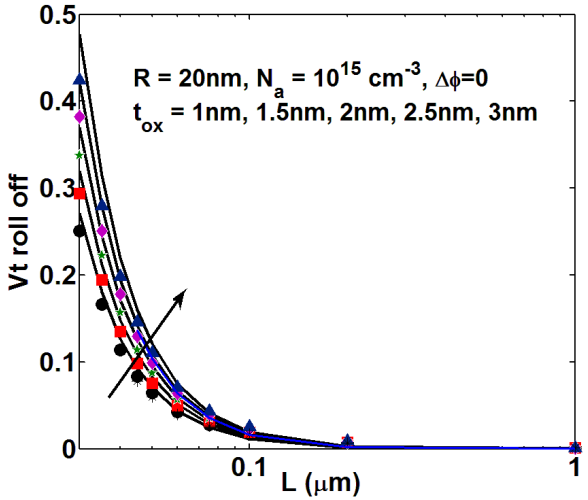
$$\frac{1}{r}\cdot\frac{\partial}{\partial r}\left(\frac{\partial\psi}{\partial r}\right)+\frac{\partial^2}{\partial y^2}\psi=\frac{qN_a}{\epsilon_{si}}$$

- Along the channel – 2D
- Quasi-2D analysis

$$\frac{d^2\psi_c}{dy^2}+\frac{V_{gs}-V_{fb}-\psi_c}{\lambda^2}=\frac{qN_a}{\varepsilon_{si}}$$

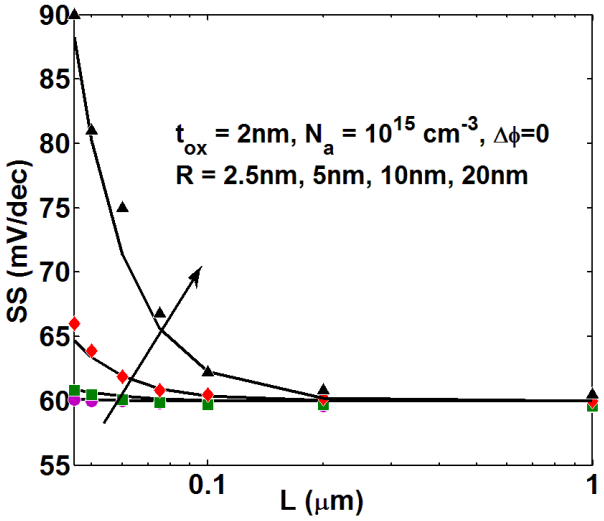
Characteristic Length

$$\lambda=\sqrt{\frac{R^2}{4}+\frac{\epsilon_{si}}{2\epsilon_{ox}}R\cdot EOT}$$



Symbols: TCAD Results; Lines: Model

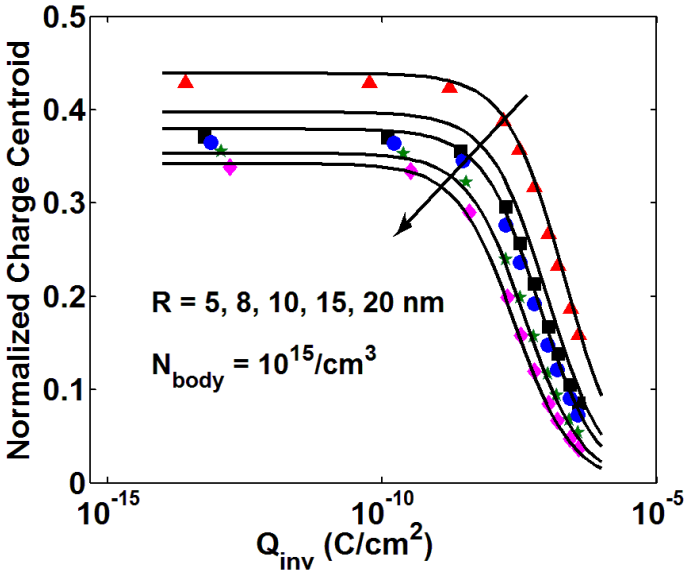
- Similar expression for Double Gate and FinFET/Trigate
- Analytical expressions model
  - Threshold Voltage roll off
  - Drain induced barrier lowering (DIBL)
  - Sub-threshold swing degradation

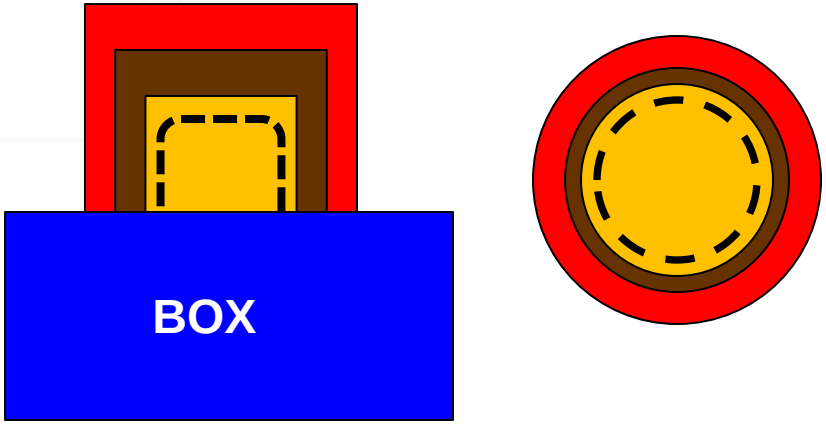


Auth and Plummer, IEEE EDL, 2007

Quantum Mechanical Effects

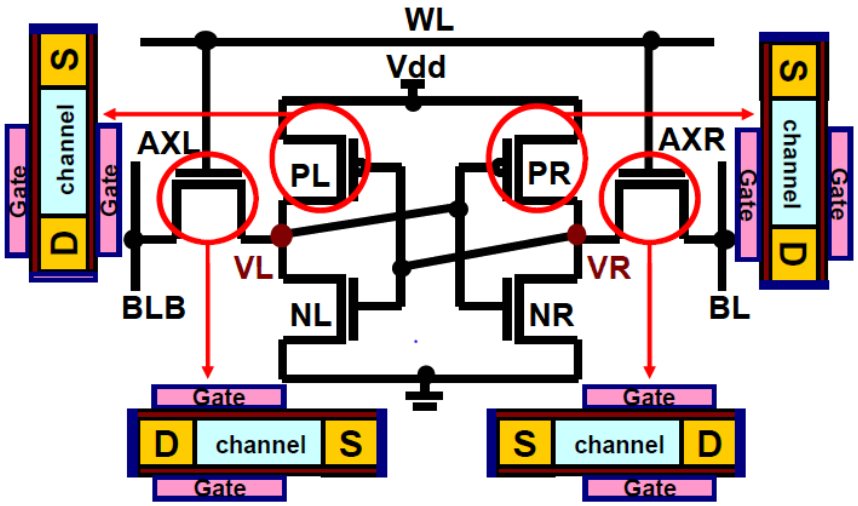
- Predictive model for confinement induced V_{th} shift due to band splitting present in the model
- Can choose to use an effective t_{ox} that accounts for charge centroid behavior with bias
- Effective Width model that accounts for reduction in width for a triple / quadruple / surround gate structure

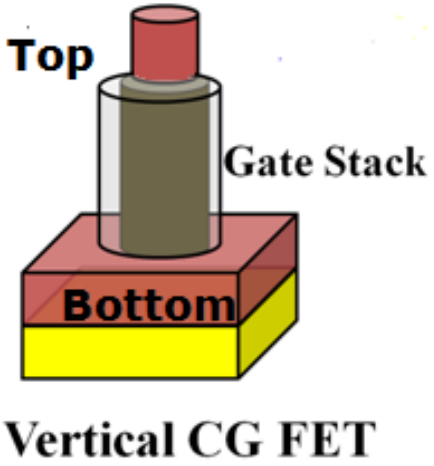




Width reduction due to structural confinement of inversion charge. (Dotted lines represent the effective width perimeter)

Asymmetric Device Model





Vertical CG FET

V.P.Hu et al VLSID 2006

- S/D under-lapped FinFETs used as PU and AX transistors in SRAMS show
  - Improved RSNM at same WSNM
  - Decreased Time-to-Write (but increased cell read access time)
- Asymmetric Halo could be used to create I/O FinFETs for special applications

Asymmetry Model : Parameters Identified

- Identified five existing parameters and created their reverse mode equivalents

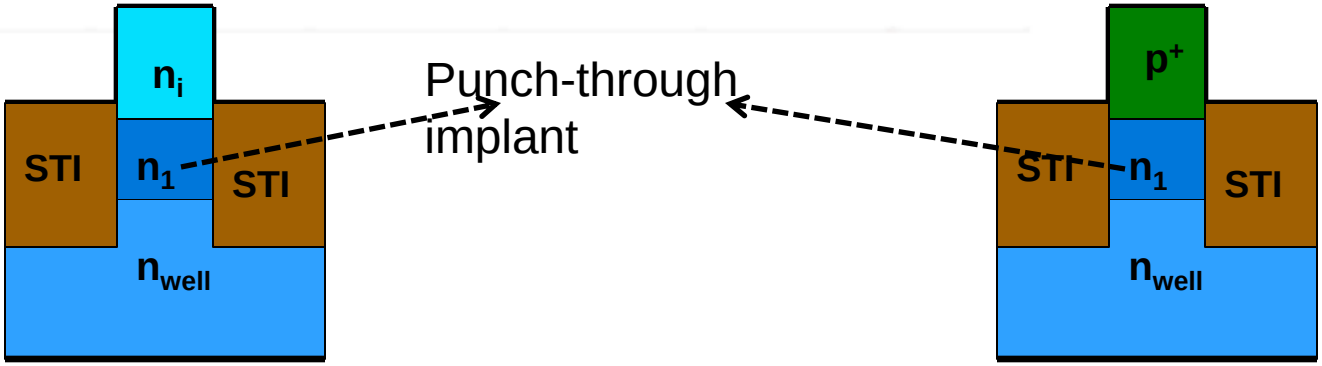
- Doping Gradient in Channel
  - On-current degradation parameter
  - Source-side barrier different – DIBL parameter
  - Output conductance parameter

- Top/Bottom Electrode Asymmetry
  - Quasi-saturation amplification / suppression – $R_{s/d}$ Parameters

S. Venugopalan et al., NVMTS 2011

Source/Drain Junctions in FinFETs

- FinFETs on Bulk require an implant positioned just below the fin to prevent punch-through (and a retrograde profile).
  - Creates S/D junctions to have two metallurgical junctions of the form p^+-n_1-n_{well} or n^+-p_1-p_{sub}.
  - Simulations indicate that the depletion region beneath the junction could traverse the second junction too.



Cross-section at middle of channel

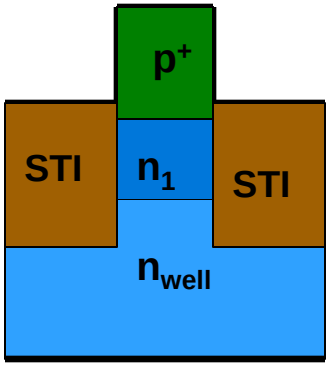
Cross-section at S/D junction

S/D Junction Cap in FinFETs - Model

- Enhanced BSIM4 style junction charge model with just 2 additional parameters – C_{j02} and m_2

$$Q_{jn,rev} = C_{j01}\phi_{b1}\frac{1-\left(1-\frac{V_{bs/d}}{\phi_{b1}}\right)^{1-m_1}}{1-m_1} \qquad V_{bc}<=V_{bs/d}<=0$$

$$= C_{j01}\phi_{b1}\frac{1-\left(1-\frac{V_{bc}}{\phi_{b1}}\right)^{1-m_1}}{1-m_1} + C_{j02}\phi_{b2}\frac{1-\left(1-\frac{V_{bs/d}}{\phi_{b2}}\right)^{1-m_2}}{1-m_2} \qquad V_{bs/d}<= V_{bc}$$



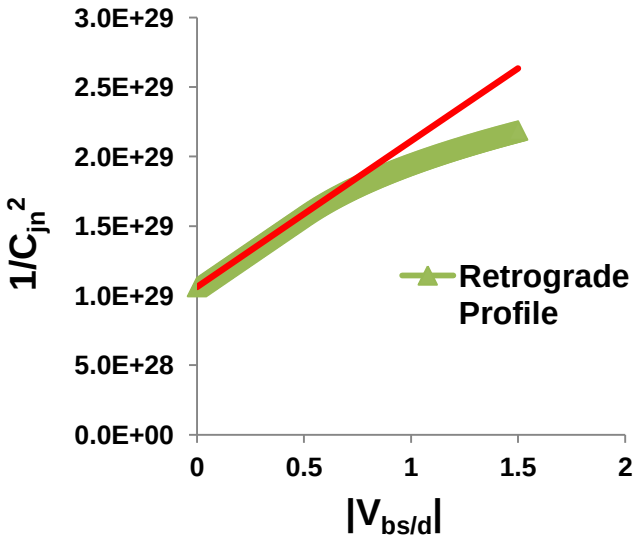
Cross-section at S/D junction

where,

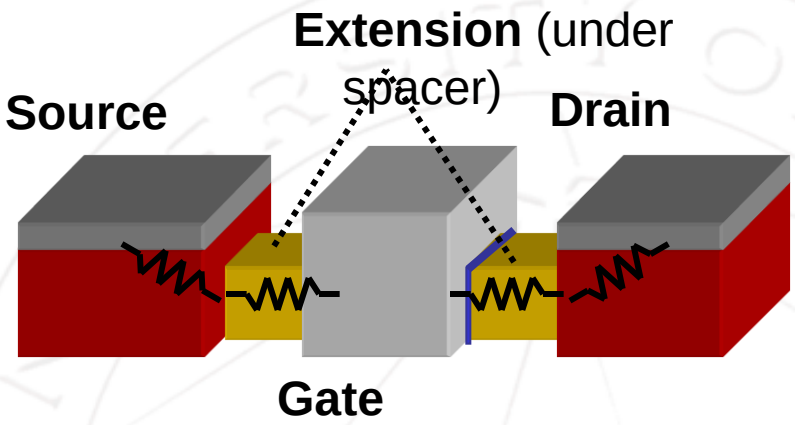
$$V_{bc} = \phi_{b1}\left(1-\left(\frac{C_{j01}}{C_{j02}}\right)^{\frac{1}{m_1}}\right)$$

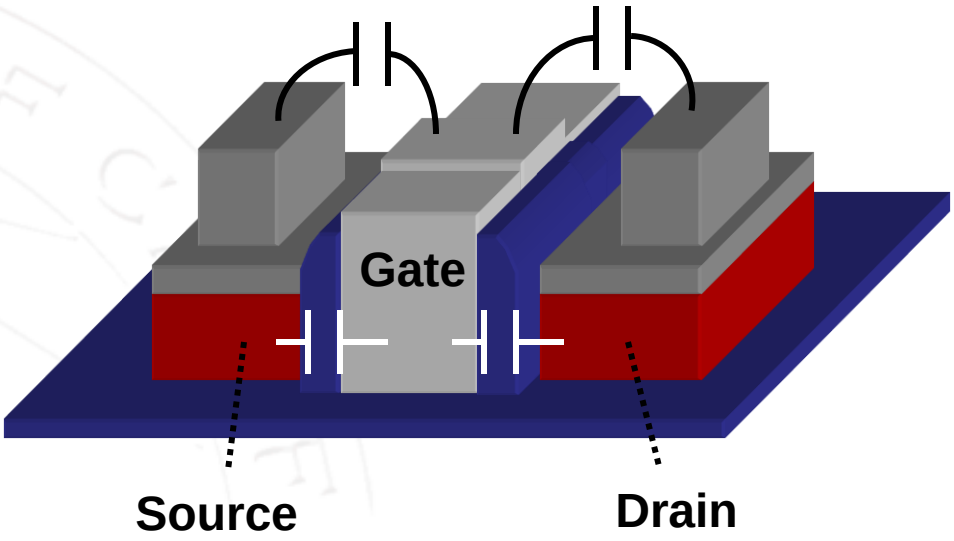
$$\phi_{b2} = \frac{C_{j02}\phi_{b1}m_2}{C_{j01}m_1\left(1-\frac{V_{bc}}{\phi_{b1}}\right)^{-1-m_1}}$$

V_{bc}: the voltage at when the depletion edge reaches the n_1-n_{well} boundary



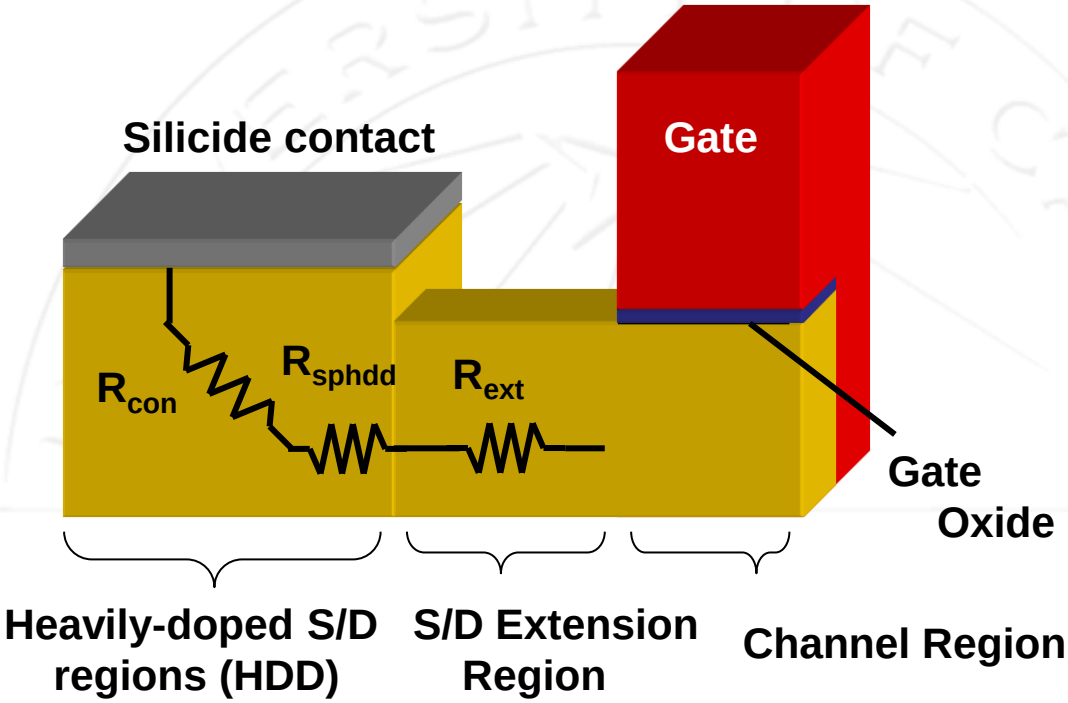
Unified Framework for FinFET Parasitic Resistances and Capacitances



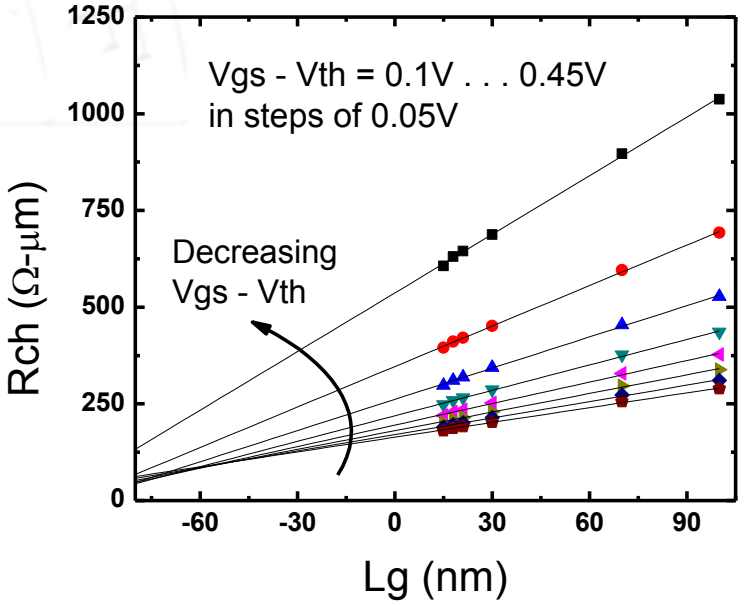


- In sub-45nm tech.
  - Parasitic Resistance – significant portion of RON
  - Total Parasitic Caps ~ Intrinsic Gate Capacitance
- Geometrically scalable parasitic resistance and capacitance model present in BSIM-CMG

FinFET R_{ds} Modeling



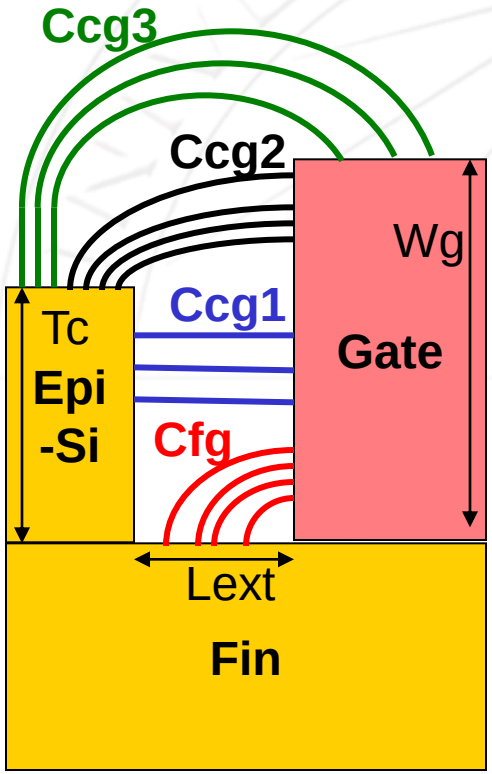
- Contact Resistance
- Spreading Resistance
- Extension Resistance

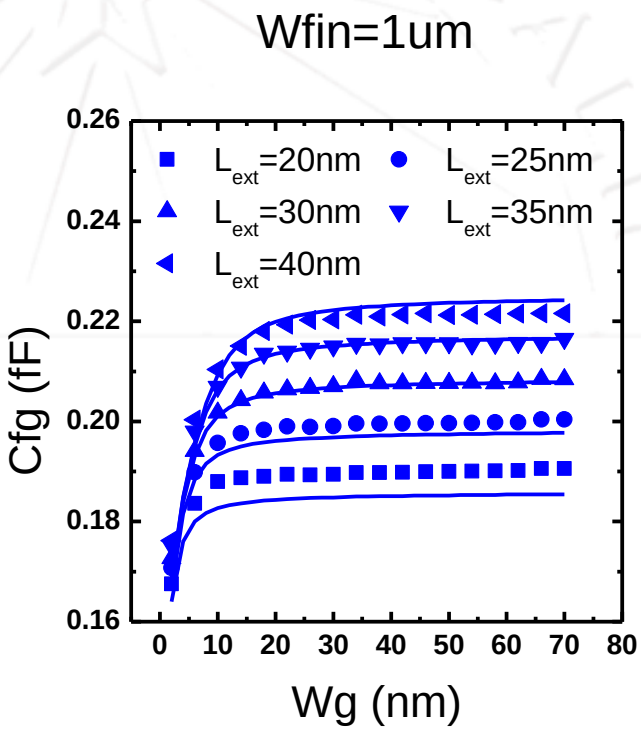


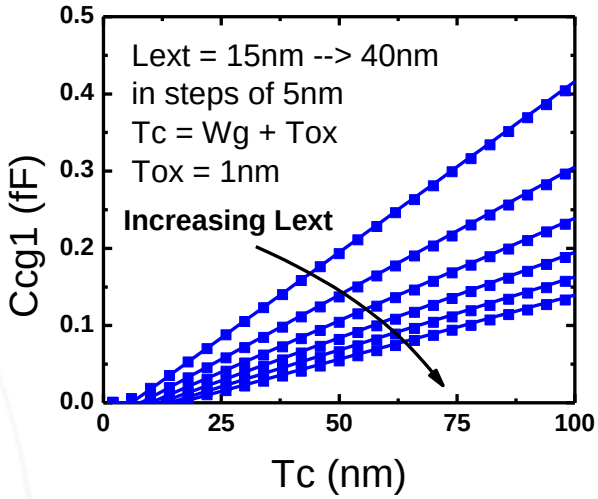
Darsen Lu, PhD Dissertation, UC Berkeley

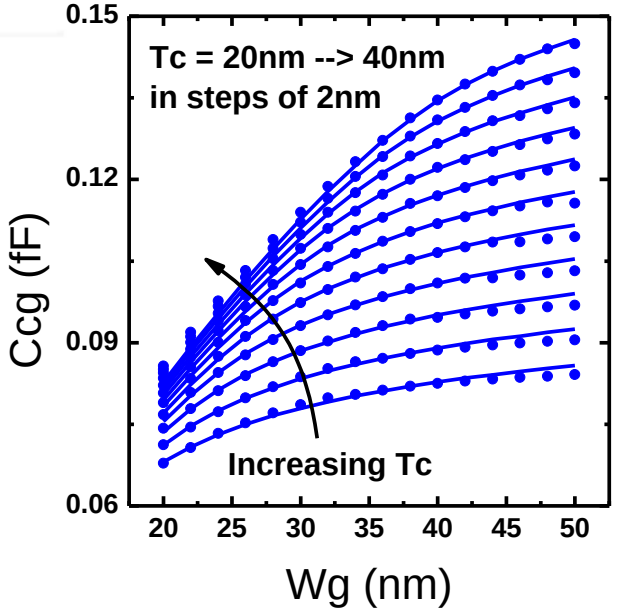
FinFET C_{fr} Modeling – TCAD Verification

- C_{fg}: fin ➔ gate
- $C_{cg}=C_{cg1}+C_{cg2}+C_{cg3}$: contact ➔ gate



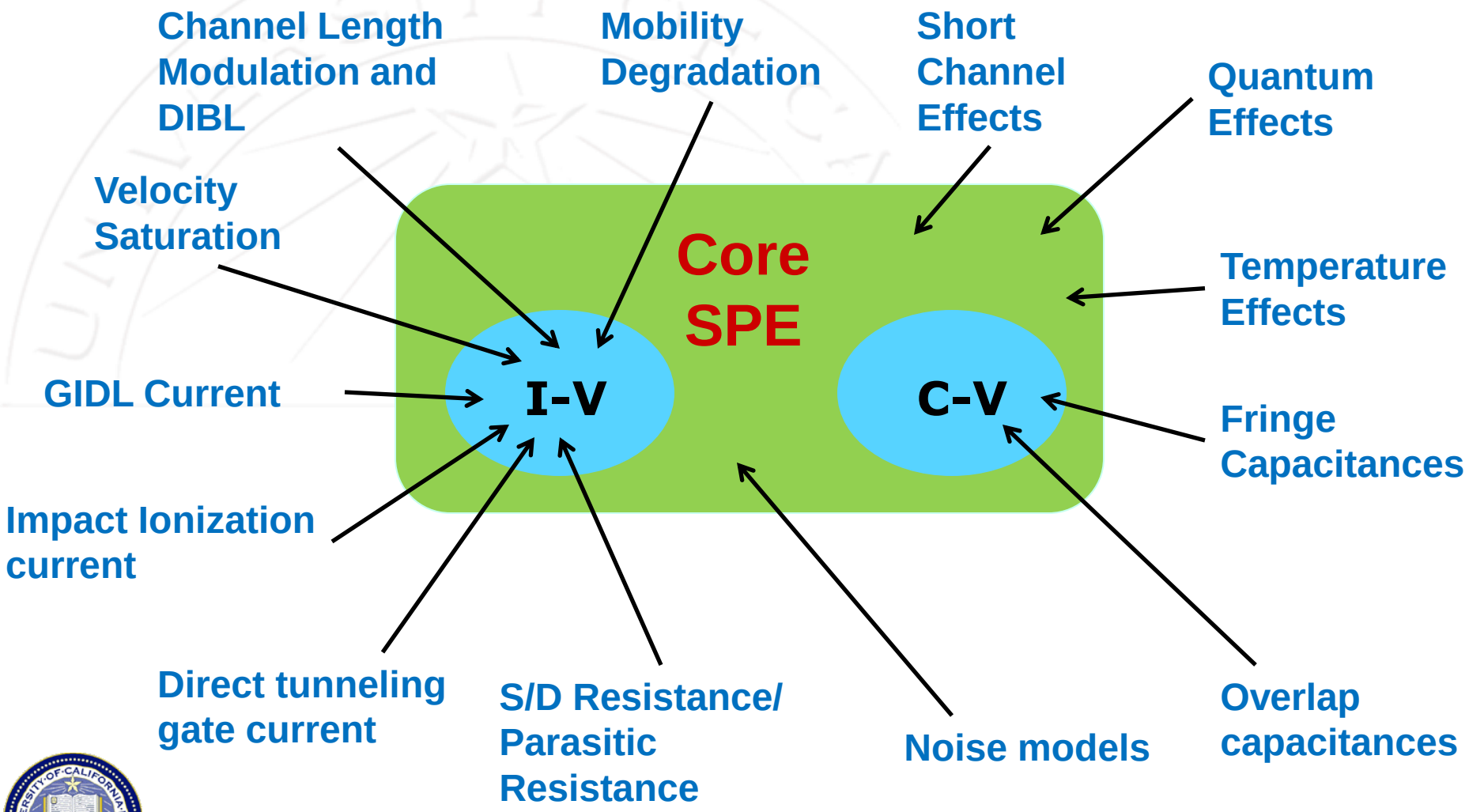






- Both C_{fg} and C_{cg} agree well with 2D numerical simulations

Real Device Effects



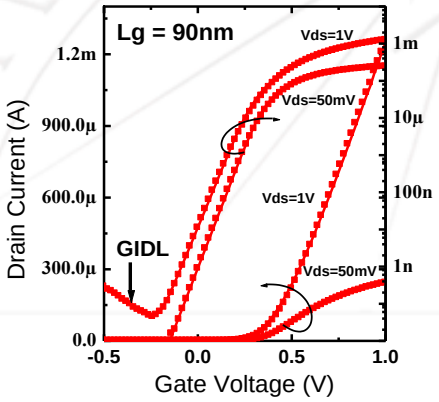
BSIM-CMG

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- **Model Validation & QA**
- Conclusion

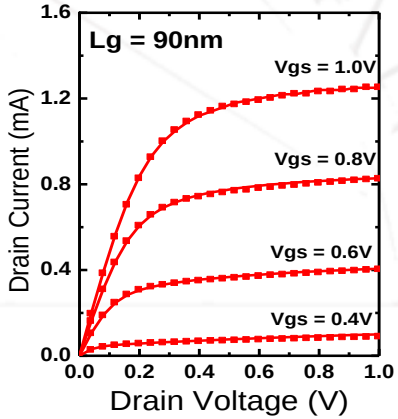
SOI FinFET Fitting

- SOI FinFETs are fabricated at TI
- TFIN=22nm, HFIN=60nm, T_{OX}=2nm

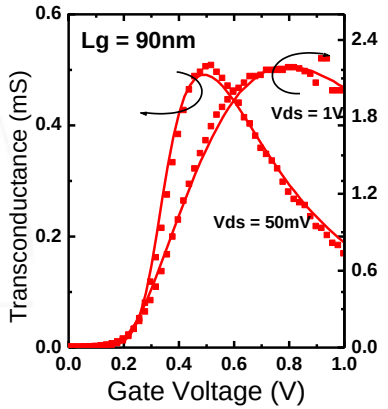
Drain Current v.s Vgs (Lg = 90nm)



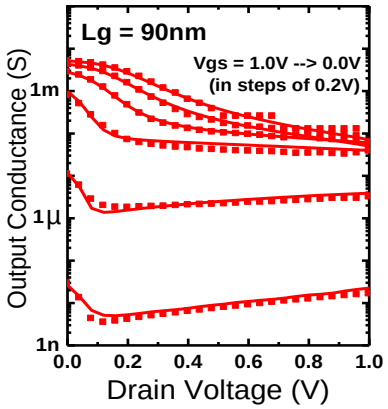
Drain Current v.s. Vds (Lg = 90 nm)



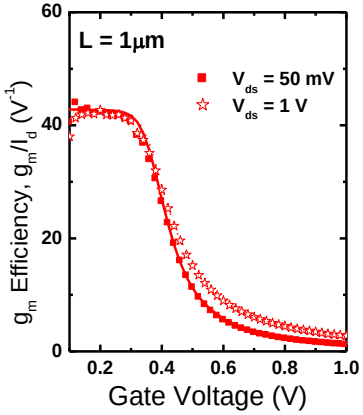
Transconductance (Lg = 90nm)



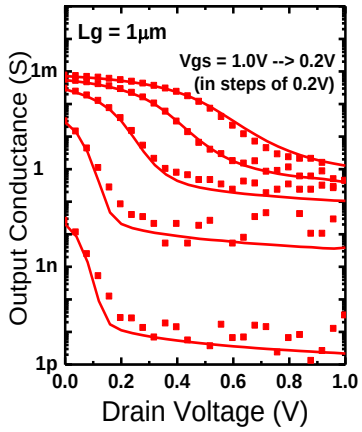
Output Conductance (Lg = 90 nm)



G_m / I_{ds} (Lg = 1 µm)



Output Conductance (Lg = 1 µm)



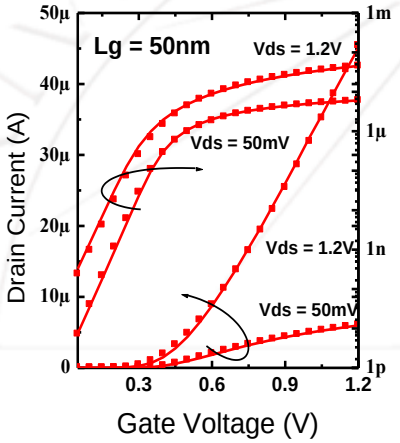
Symbols: Data
Lines: Model

Bulk FinFET Fitting

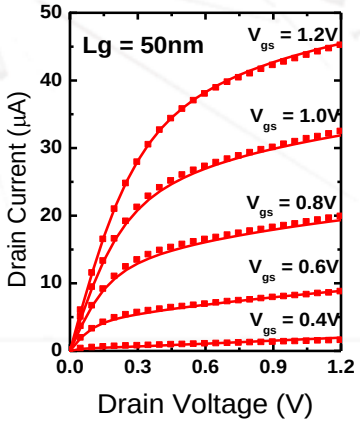
- Bulk FinFETs are fabricated by TSMC
- TFIN=25nm, HFIN=27.5nm, EOT=2.42nm

Symbols: Data
Lines: Model

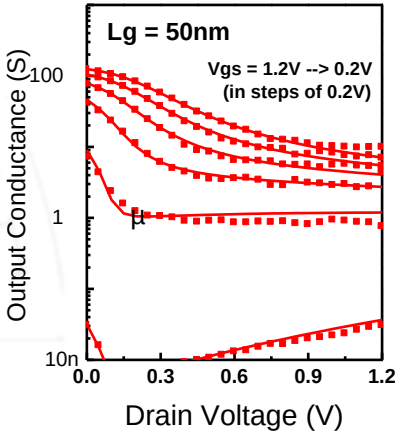
Drain Current vs. V_{gs} (Lg = 50nm)



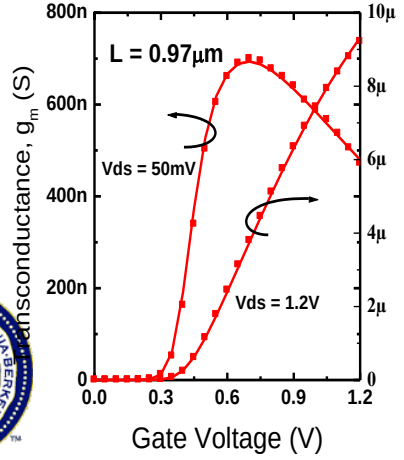
Drain Current vs. V_{ds} (Lg = 50 nm)



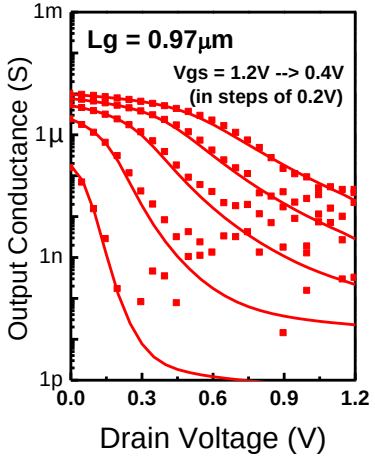
Output Conductance (Lg = 50nm)



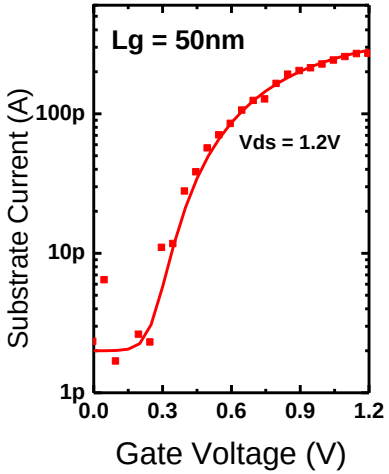
Transconductance (Lg = 0.97μm)



Output Conductance (Lg = 0.97 μm)



Substrate Current (Lg = 50nm)

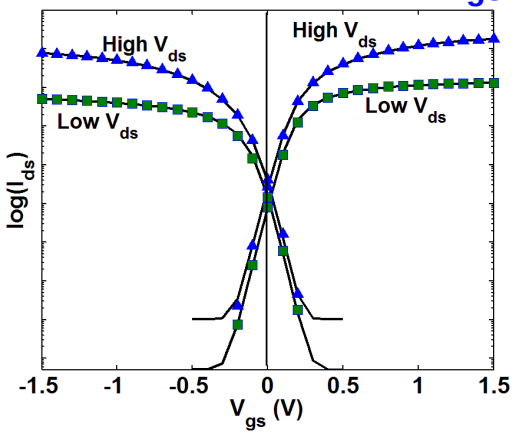


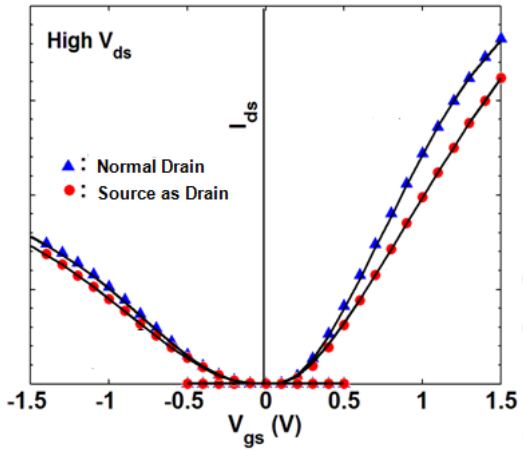
Vertical GAAFET Overlay

- Lg=120nm, D=80nm, Tox=3nm

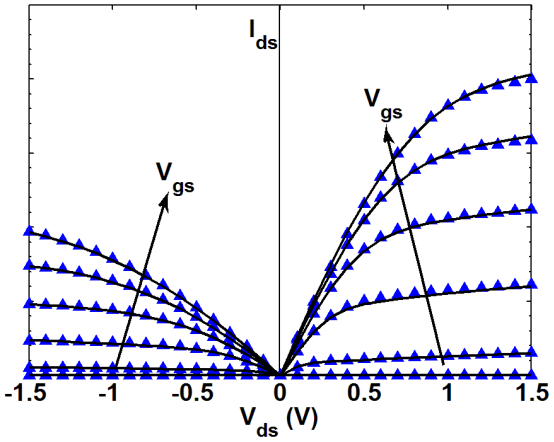
Symbols: Data
Lines: Model

Drain Current vs. V_{gs}

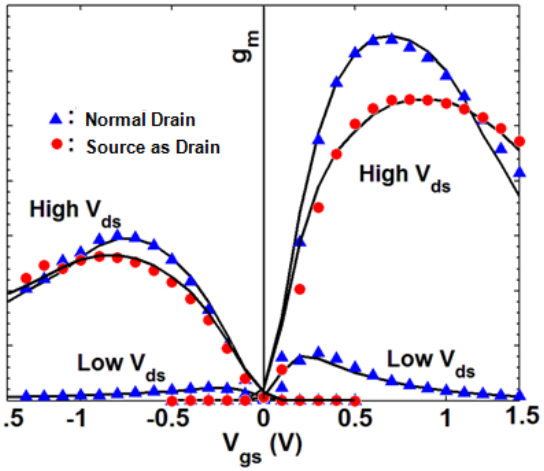




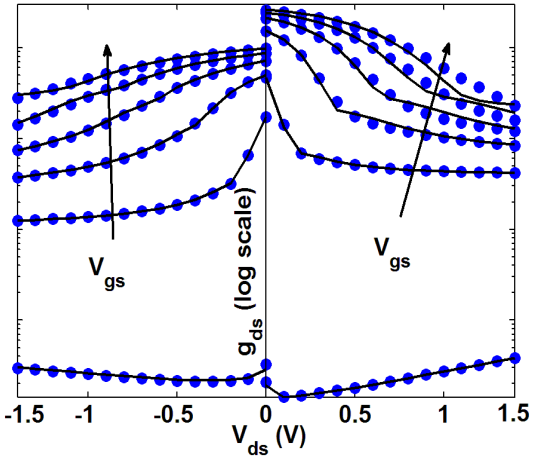
Drain Current vs. V_{ds}



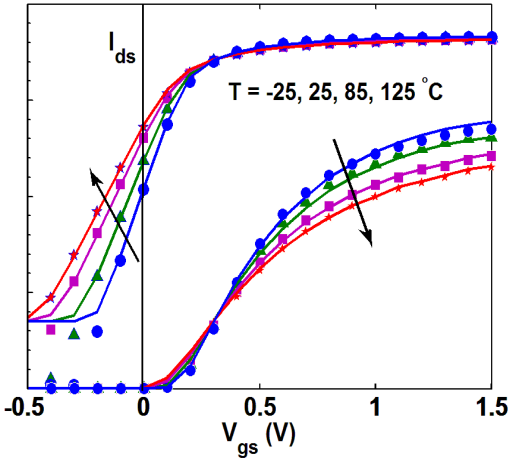
Transconductance



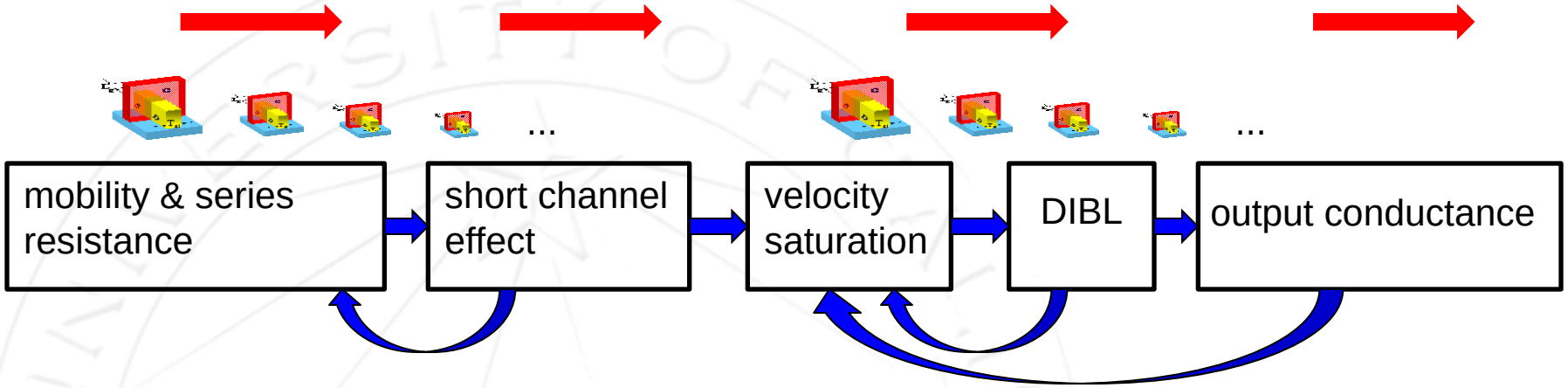
Output Conductance



Temperature Dependence

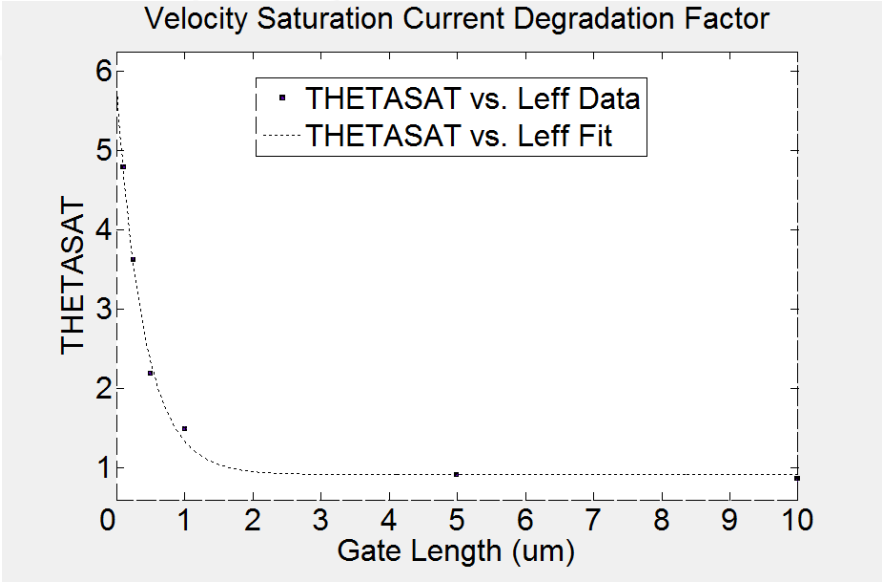


Global Extraction Procedure



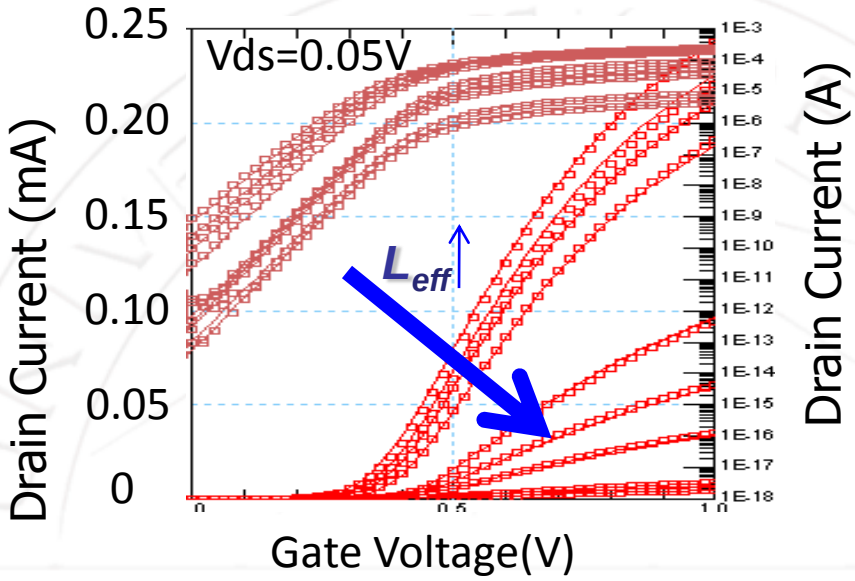
e.g.

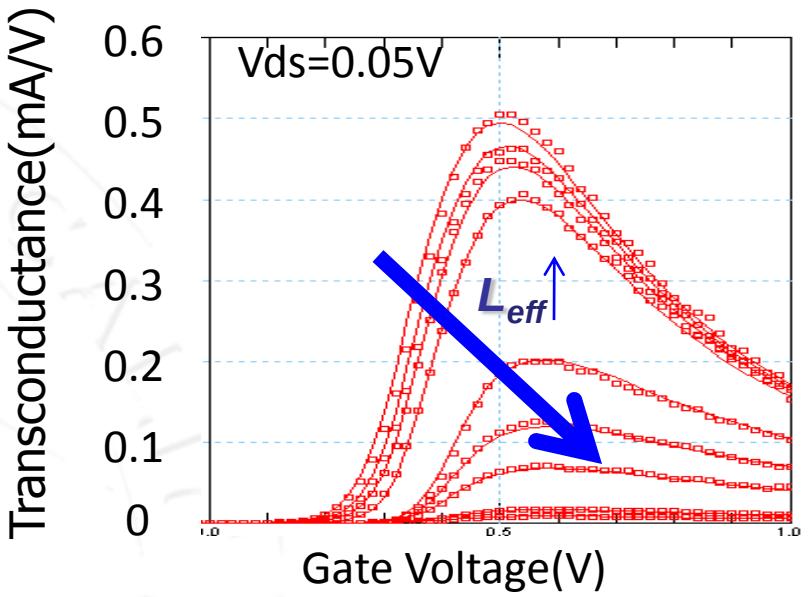
$\theta SAT[L] = \theta SAT_0 \times (1 + C\theta SAT \times \exp(-L_{eff} / D\theta SAT))$

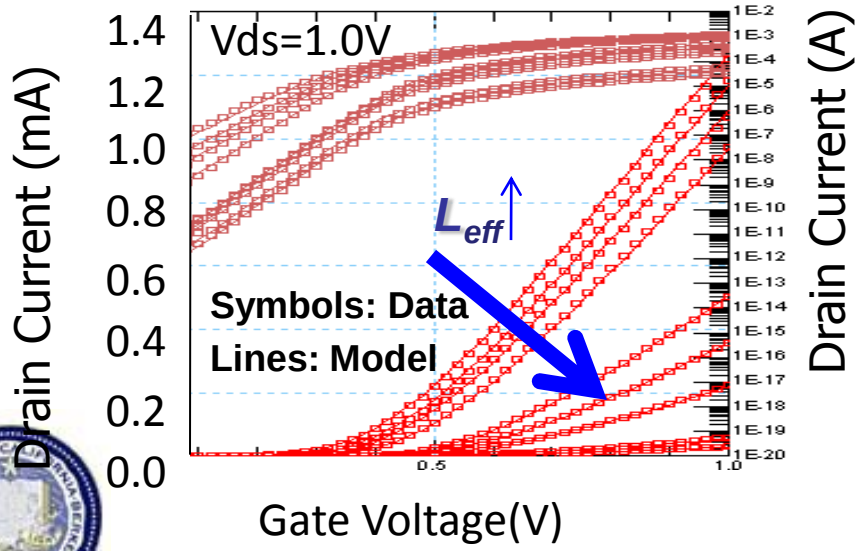


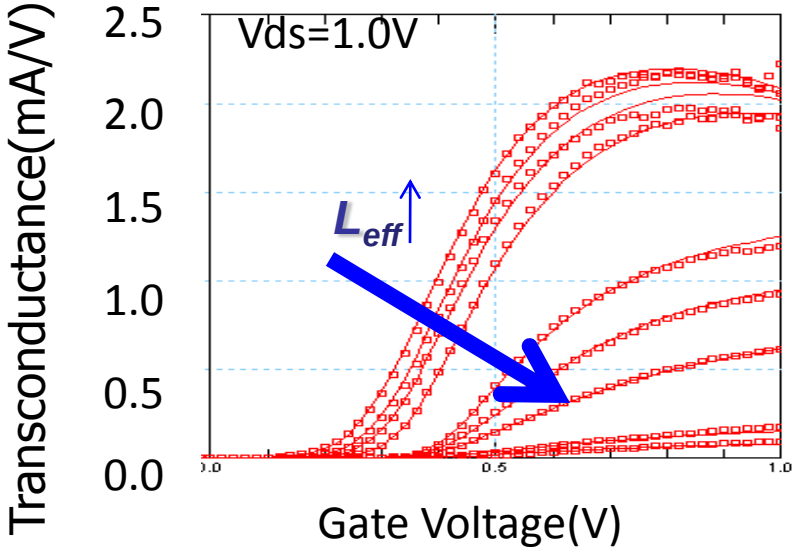
Shijing Yao et al., ICMTS 2010

NMOS L_{eff} from 30nm to 10um

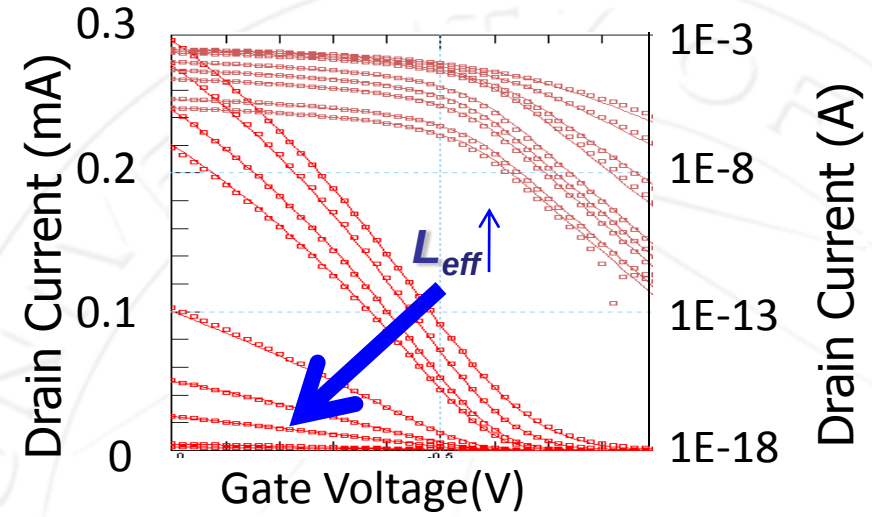


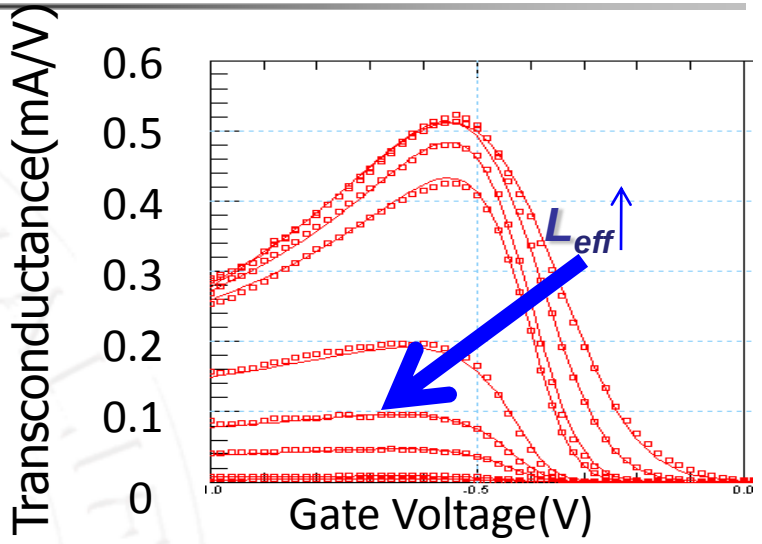


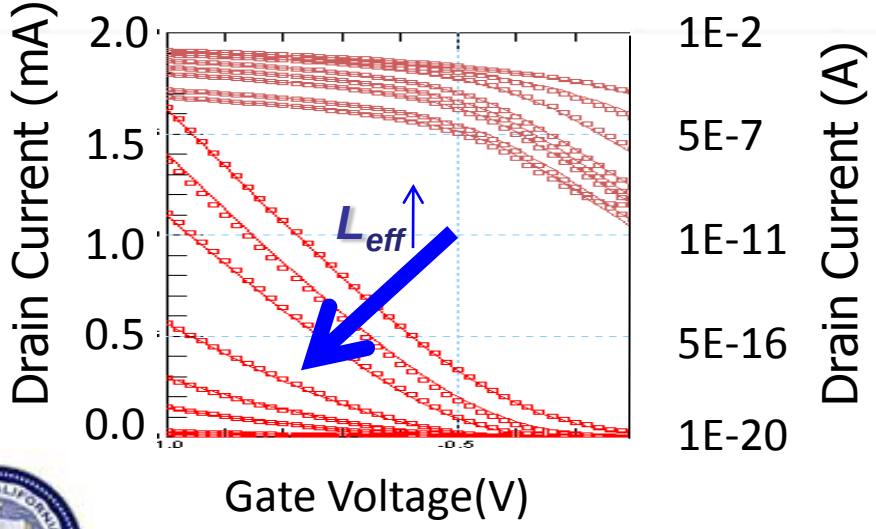


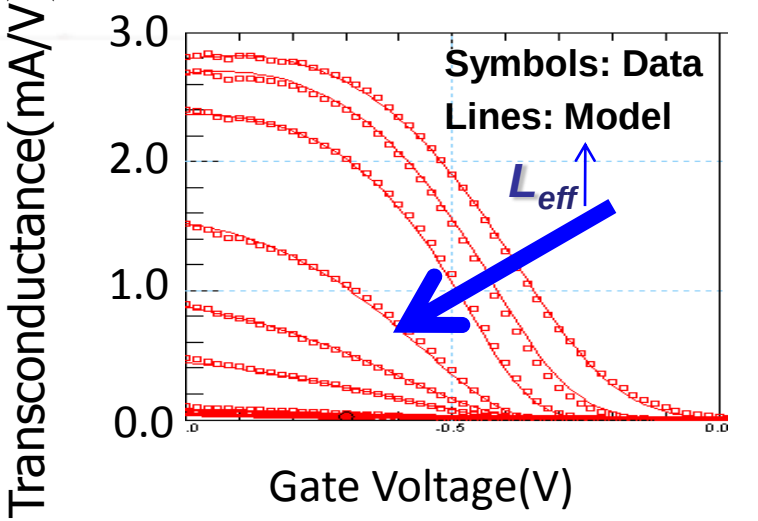


PMOS L_{eff} from 35nm to 10um

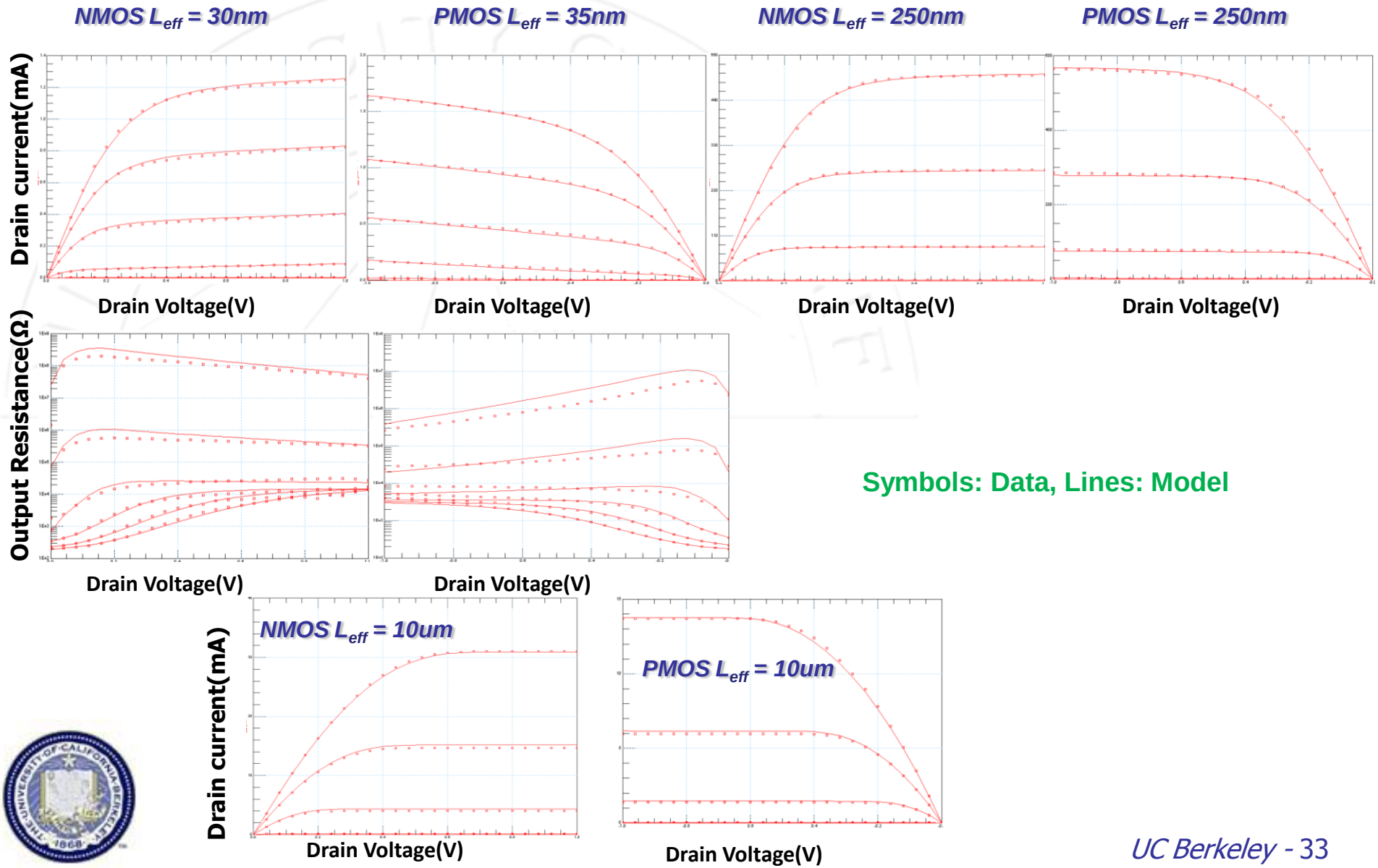






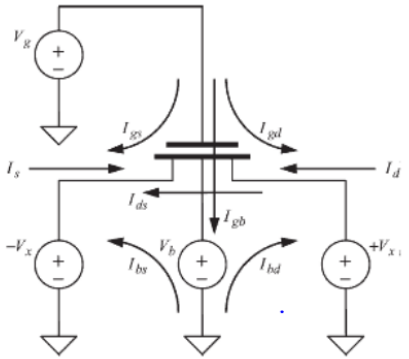


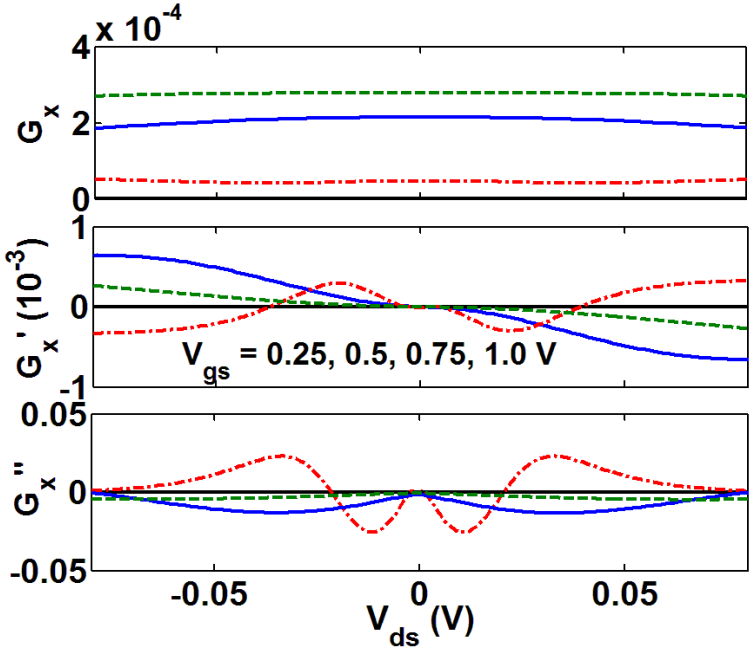
Short Channel Output Characteristics

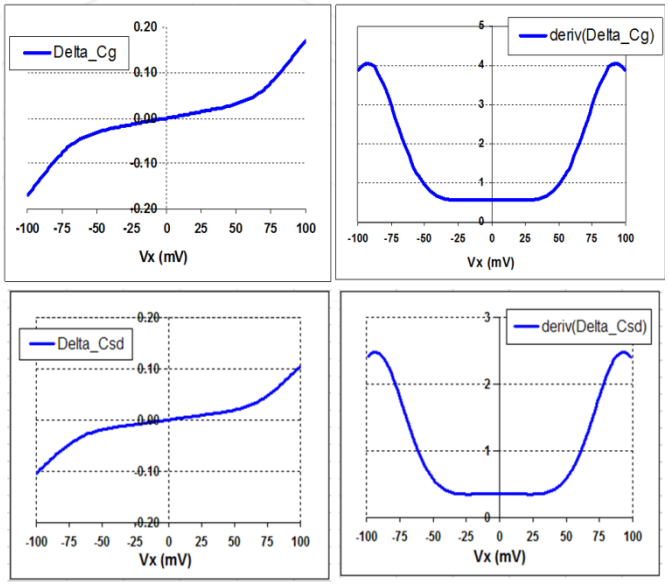


Symmetry / Continuity Tests

- Model passes both DC and AC Symmetry Tests







Drain Current

Capacitances (C_{gg} and C_{sd})

C.C.McAndrew, IEEE TED, Vol. 53, No. 9, 2006

Speed Tests

Circuit	# MOSFETs	Model	Runtime per iteration per transistor (normalized)
1-Transistor Id-Vds	1	BSIM4 BSIM-CMG	1.00 1.22
17-Stage Ring	34	BSIM4 BSIM-CMG	1.00 1.31
Coupled Rings	2020	BSIM4 BSIM-CMG	1.00 1.24

- Speed of BSIM-CMG v105 and BSIM v4.5 compared
  - Both model compiled with the in-built Verilog-A compiler of HSpice
  - Note: Each model uses its own default parameter. Parameters are not extracted for a real technology.

Averaged over multiple runs on the same machine

BSIM-CMG

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Model Validation & QA
- **Conclusion**

Roadmap of BSIM-CMG

- BSIM-CMG100.0 was released in October 2006
- BSIM-CMG105.03 is under balloting stage at the Compact Model Council for standardization
  - Verilog-A and a well documented manual
  - Available in major commercial simulators
- BSIM-CMG105.04 was released Dec 2011

Summary

- BSIM-CMG is a Turnkey , Production Ready model
  - Final Phase of Standardization at the CMC
- Physical, Scalable Core Models for multiple device architectures
  - Supports both SOI and Bulk Substrates
- Many Real Device Effects captured
- Validated on Hardware Data from different technologies
- Available in major EDA tools

Acknowledgement

SRC, Industry Supporters, EDA Vendors