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Analog modeling requirements for HV CMOS technology

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Presentation Overview

- Design perspective on High Performance Analog
- HV CMOS Analog modeling requirements
- HV Transistor compact modeling
- Aging modeling
- 1/f noise modeling
- Process Variability

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Design Perspective on Analog Modeling

Analog Application	Critical feature	Critical Modeling Parameter
Pre-Amplifier for ADC Reference circuit	Signal to noise ratio, effective number of Bits	Transistor and resistor noise
ADC/DAC	Linearity,Distortion	Resistor Mismatch
Operational Amplifier Current Mirror Multi-channel devices	Voltage matching Current matching Gain matching	Analog parameter (gds, gm, Vt etc.) mismatch
Voltage Reference (e.g. Bandgap) Current Reference	Voltage stability Current stability	Bipolar parasitics (gain, linearity etc.)

Design Perspective on Analog Modeling

Analog Application	Critical feature	Critical Modeling Parameter
Capacitor switching design Transmission gates IC/RC Oscillator High impedance signal source	parasitic voltage divider Charge Injection frequency stability capacitive coupling	Parasitic capacitance
Current source Operational Amplifier	Output resistance Gain	Small signal parameters (gds, gm etc.)
Operational Amplifier Voltage Reference	Offset & Gain shift Output voltage shift	2nd order parameters (linearity and temperature)

HV TRANSISTOR MODELING

FOMs for HV Transistors

- RON (On Resistor) (high vgs, low vds, and temp.)
- IDSAT (Saturation Current) ?
- VT long & short
- Cgg & Cgd Miller Cap ?
- Analog parameter for long channel length (gds, gm)
- RF Parameter FT, FMAX ?
- 1/f noise.

State of the Art HV Compact Models and new Developments

EKV HV Transistor

– Under development within the EU Project COMON

"A Physics-Based Analytical Compact Model for the Drift Region of the HV-MOSFET" Antonios Bazigos, François Krummenacher, Jean-Michel Sallese, Matthias Bucher, Ehrenfried Seebacher, Werner Posch, Kund Molnár, and Mingchun Tang

HiSIM_HV

– CMC Standard model version 1.1.2 ;1.2.1; 2.0

PSP HV – Transistor Model

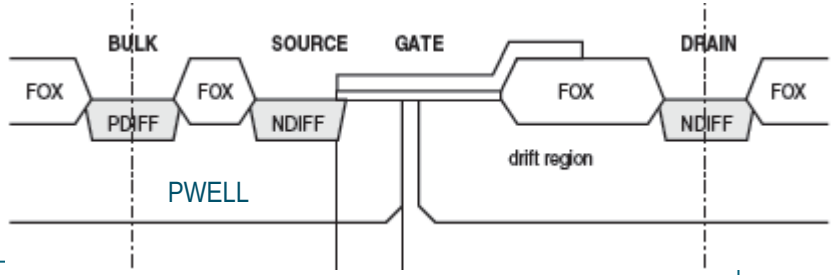
– In development based on PSP surface potential model

MM20

– asymmetrical, surface-potential-based LDMOS model, developed by NXP Research

BSIMx Sub-circuit Model

HV CMOS Transistor Types

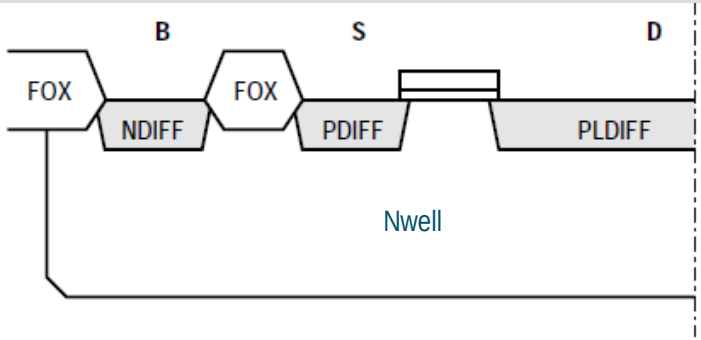


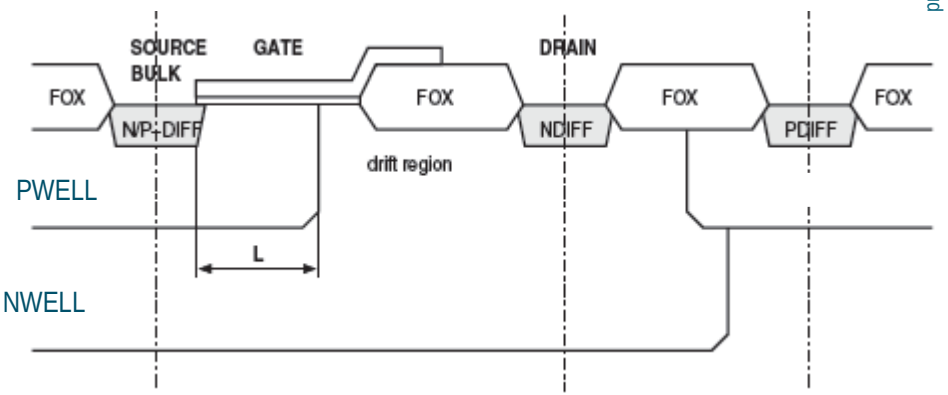
Increased junction breakdown voltage (BV) of the drain diffusion is achieved by using a deep drain well

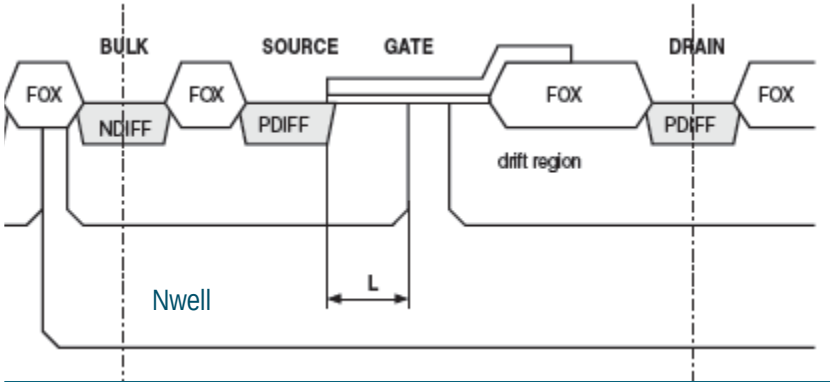
Small on-resistance and high BV are contrary effects. The optimization of the tradeoff between both quantities is of major interest.

The gate length is extended beyond the body-drain well junction, which increases the junction BV. The gate acts as a field plate to bends the electric field. RESURFeffect

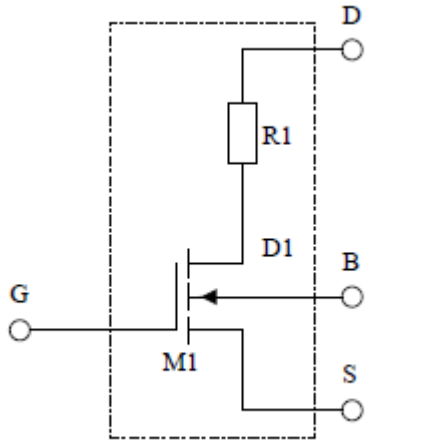
Quasisaturation Effect.



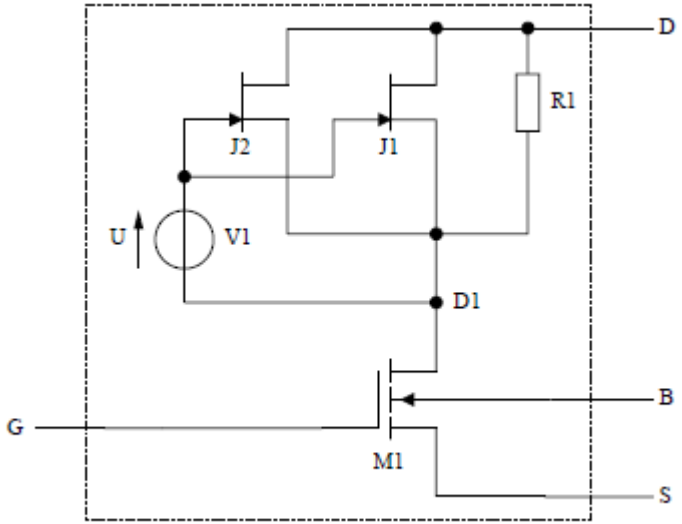




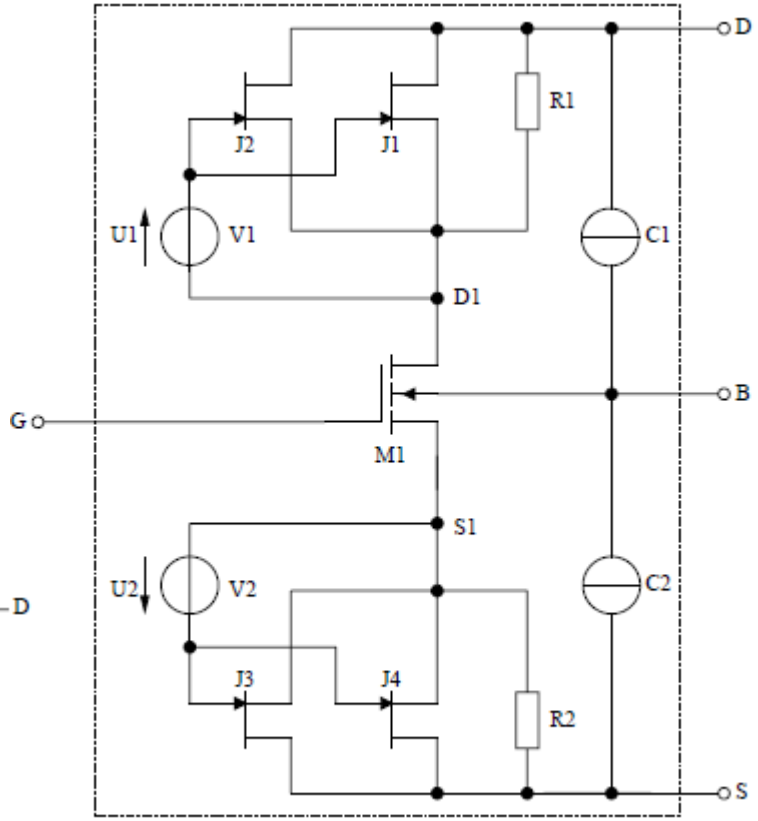
Sub-circuit Modeling



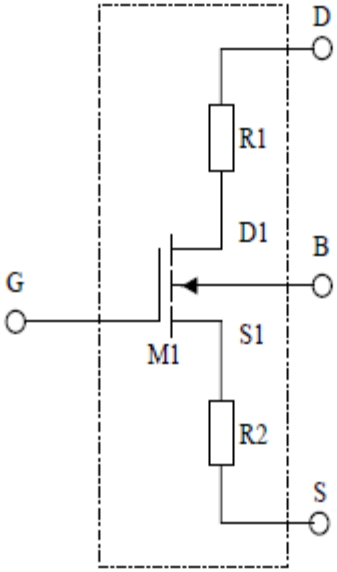
Unsymmetrical HV transistor sub-circuit



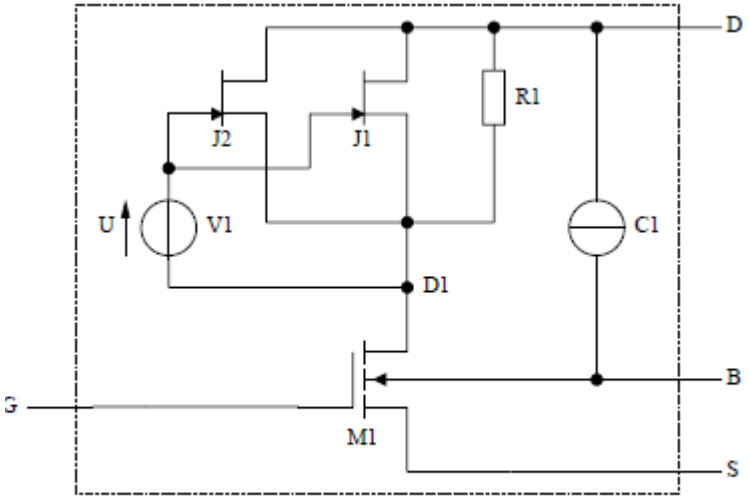
: Unsymmetrical HV transistor sub-circuit



: Symmetrical HV transistor sub-circuit



Symmetrical HV transistor sub-circuit



: Unsymmetrical HV transistor sub-circuit

HiSIM_HV

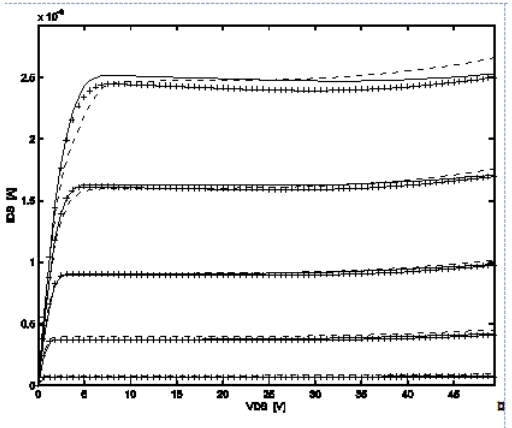
Complete Surface potential-based:
HiSIM_HV solves the Poisson equation along the MOSFET channel iteratively,
including the resistance effect in the drift region.

high flexibility
20 model flags
scales with the gate width,
the gate length,
the number of gate fingers
and the drift region length.
In addition, HiSIM_HV is capable of modeling
symmetric and asymmetric HV devices.

The following effects are also included:

- Depletion effect of the gate polycrystalline silicon (poly-Si).
- Quantum mechanical
- CLM
- Narrow channel
- STI
- Leakage currents (gate, substrate and gate-induced drain leakage (GIDL) currents).
- Source/bulk and drain/bulk diode models.
- Noise models (1/f, thermal noise, induced gate noise).
- Non-quasi static (NQS) model.

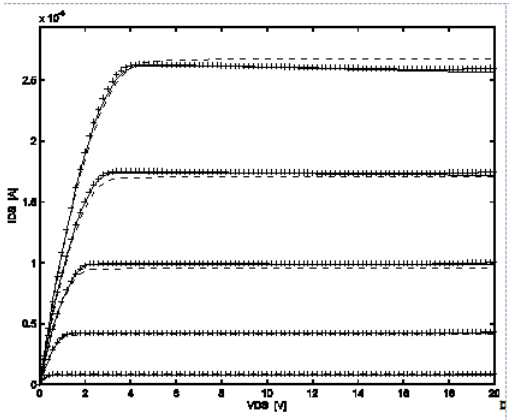
Model Benchmark Output Characteristic



output characteristic of a typical wafer. W/L = 40/10

VGS = -1.5, -2.5, -3.5, -4.5, -5.5V V, VBS = 0 V

→ + = measured, — = HiSIM_HV model, --- = BSIM3v3 sub-circuit



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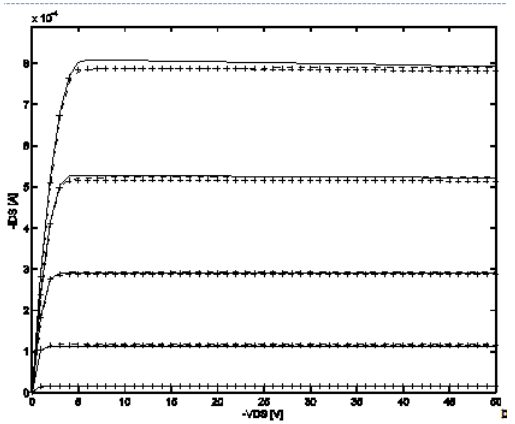
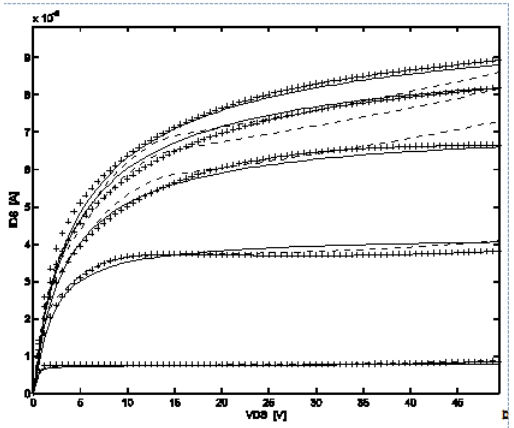


transfer characteristic of a typical wafer. W/L = 40/10,

VGS = -1.5, -2.5, -3.5, -4.5, -5.5V, VBS = 0 V

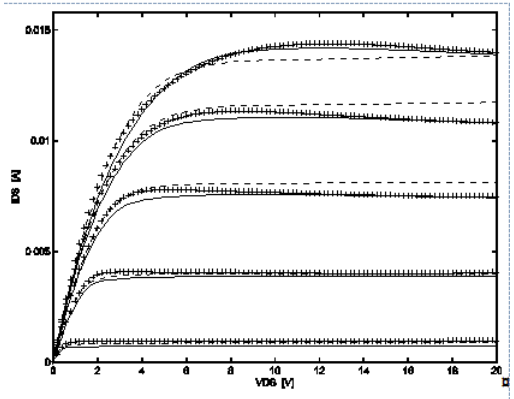
→ + = measured, — = HiSIM_HV model, --- = BSIM3v3 sub-circuit



output characteristic of a typical wafer. W/L = 40/0.5

VGS = -1.5, -2.5, -3.5, -4.5, -5.5V V, VBS = 0 V

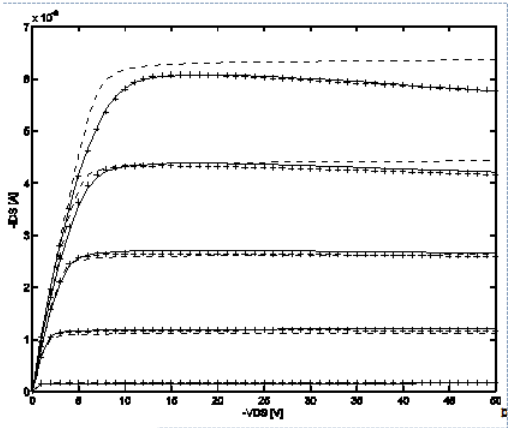
→ + = measured, — = HiSIM_HV model, --- = BSIM3v3 sub-circuit



output characteristic of a typical wafer. W/L = 40/0.5

VGS = -1.5, -2.5, -3.5, -4.5, -5.5V V, VBS = 0 V

→ + = measured, — = HiSIM_HV model, --- = BSIM3v3 sub-circuit



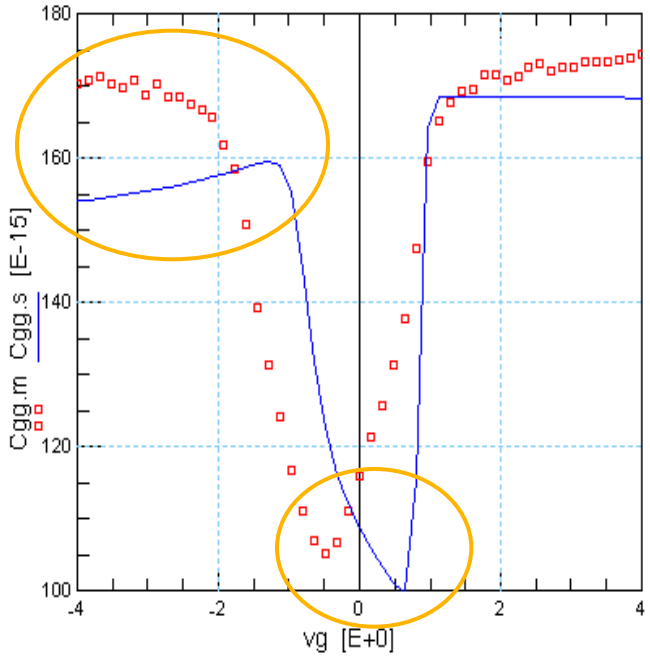
transfer characteristic of a typical wafer. W/L = 40/1.0,

VGS = -1.5, -2.5, -3.5, -4.5, -5.5V, VBS = 0 V

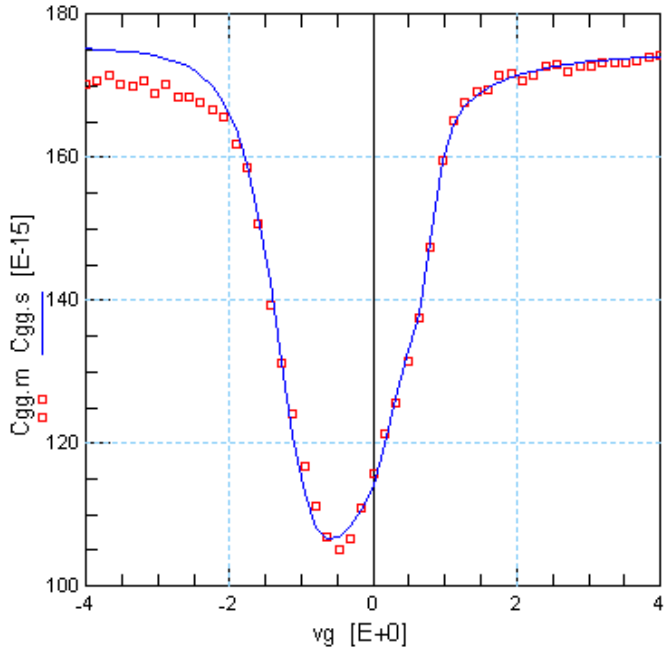
→ + = measured, — = HiSIM_HV model, --- = BSIM3v3 sub-circuit

AC Modeling: Cgg

BSIM3+JFETS Subckt.

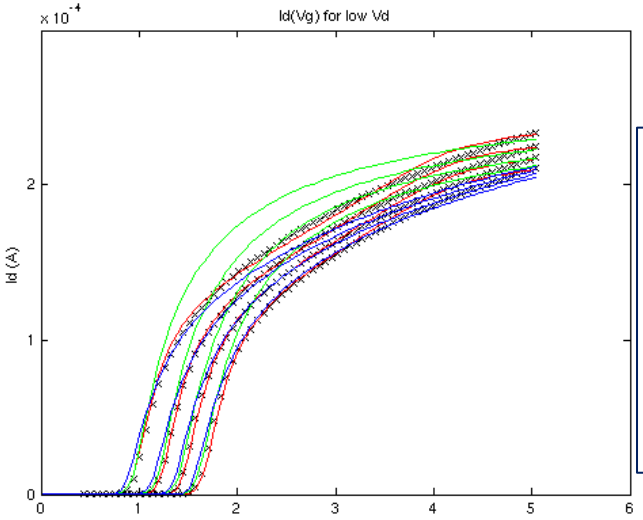


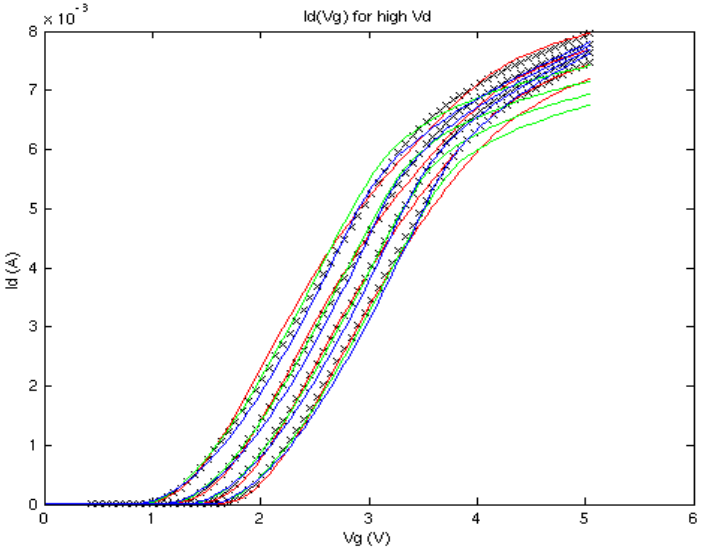
HiSIM_HV



- Subcircuit: bad fitting quality, especially in accumulation.
- HiSIM_HV: good fitting quality in all regions.

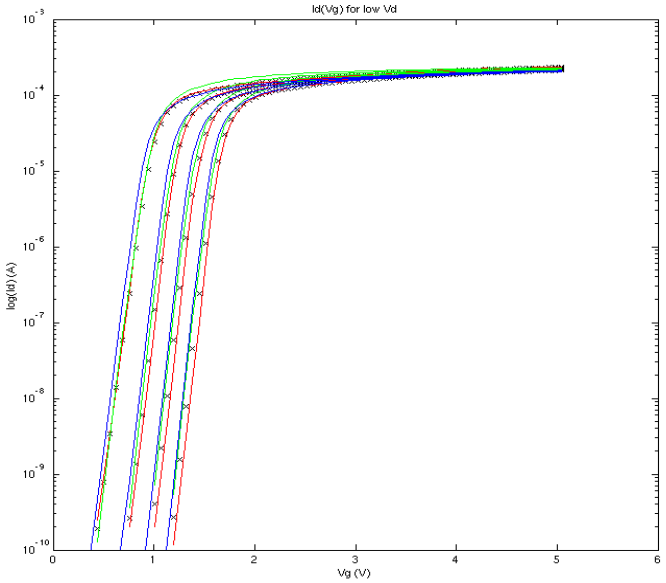
Short Device: Transfer Characteristics at low and high Vds

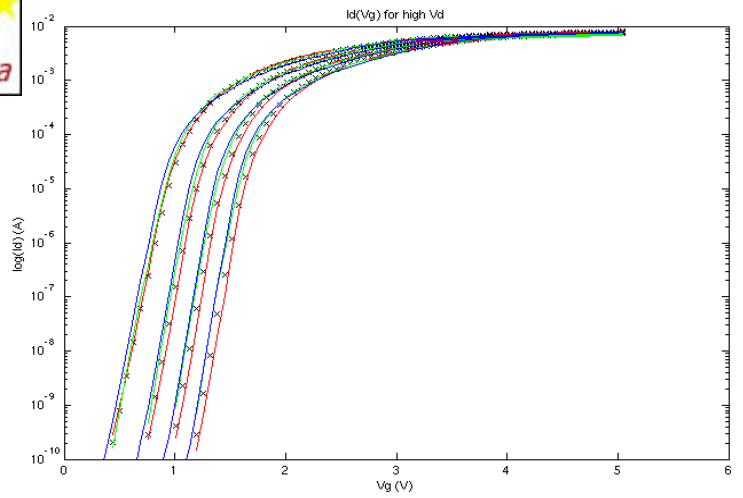




x:	Meas.
Blue:	EPFL_HV
Green:	BSIM sub-circuit
Red:	HISIM_HV

CoMoN Compact Modelling Network beta





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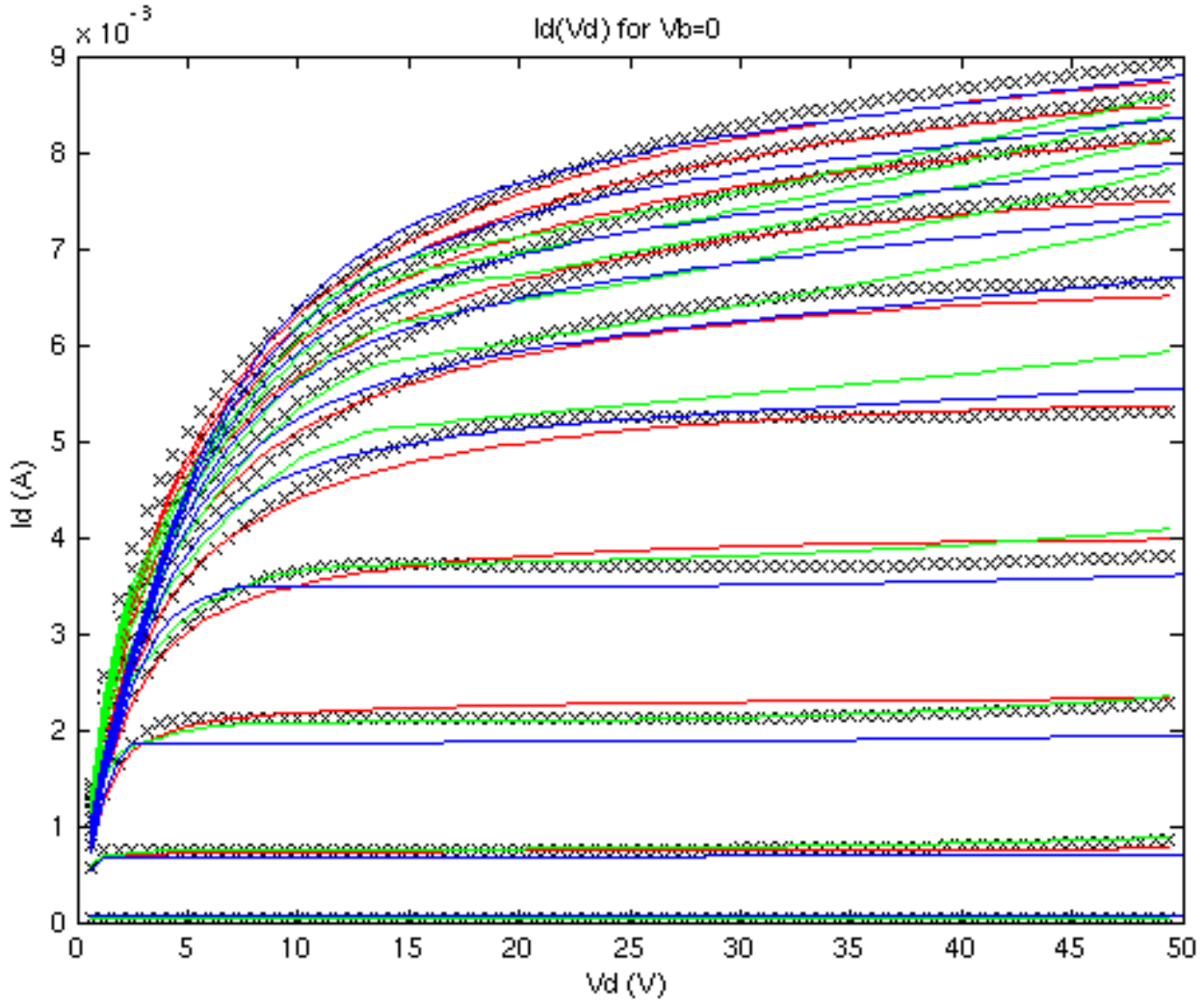
Short Device: Output Characteristics



CoMoN Compact Modelling Network beta

x:	Measurement
Blue:	EPFL_HV
Green:	BSIM sub-circuit
Red:	HISIM_HV

Table of Model Capabilities (1/3)

Physical Effects	BSIM3/JFET Subcircuit	HiSIM_HV	EPFL-HV
Technology Related Device Effects:			
Symmetric / Asymmetric Device	☑	☑	asymmetric only
Quasi-Saturation	☑	☑	☑
RON	☑	☑	☑
Mobility	☑	☑	☑
Carrier Velocity Saturation	☑	☑	☑
Channel Length Modulation	☑	☑	☑
Impact Ionization current	extrinsic model	☑	☑
Poly-Silicon-Gate Depletion Effects	☑	☑	☒
Geometry Scaling:			
Short Channel Effects	☑	☑	☑
Reverse Short Channel Effects	☑	☑	☑
Narrow Channel Effects	☑	☑	☑
Drain Induced Barrier Lowering	☑	☑	☑

Table of Model Capabilities (2/3)

Physical Effects	BSIM3/JFET Subcircuit	HiSIM_HV	EPFL-HV
Asymetric MOS Capacitances:			
Intrinsic Capacitance	☑	☑	☑
Overlap Capacitance	☑	☑	☑
Fringing Capacitance	☑	☑	☒
Bulk Diodes:			
Diode Current	☑	☑	☑
Diode Capacitance	☑	☑	☑
Temperature Modelling:			
Threshold Voltage	☑	☑	☑
Mobility	☑	☑	☑
Quasi-Saturation	☑	☑	☑
RON	☑	☑	☑
Bulk Current	☑	☑	☑
Self-Heating	☒	☑	☑

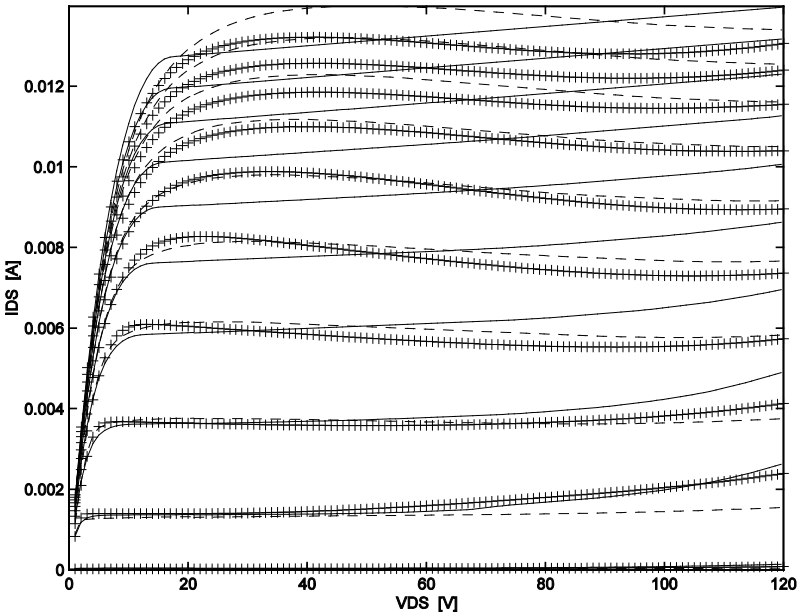
Table of Model Capabilities (3/3)

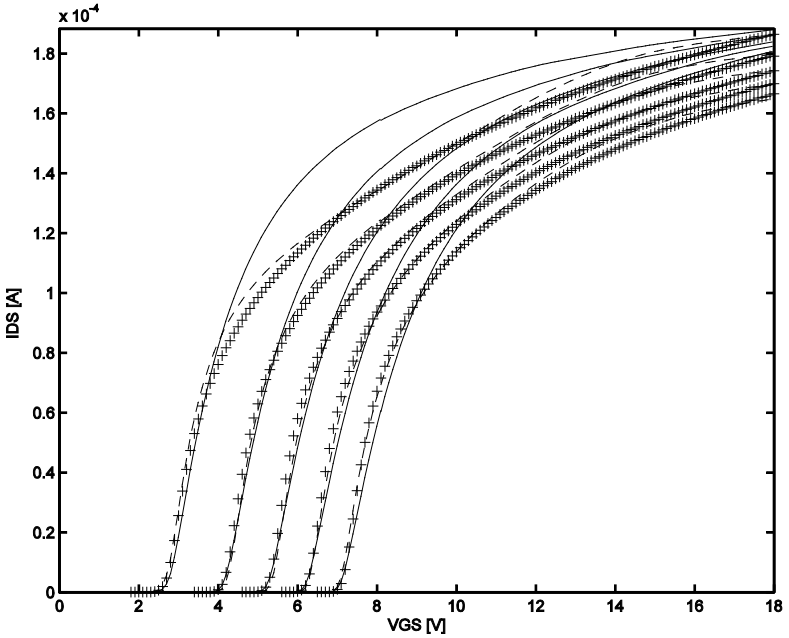
Physical Effects	BSIM3/JFET Subcircuit	HiSIM_HV	EPFL-HV
Noise:			
SPICE Noise model	☑	☒	☒
Flicker Noise Model	☑	☑	☒
Short Channel Thermal Noise Model	☒	☑	☒
Induced Noise in Gate	☒	☑	☒
Induced Noise in Substrate	☒	☑	☒
RF Modeling:			
Gate resistance model	☒	☑	☑
Substrate resistance model	☒	☑	☑
Multi-finger transistors	☒	☑	☑
Non-Quasi-Static (NQS):			
NQS	☑	☑	☒

Modeling of parasitic diodes and bipolar in HV transistors

PARASITIC MODELING

Benchmarking HiSIM_HV 1.2.1 for 120V Transistors





HV NMOS output and transfer characteristic of a typical wafer. W/L=40/0.5,

VGS= 2.9, 4.8, 6.7, 8.6, 10.5, 12.4, 14.3, 16.2, 18.1, 20 V, VBS=0 V. &

VBS= 0, -1, -2, -3, -4 V, VDS=0.1 V.

+ = measured, full lines= BSIM3v3 model; dashed lines = HiSIM_HV 1.2.1

Isolated HVMOS: High-Side Switch Modeling

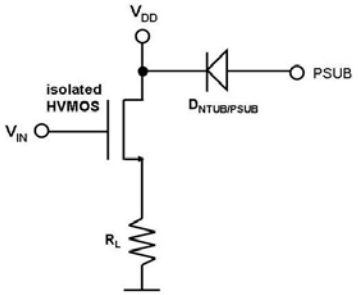
- HVMOS used on the low-side of a load:

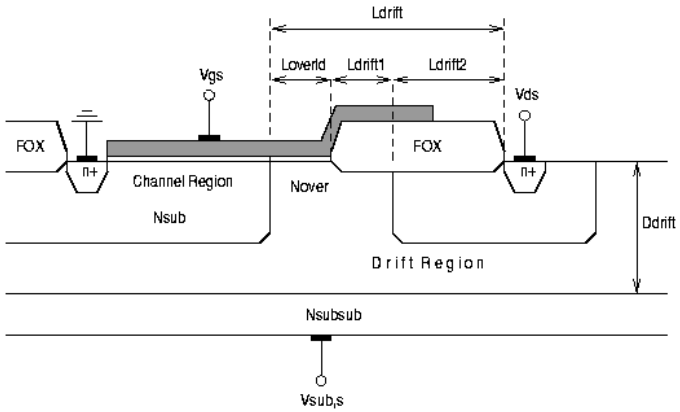
Source and Substrate hold at the same potential

- HVMOS used on the high-side of a load:

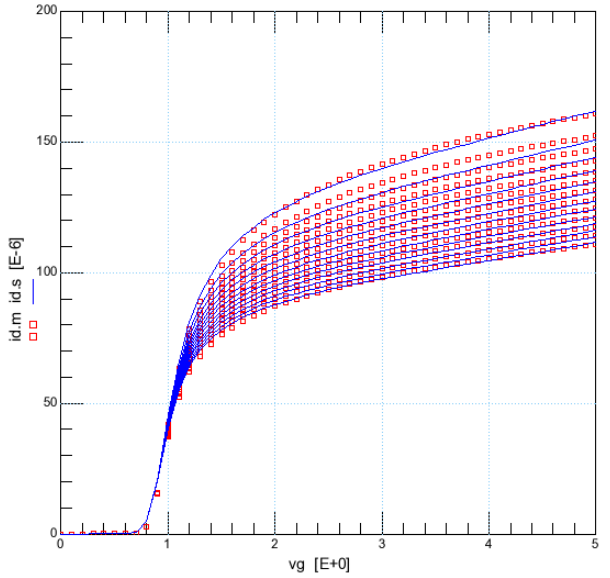
Both Source and Drain can be placed at high potentia

=> Ron is changing with V_{sub-s}





Transfer Characteristics



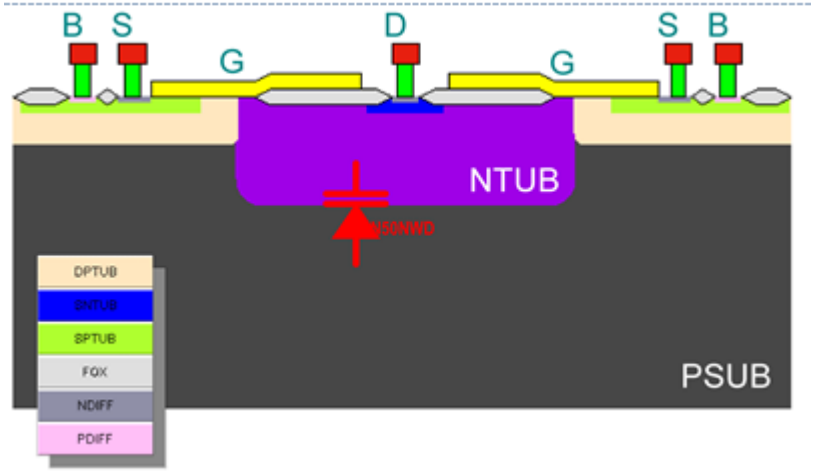
Vsub=0

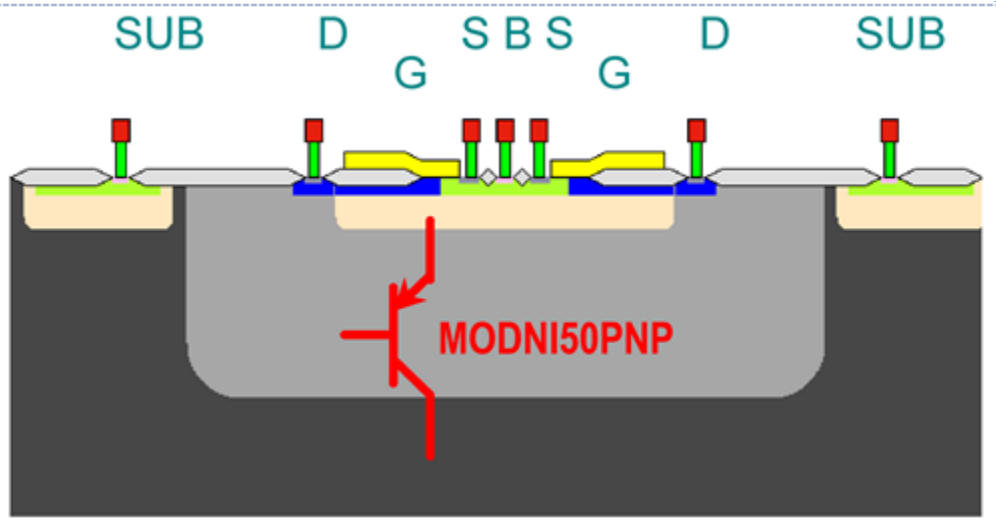
Vsub=-120V

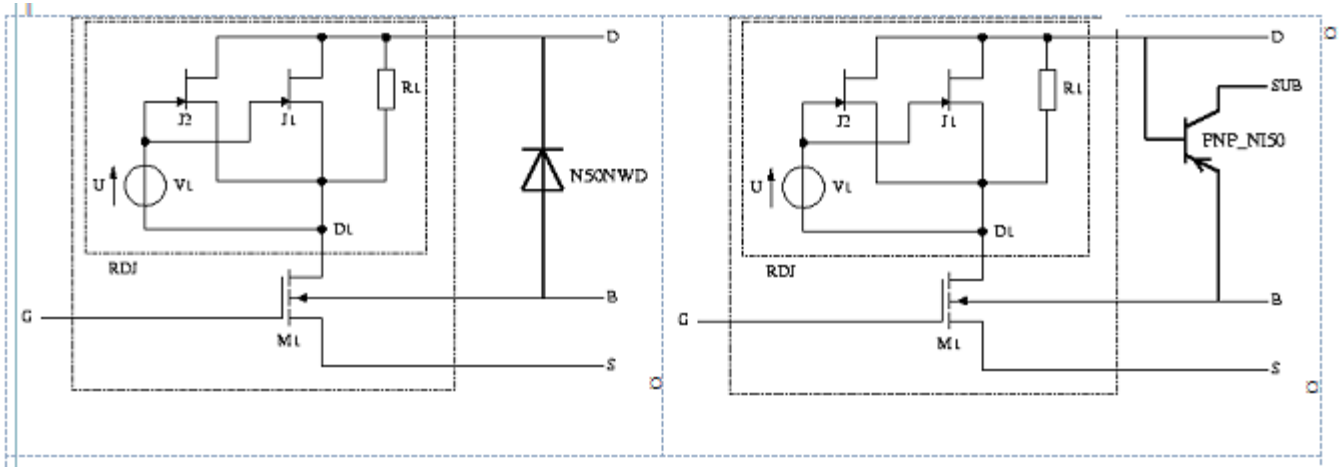
Vd=0.1V, Vs=Vb=0

HiSIM_HV 1.2.1: Vsub modulates the effective depth of the drift region: Rdrift($V_{sub,s}$)

HV Transistor Parasitic Modeling



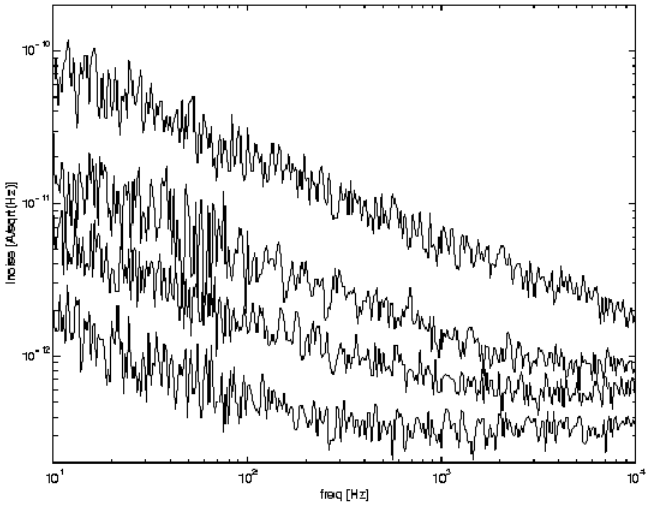




Analog design requirement

1/F NOISE MODELING

1/f Noise Modeling for HV Transistors



Mobility fluctuations as well as charge carrier fluctuations

HiSIM_HV:

NFALP which is applied for the mobility fluctuation phenomenon

NFTRP which is applied for the ratio of **trapped density** to attenuation coefficient.

CIT, a capacitance parameter applied for interface-trapped carriers.

Normally it is fixed to zero.

1.) The BSIM3v3 approach has a different formulation for operating regions vg > vth + 0.1V and vg < vth + 0.1V;

Therefore a discontinuous flicker noise model may occur

HiSIM_HV which uses one common formulation for strong and weak inversion operating regions.

2.) The DC modeling approach is of course different therefore the thermal noise description will also differ.

3.) Another approach to check is the input referred noise.

For accurate gm modeling also the input referred noise is simulated with higher accuracy.

If the gm does not differ much from both HV model approaches then the noise models it can be compared

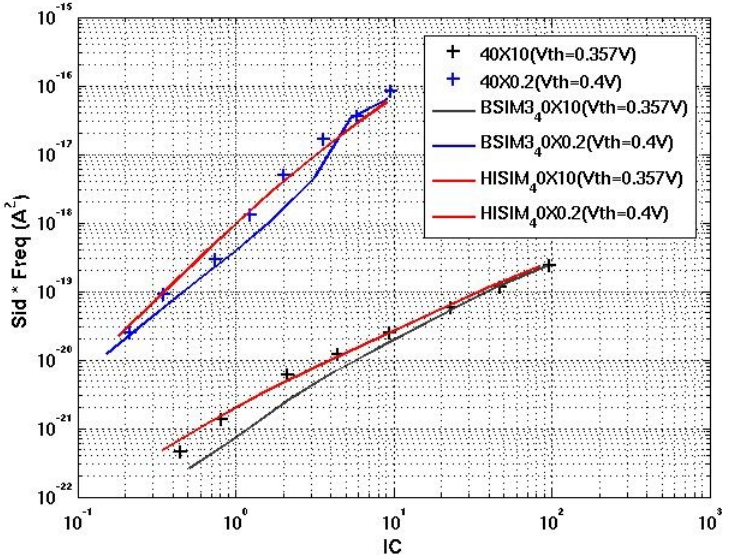
Sid & Svg Benchmark

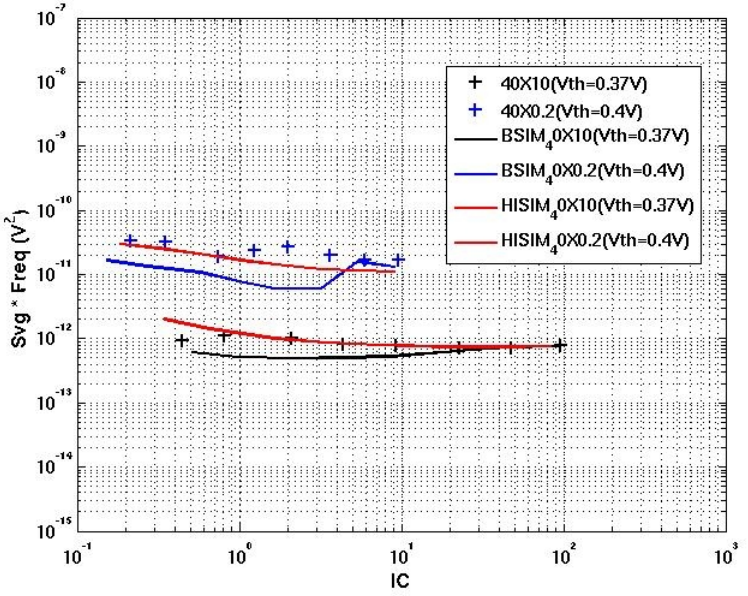
Sid Output referred Noise

&

Svg input referred Noise

Vds=3V versus inversion coefficient IC for a short channel and a long channel device (lower curves) measurements: black crosses, HiSIM_HV: red lines, BSIM3v3: dark lines





HV transistor performance constraints between RON and lifetime

AGING MODELING

Transistor Aging Effects and Reliability Constraints

Hot Carrier induced stress (HCS) for analog operation:

- –Transistors are stressed at VDSmax and VGS=Vt+Voverdrive.
- –Vt, IDSAT, IDlin and GMmax are used as degradation parameters.
- –The maximum allowed shift e.g. 10% for analog applications within extrapolated target lifetime (10 years with Duty Factor of 100).

Biased temperature high gate stress (BTS-VGS):

- –PMOS transistors are stressed at high temperature (e.g. T=125° C) and maximum Gate voltage.
- –The shift in threshold voltage (BMi) is used as degradation parameter for this effect.
- –The maximum allowed shift e.g. 10% for analog applications within extrapolated target lifetime (10 years with Duty Factor of 100).

Aging Simulation

SPICE Input dec
& Schematic

Analog Simulator

+

Aging Parameter Model
VT=f(t)
RD=f(t)
$\Delta = At^n$

Aging Simulator
P=f(t)
Sum (p.t)
Extrapolate product lifetime

Analog Simulator

Aging Modeling

HC:

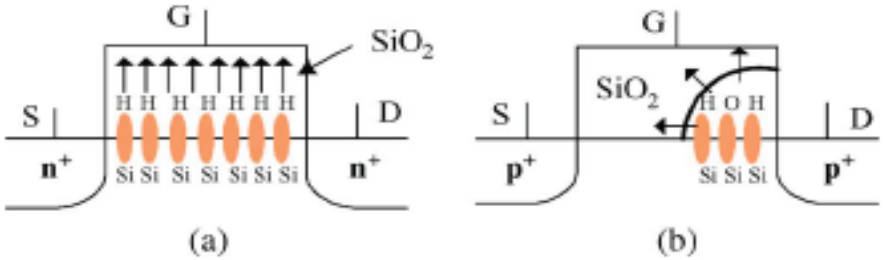
The *de facto* modeling method to analyze

CHC is based on substrate current Isub,

NBTI:

Generation of interface traps at Si/SiO2 interface

Vt degradation → partial recovery



R–D mechanism. (a) NBTI: 1-D hydrogen species diffusion (b) CHC: 2-D hot-carrier trapping.

HC and NBTI Modeling with Reaction Diffusion and hole trapping/detrapping mechanism :

→**ΔVT, Δ U0, Δ RON = f (N_{it})**

→**=f (isub, ids)**

Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology: Wenping Wang

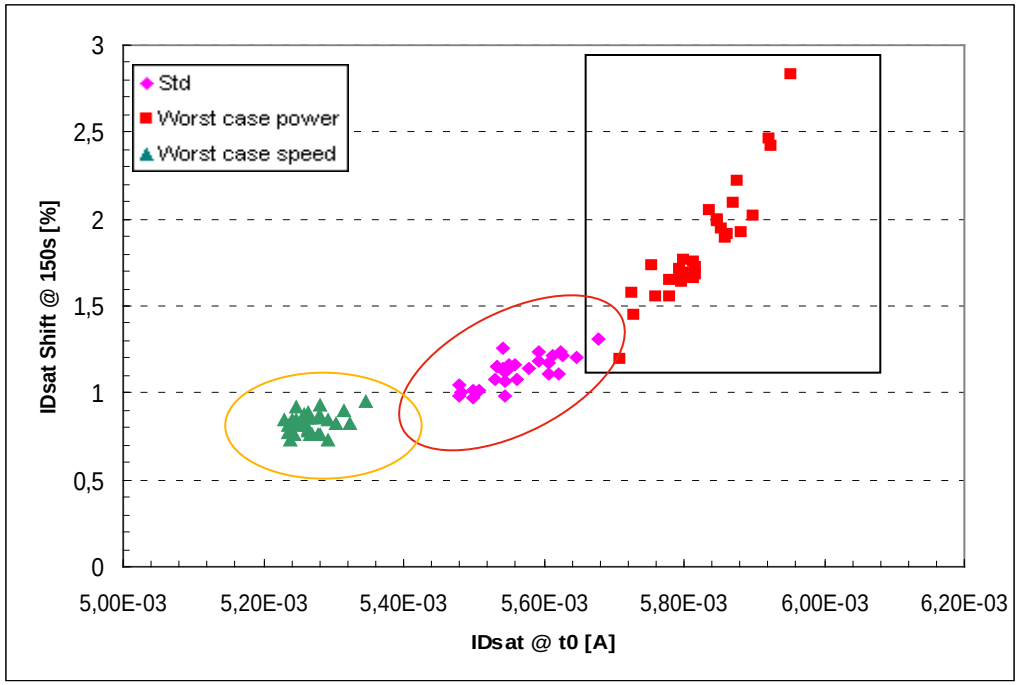
IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY, VOL. 7, NO. 4, DECEMBER 2007

HC Stress 150s @ 4.7V

IDsat shift %

Operating point definition:

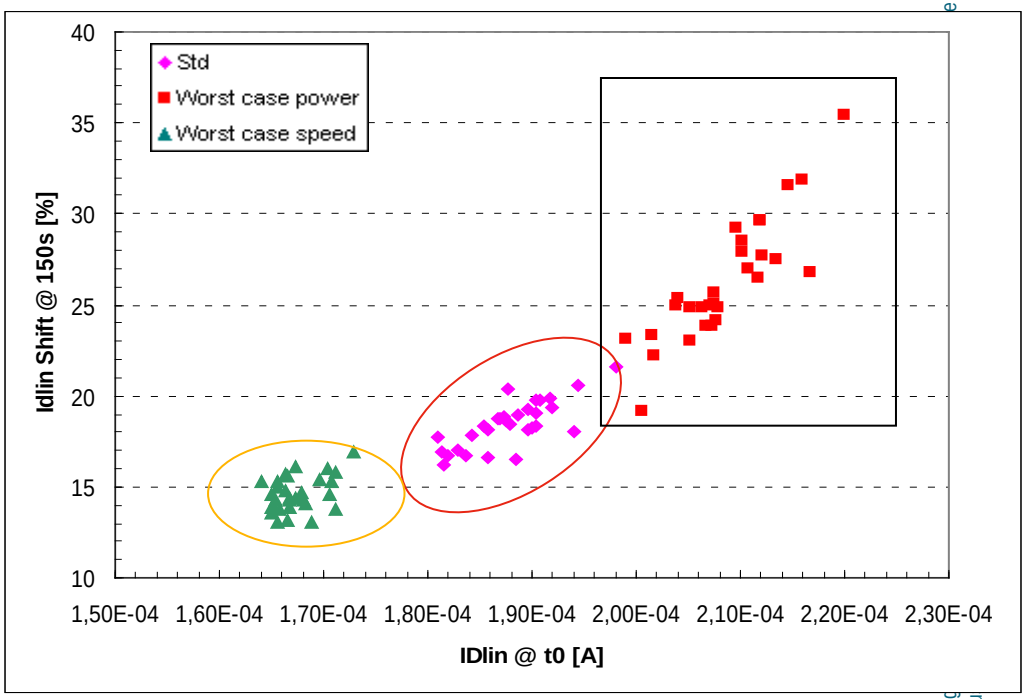
VD=VDmax, VG=VGmax



IDlin shift %

Operating point definition:

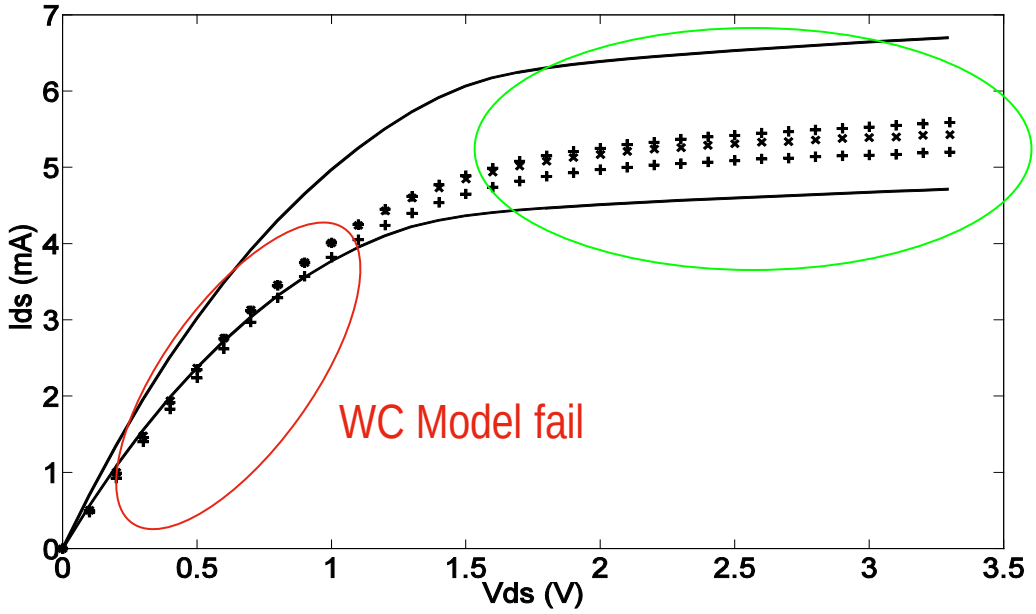
VD=0.1V, VG=VGmax



WC Reliability Model

- Investigation:
  - WC models v. reliability effects
- Consideration of output characterisitc shows:
  - Saturation region
    - ID variation covered also for stressed device
  - Linear region
    - Change in the resistive behavior
    - abs value of ID below WC emphasis

→ Additional reliability modeling necessary



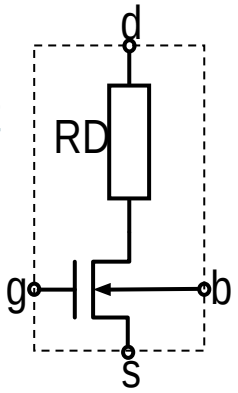
WC Reliability Model

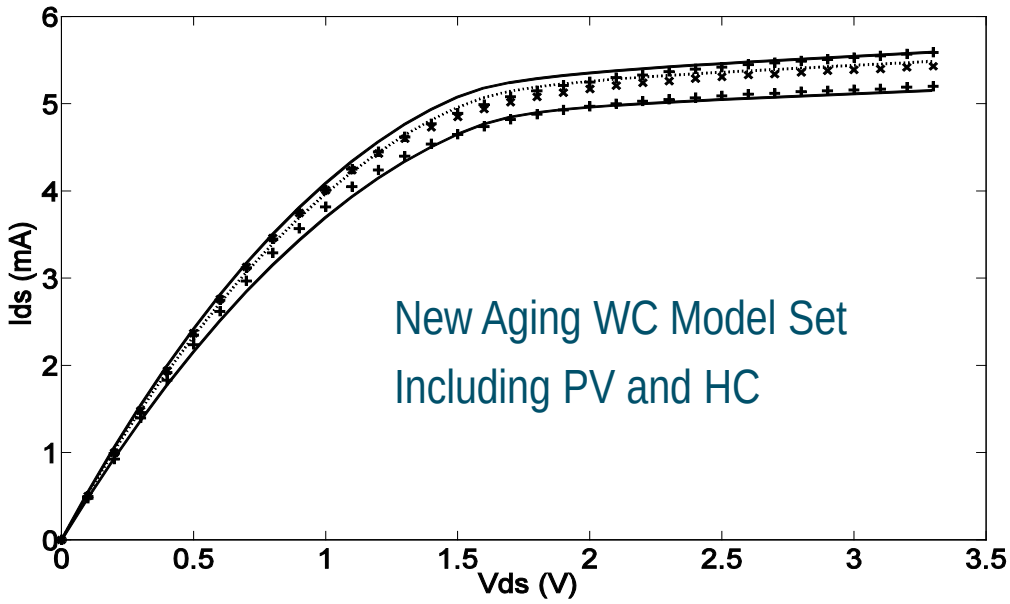
– Result:
  - Perfect curve fit due to the included PV method
  - Triode region shows also perfect fit after introduction of series resistance
  - Length dependency taken into account by voltage divider behavior

  - → This method is reliable
  - → provides fast simulation opportunity

Introduced Sub-circuit

$$R_{(t=x)} = R_{(t=0)} + R_{D(t=x)}$$





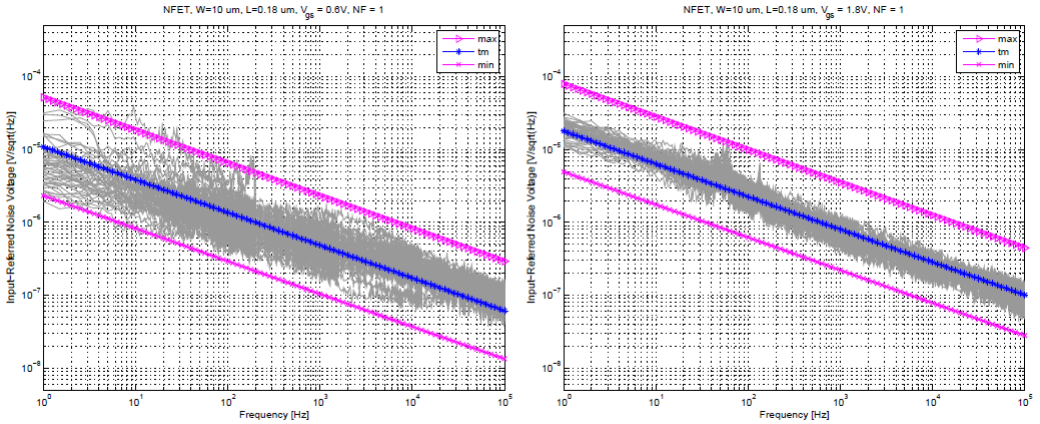
High Performance Analog

Variability of analog parameter gm/ID; gds; 1/f noise

Mismatch of active and passive devices

PROCESS VARIABILITY

1/f Noise Process Variability



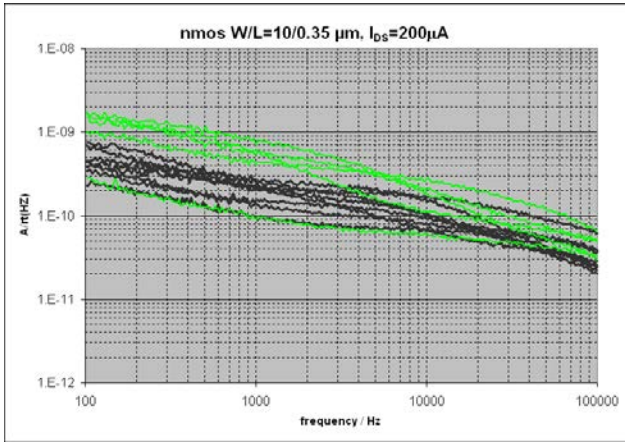
1/f noise variability

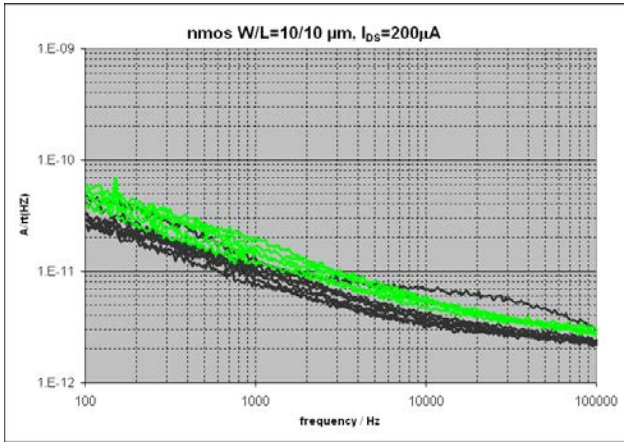
Variability increase with smaller ID

Variability increase with smaller L

→ Lorentzian Noise

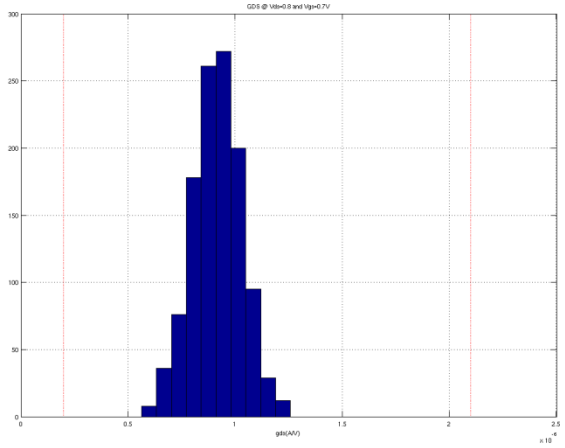
→ Covered with WC models



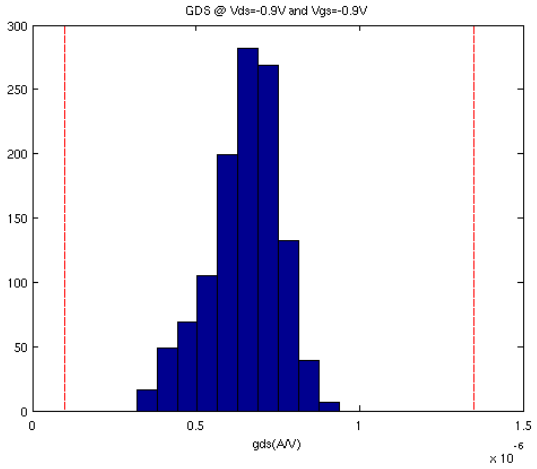


GDS MAP Implementation (1430 Data) v. WC Model

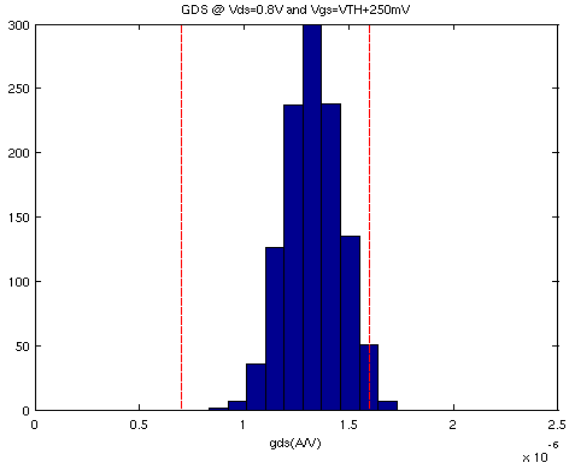
NMOS VGS=0.8V



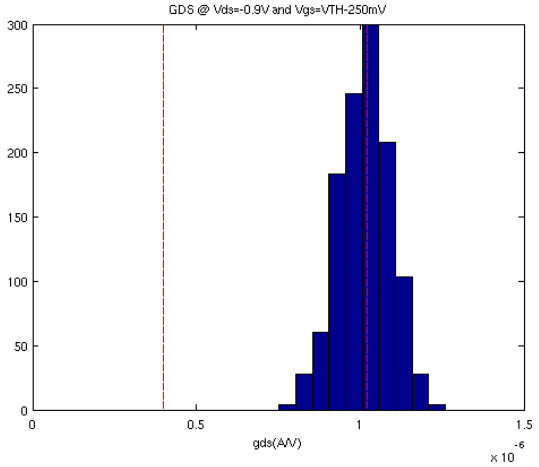
PMOS VGS=0.9V



NMOS VTH + 250mV

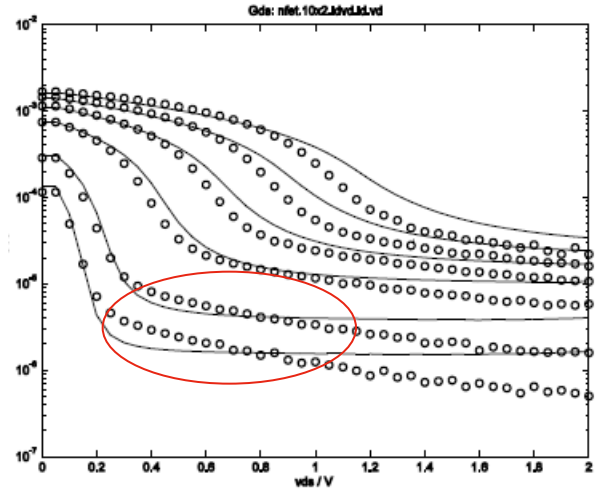


PMOS VTH + 250mV

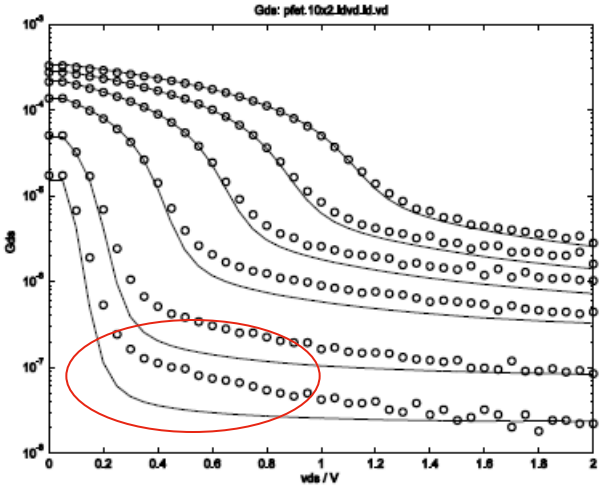


H18 GDS BSIM3v3 W/L= 10/2.0 (alpha3 version)

Standard Gds Modeling VGS=-0.48…1.8V

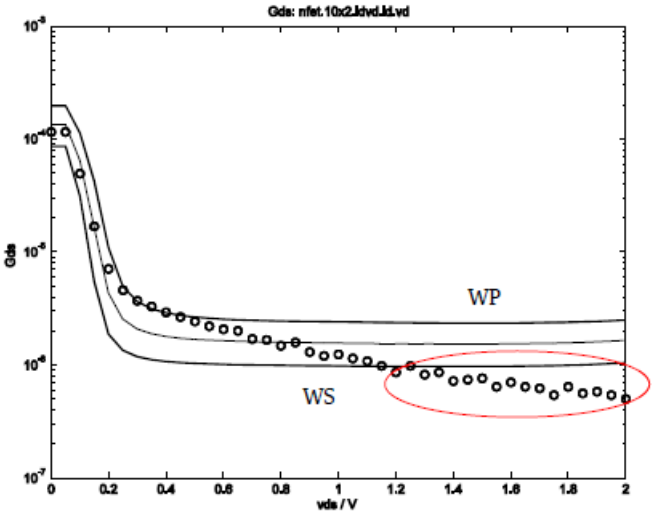


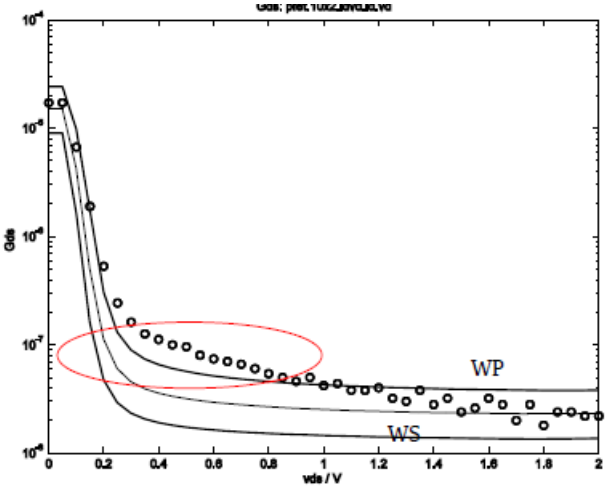
NFET



PFET

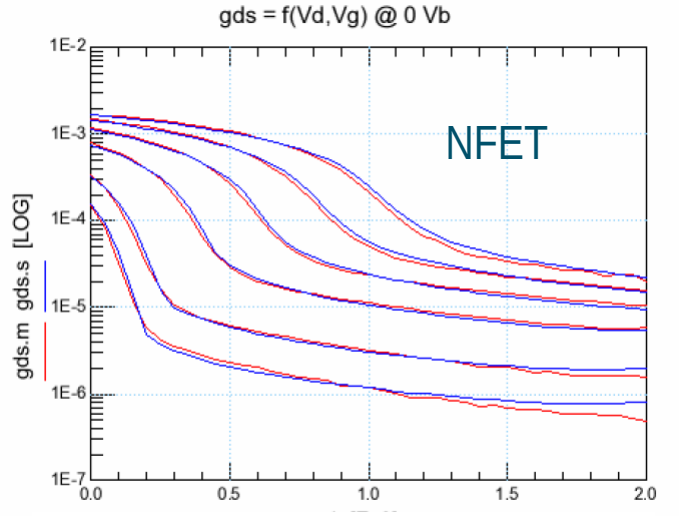
Analog Gds Modeling VGS=-0.47V Gds Modeling

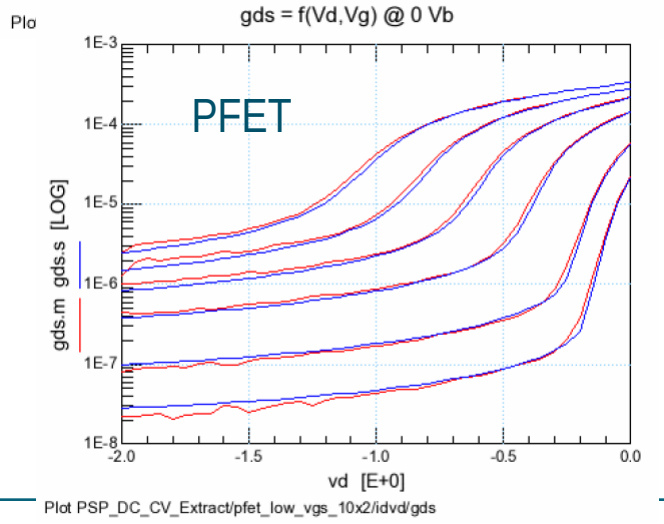




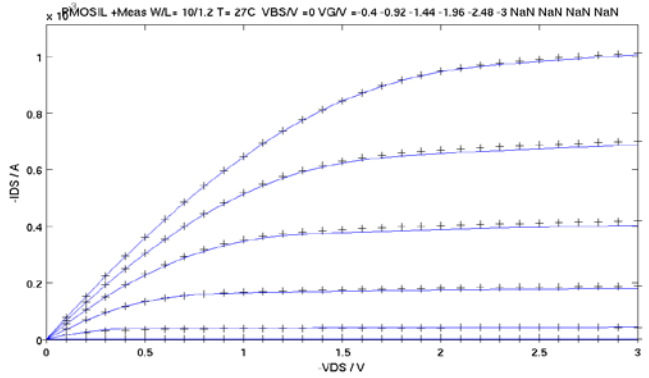
GDS with PSP and HiSIM2

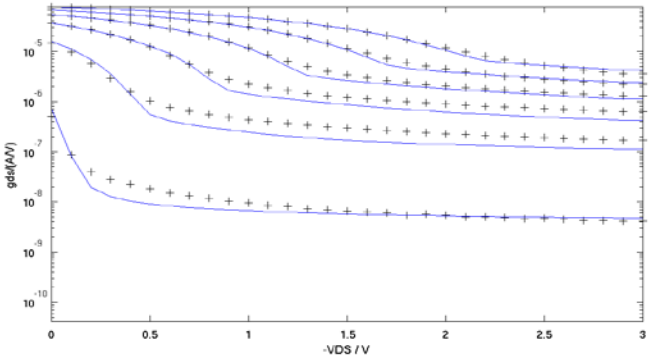
PSP Standard Gds Modeling W/L=10/2





HiSIM2 W/L=10/1.2





Summary

Analog modeling requirements for HV CMOS technology:

Analog design relies on

- Careful modeling of HV transistor
- Additionally PV for Small signal parameter, parasitic modeling, 1/f noise
- Need for aging modelling