Analytical Modeling of Triple-Gate MOSFET Structures

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Compact Modeling Network

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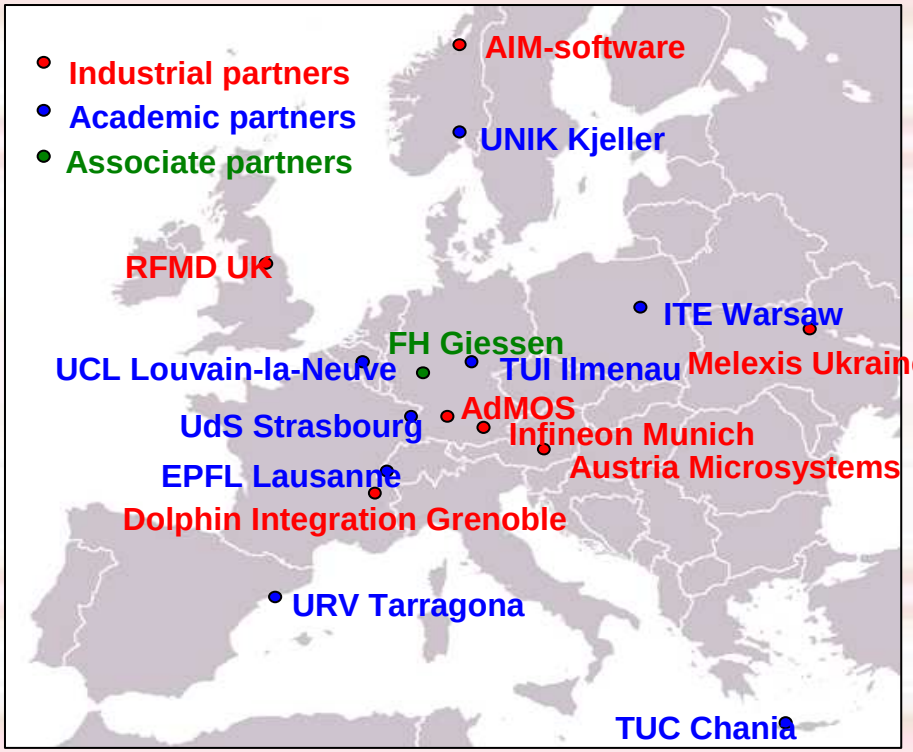
Outline

- Introduction
  - COMON project activities
  - Multi-Gate MOSFETs
- Analytical Electrostatic Modeling of Triple-Gate MOS Structures
- Complete Triple-Gate MOSFET models developed in the framework of COMON
- Conclusions

EU COMON Project – Who are we?

COMON: COmpact MOdeling Network



✓ "Marie-Curie" Industry-Academia Partneship and Pathways project (IAPP FP7, ref. pro. 218255)

✓ Duration:
4 years, started from December 1 2008.

✓ Coordinator:
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➢ More information available on our website:
http://www.compactmodelling.eu

Goals

To address the full development chain of Compact Modeling, to develop complete compact models of Multi-Gate MOSFETs (Foundry: Infineon, now Intel), HV MOSFETs (Foundry: Austriamicrosystems) and III-V HEMTs (RFMD (UK)).

Development of complete compact models of these types of advanced semiconductor devices.

Development of suitable parameter extraction techniques for the new compact models.

Implementation of the compact models and parameter extraction algorithms in automatic circuit design tools.

Demonstration of the implemented compact models by means of their utilization in the design of test circuits.

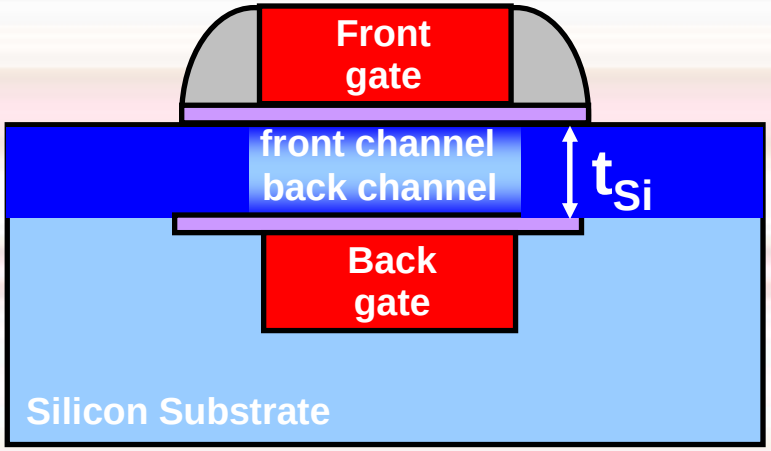
Validation and benchmarking: compact model evaluation for analog, digital and RF circuit design: convergence, CPU time, statistic circuit simulation.

As an IAPP project the ultimate COMON goal is the know-how transfer from the academia to the industry

Activities funded by COMON

- Secondments of young researchers between academia and industry
  - Universities sending students to the participating companies for several months
  - Also, several companies sending employees to universities for trainings
  - Secondments are the most instrumental tool for the transfer of knowledge between academia and industry
- Recruitments of postdoctoral researchers from outside the COMON network
- MOS-AK Workshops
- Training Courses on Compact Modeling
  - 1st Course, held in Tarragona (Spain) on June 30-July 1 2010
  - **2nd Course, to be held Tarragona (Spain) on June 28-29 2012**

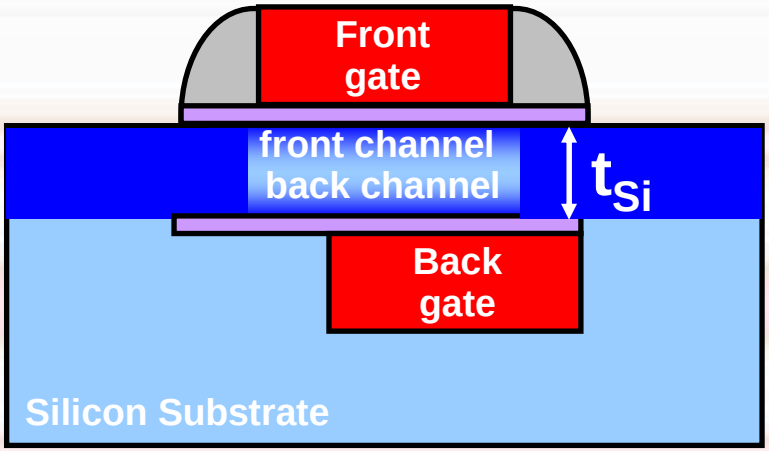
Why several gates?



'Planar double-gate' architecture

- Double-gate transistor
- Two conduction channels
  - ➡ good I_{ON}
- Excellent electrostatic coupling:
  - ➡ ✓ Short Channel Effects (SCEs) reduction
  - ✓ leakage currents reduction

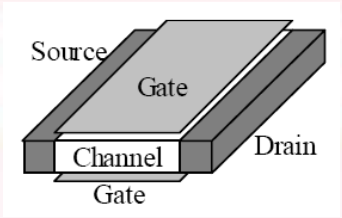
- But self-alignment of the gates required to maintain Double-gate advantages
  - ➡ idea of vertical gates: FinFET type transistors



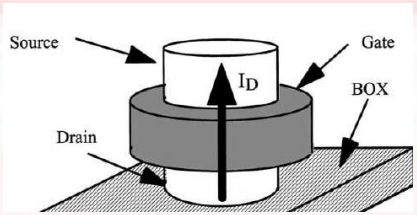
Gate misalignment

Multi-Gate MOSFETs

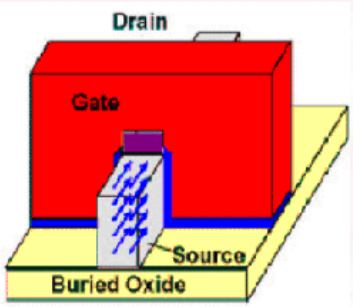
- The non-classical multi-gate devices such as Double-Gate (DG) MOSFETs, FinFETs or Gate-All-Around (GAA) MOSFETs show an even stronger control of short channel effects, and increase of on-currents taking advantage of volume inversion/accumulation.



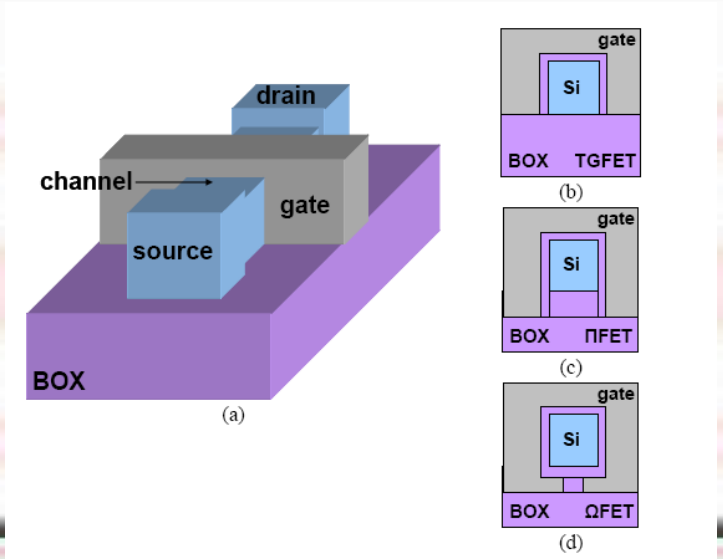
DG MOSFET



GAA MOSFET



FinFET



Tranversal cross-section for Triple-gate (b), Pi-gate FETs (c), and Omega-gateFETs (d).

Modeling Approaches

1) A **purely design-oriented** model developed by UCL/URV for symmetric DGMOSFETs. It is based on a 1D electrostatic analysis with semi-empirical equations with fitting parameters for short-channel effects. It can work for FinFETs and Tri-Gate MOSFETs if they are narrow enough.

2) A **predictive design-oriented** model developed by UdS/EPFL with the recent collaboration from URV. It was originally a quasi-2D model for DG MOSFET that became recently a quasi-3D model for Tri-Gate MOS structures. It uses very few fitting parameters and is explicit.

3) A fully 2D/3D **predictive technology-oriented** model, based on isomorphic expressions, developed by UniK in cooperation with URV. It is a predictive technology-oriented semi-analytical model.

1D Models

The first step to develop a compact model is to consider a well behaved device, with good electrostatic control by the vertical field (from the gate) and where the derivative of the lateral field in the direction of the channel length can be neglected compared to the derivative of the vertical field in the direction perpendicular to the channel.

- This is the gradual channel approximation, and simplifies the electrostatic analysis. This leads to neglect the short-channel effects

By integrating the Poisson's equation between the centre (y=0) and the top surface of the film ($y=-t_{si}/2$) we get an analytical expression of the vertical field at the interface, but it cannot be integrated to give an analytical expression of the potential if the doping is considered.

Approximations are needed, but there is an analytical solution in the case of undoped devices

Core (1D) undoped DG MOSFET Model

- An analytical solution is possible in the case of undoped DG MOSFET or cylindrical Surrounding-Gate MOSFETs
- For undoped DG MOSFETs, Poisson's equation:

$$\frac{d^2\psi(x)}{dx^2} = \frac{d^2(\psi(x)-V)}{dx^2} = \frac{q}{\varepsilon_{Si}} \cdot n_i \cdot e^{\frac{q(\psi(x)-V)}{kT}}$$

- The resulting charge control model can be written as:

$$(V_{GS} - V_0 - V) - = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right) \qquad Q_0 = 4\frac{kT}{q}C_{Si}$$

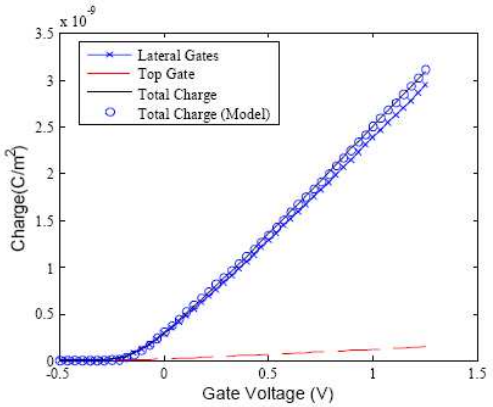
From this charge control model,

we get the expression of the current:

$$I_{DS} = \frac{W\mu}{L}\left[2\frac{kT}{q}(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\left(\frac{kT}{q}\right)^2 C_{Si}\log\left[\frac{Q_d + 2Q_0}{Q_s + 2Q_0}\right]\right]$$

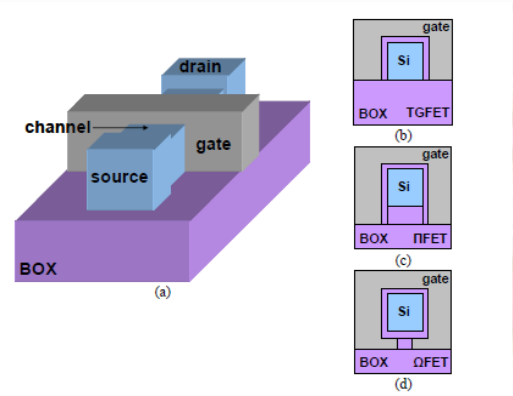
1D models: FinFET and Tri-Gate FET

In general, in symmetric Multi-Gate MOSFETs



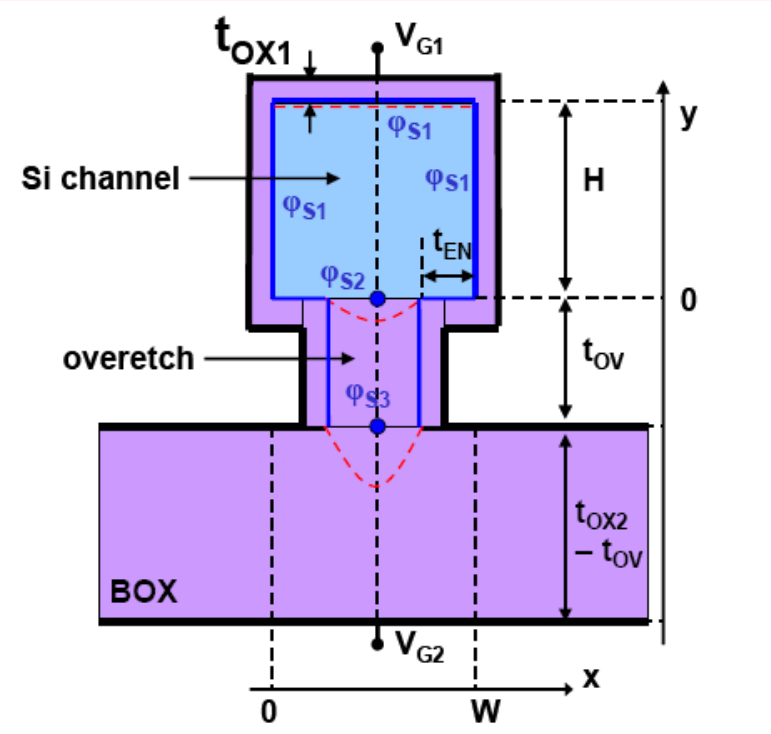
$$(V_{GS} - V_0 - V) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right)$$

Charge associated to top, lateral and total charge calculated with ATLAS 3-D simulations and with the unified charge control model (FinFET with W_{fin}=10 nm, H_{fin}=50 nm)



Anyway, a more physical and scalable model is needed, taking also into account the back-bias effects

Tri-Gate Modeling Assumptions



Transversal cross-section of an ΩFET transistor, with the notations used in this work.

- Undoped channels (mandatory for TG/Pi/Omega-gate FETs due to process considerations)
- 'Well-behaved' devices
- No corner effects (undoped channels)
- Constant surface potential (φ_{S1})
- Parabolic approximation at the body/overetched BOX boundary and at the overetched BOX/BOX boundary
- No quantum effects (W and H > 10 nm)
- Negligible carrier's concentrations up to threshold

✓ Simplified boundary conditions
✓ Electrostatics described by the Laplace equation ($\Delta\varphi \approx 0$)

Obtaining the potential (1)…

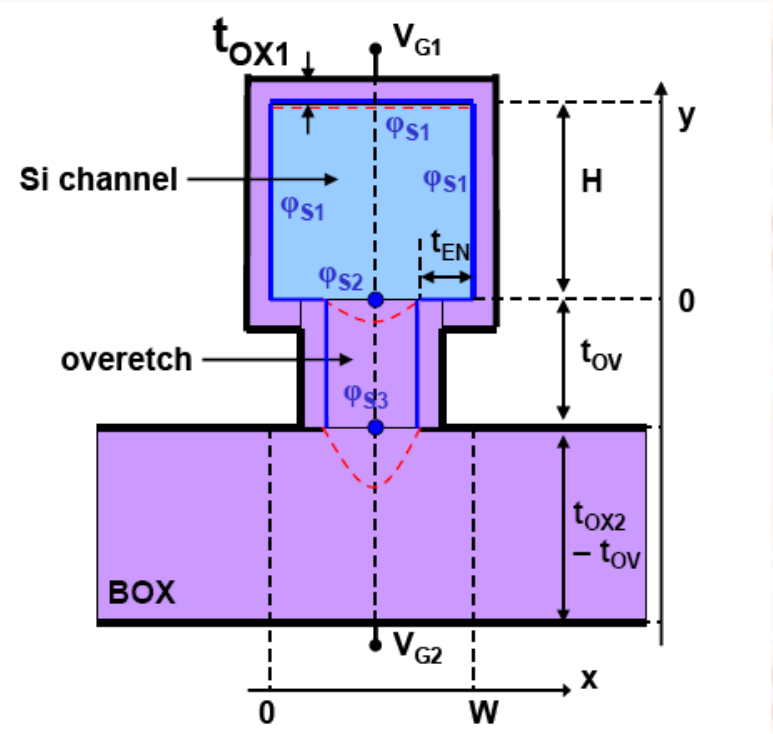
➢ Solution: development in Fourier's series with the coefficient calculated with respect to the boundary conditions (here, surface potentials $\varphi_{S1,2,3}$):

✓ In the channel:

$$\psi_{Si}(x,y) = \varphi_{S1} + (\varphi_{S2} - \varphi_{S1}) \sum_{n=1}^{+\infty} \frac{F_n}{W} \frac{\mathrm{sh}\left(\frac{n\pi(H-y)}{W}\right)}{\mathrm{sh}\left(\frac{n\pi H}{W}\right)} \sin\left(\frac{n\pi x}{W}\right)$$

✓ In the overetched region:

$$\psi_{OV}(x,y) = \varphi_{S1} + \left[P_n \sin\left(\frac{n\pi x}{W_2}\right) \sum_{n=1}^{+\infty} \frac{(\varphi_{S2} - \varphi_{S1})\mathrm{sh}\left(\frac{n\pi y}{W_2}\right) + (\varphi_{S3} - \varphi_{S1})\mathrm{sh}\left(\frac{n\pi(t_{OV} - y)}{W_2}\right)}{\mathrm{sh}\left(\frac{n\pi t_{OV}}{W_2}\right)} \right]$$



Transversal cross-section of a ΩFET transistor, with the notations used in this work.

with: $W_2 = W - 2t_{EN}$ the overetched region width.

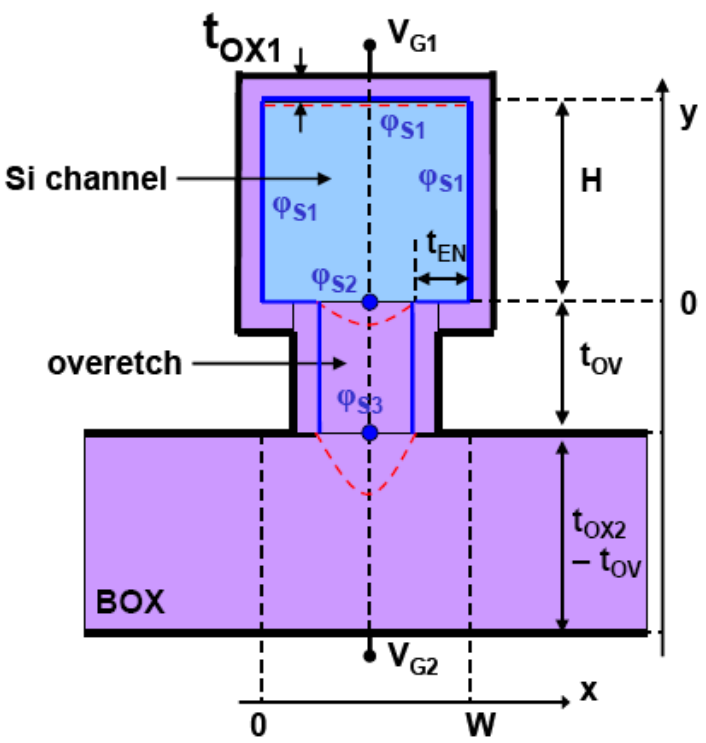
Obtaining the potential (2)...

with: $$P_n = \frac{2(1-\cos(n\pi)) - n\pi\sin(n\pi)}{(\frac{n\pi}{2})^3}$$

Coefficients coming from the **parabolic** approximation

Coefficients coming from the **Ω-shape** approximation

and:



Transversal cross-section of a ΩFET transistor, with the notations used in this work.

$$F_n = \frac{W\left[\begin{array}{l}(2t_{EN}n\pi\sin(n\pi) - n\pi W\sin(n\pi) - 2W\cos(n\pi) + 2W)\cos(\frac{n\pi t_{EN}}{W}) + \\ (-2t_{EN}n\pi\cos(n\pi) + n\pi W\cos(n\pi) + 2t_{EN}n\pi - n\pi W))\sin(\frac{n\pi t_{EN}}{W})\end{array}\right]}{(\frac{n\pi}{2})^3(W - 2t_{EN})}$$

Obtaining the front-gate threshold voltage

- Finally, after applying Gauss' law, we obtain the two master equations:

$$\begin{cases} V_{G1} = V_{FB1} + \varphi_{S1}(1+B) - \varphi_{S2}B \\ V_{G2} = V_{FB2} + \varphi_{S1}(C - D - (\frac{1+D}{F})(E+G-F)) + \varphi_{S2}((\frac{1+D}{F})(E+G) - C) \end{cases}$$

- Spliting the back-interface regimes (accumulation, depletion, and inversion)

$$a)\,back-gate\,accumulated\,(V_{G2} < V_{G2,ACC2} = V_{FB2} + (C - D - (\frac{1+D}{F})(E+G-F)\varphi_{ST}))$$

$$V_{TH1,ACC2} = V_{FB1} + (1+B)\varphi_{ST}$$

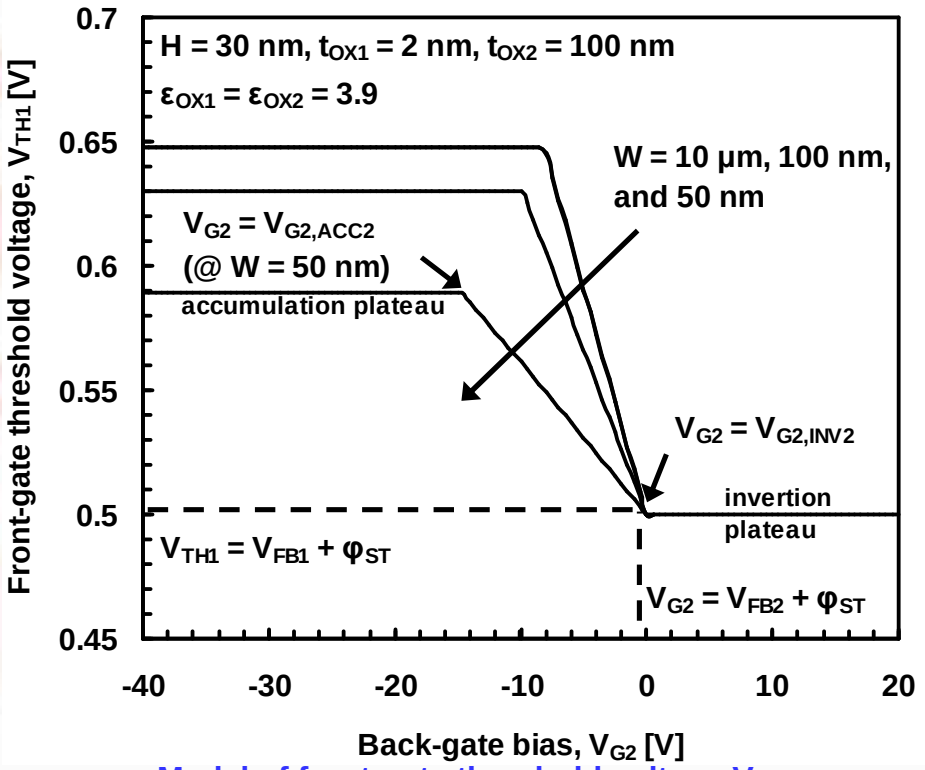
$$b)\,back-gate\,inverted\,(V_{G2} > V_{G2,INV2} = V_{FB2} + \varphi_{ST}):$$

$$V_{TH1,INV2} = V_{FB1} + \varphi_{ST}$$

$$c)\,back-gate\,depleted\,(V_{G2,ACC2} < V_{G2} < V_{G2,INV2}):$$

$$V_{TH1,DEP2} = V_{FB1} - (\frac{B}{1+\frac{1+D}{F}(E+G-F) - C + D})(V_{G2} - V_{FB2}) + (1 + \frac{B}{1+\frac{1+D}{F}(E+G-F) - C + D})\varphi_{ST}$$

Front-gate threshold voltage…



Model of front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} for Triple-gate FETs

- Plateaus when the back-interface is accumulated/inverted, linear decrease when the back-interface is depleted.
- Narrow devices: larger ‘depleted back-interface’ region and smaller amplitude of threshold voltage.

2.3 Obtaining the back-gate threshold voltage

- With the two master equations:

$$\begin{cases} V_{G1} = V_{FB1} + \varphi_{S1}(1+B) - \varphi_{S2}B \\ V_{G2} = V_{FB2} + \varphi_{S1}(C - D - (\frac{1+D}{F})(E+G-F)) + \varphi_{S2}((\frac{1+D}{F})(E+G) - C) \end{cases}$$

- Similarly, it yields:

a) front – gate accumulated $(V_{G1} < V_{G1,ACC1} = V_{FB1} - B\varphi_{ST})$

$$V_{TH2,ACC1} = V_{FB2} + ((1+D)(\frac{E+G}{F}) - C)\varphi_{ST}$$

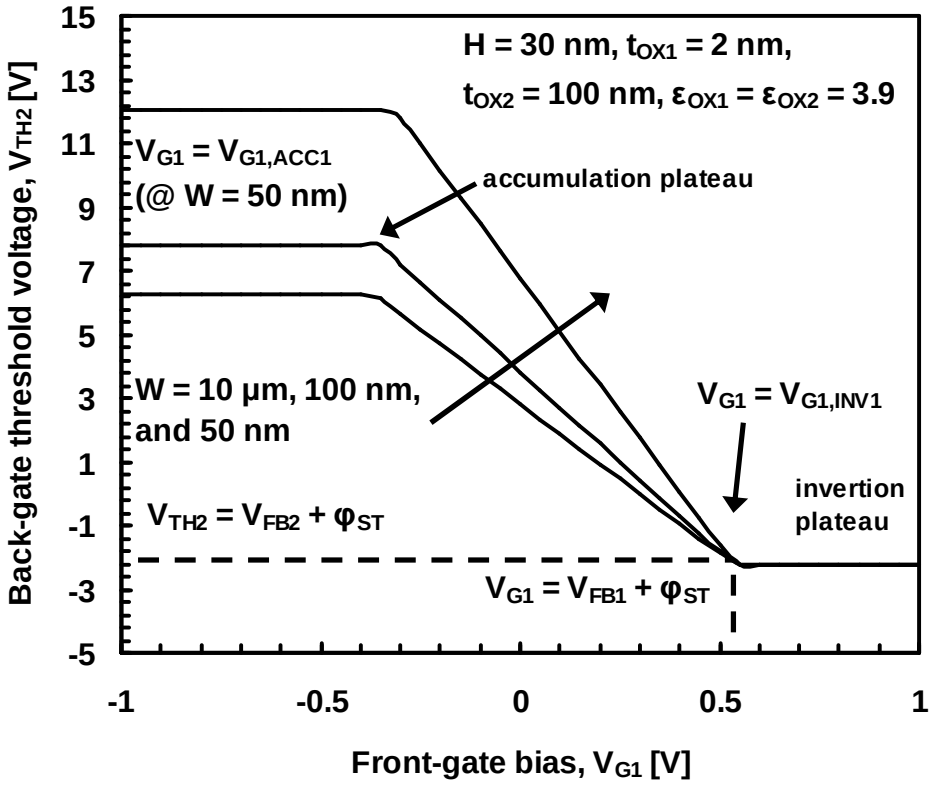
b) front – gate inverted $(V_{G1} > V_{G1,INV1} = V_{FB1} + \varphi_{ST})$:

$$V_{TH2,INV1} = V_{FB2} + \varphi_{ST}$$

c) front – gate depleted $(V_{G1,ACC1} < V_{G1} < V_{G1,INV1})$:

$$V_{TH2,DEP1} = V_{FB1} - (\frac{(1+D)(\frac{E+G}{F}) - C - 1}{1+B})(V_{G1} - V_{FB1}) + (1 + \frac{(1+D)(\frac{E+G}{F} - C - 1)}{1+B})\varphi_{ST}$$

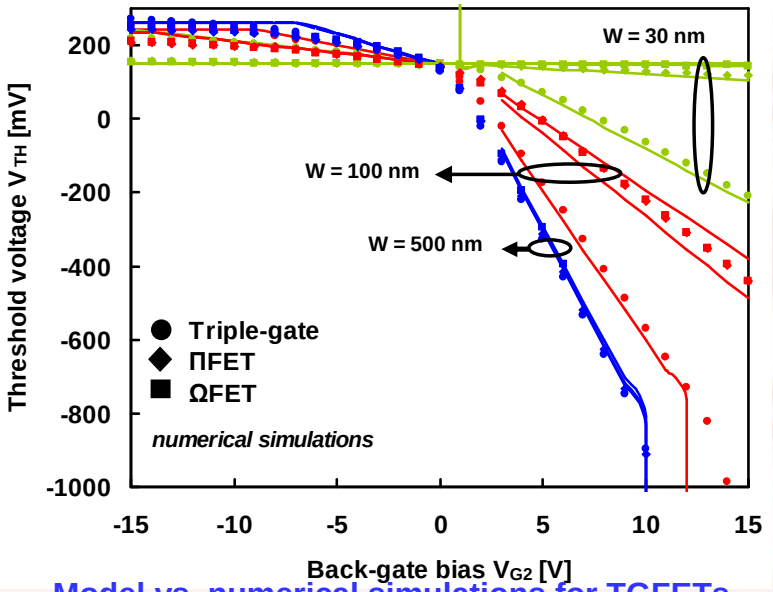
Back-gate threshold voltage…



Model of back-gate threshold voltage V_{TH2} vs. front-gate bias V_{G1} for Triple-gate FETs

- Plateaus when the back-interface is accumulated/inverted, linear decrease when the back-interface in depleted.
- Narrow devices: SMALLER ‘depleted back-interface’ region and LARGER amplitude of threshold voltage.

Validation – Numerical Simulations

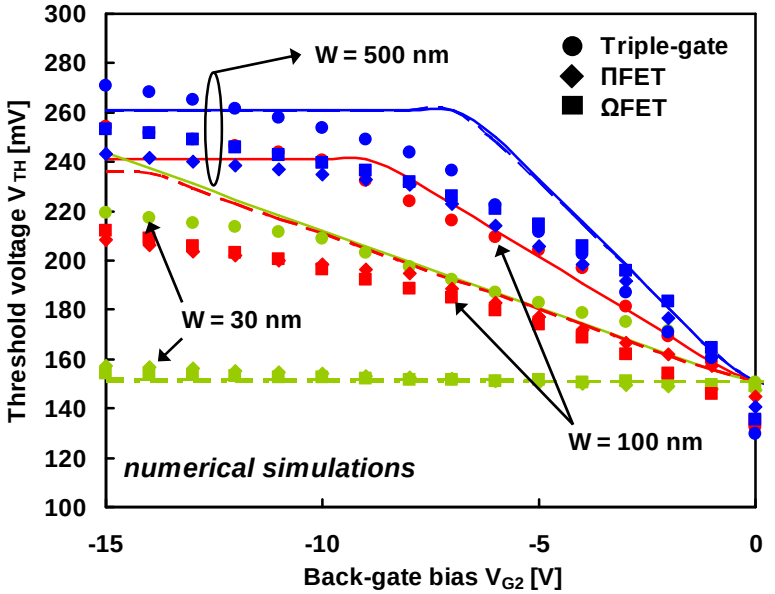


Model vs. numerical simulations for TGFETs, Pi-gateFETs, ΩFETs, and for channel width W=30, 100, and 500 nm.

- Good agreement model/simulations for TGFETs, Pi-gate FETs, and ΩFETs.
- Pi-gate FET threshold voltage less sensitive to back-gate bias than TGFET.
- ΩFET threshold voltage less sensitive to back-gate bias than Pi-gate FETs.
- Narrow devices threshold voltage less sensitive to back-gate bias than wide devices.

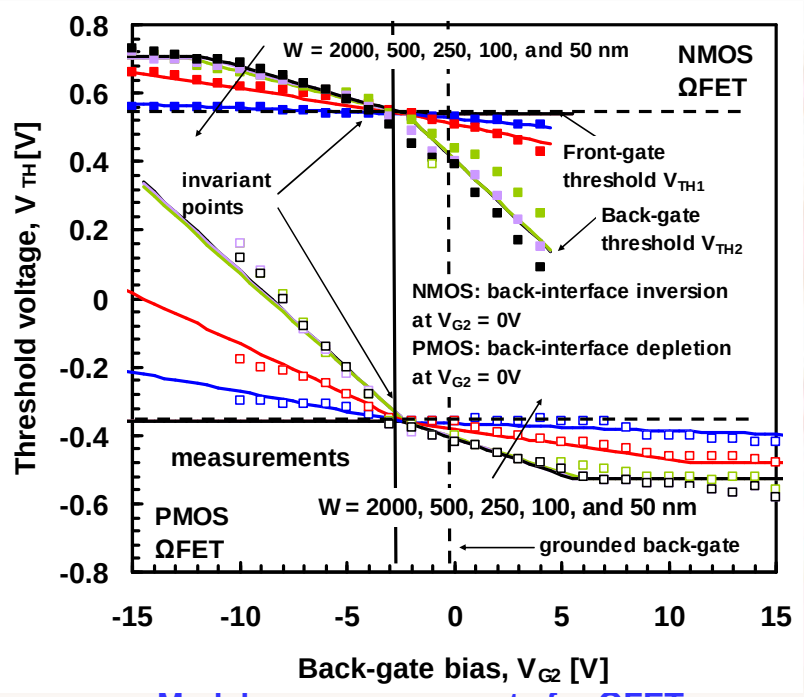
- Zoom of the previous figure in the back-interface accumulation/depletion zones:

Acceptable agreement and correct modelling of the 'front-to back-interfaces coupling' coefficients



Model vs. numerical simulations for TGFETs, Pi-gateFETs, ΩFETs, and for channel width W=30, 100, and 500 nm.

Validation – Experimental meas.

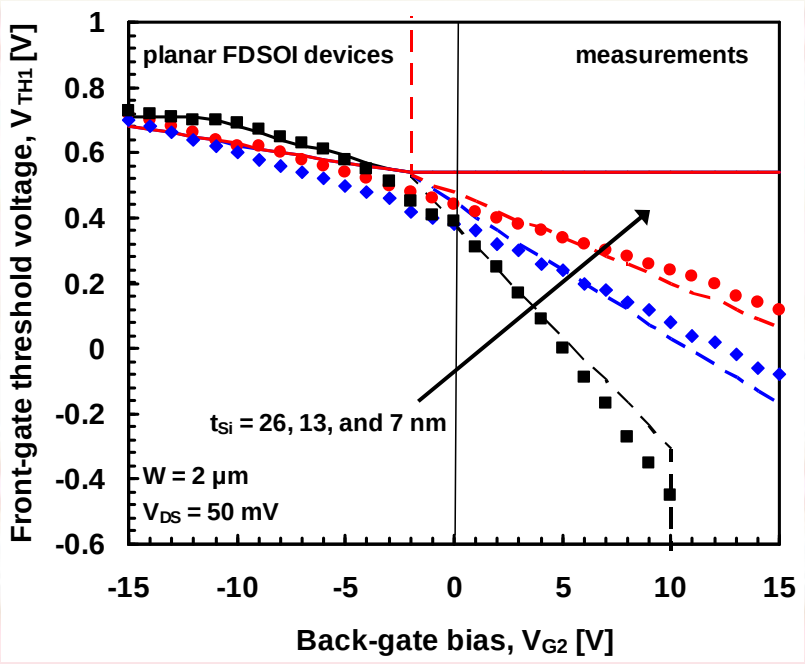


Model vs. measurements for ΩFETs, and for channel width W from 2 µm down to 50 nm.

➢ Good agreement model/measurements for experimental wide devices (ΩFETs in the planar FDSOI configuration) for different channel thicknesses (26, 13, and 7 nm).

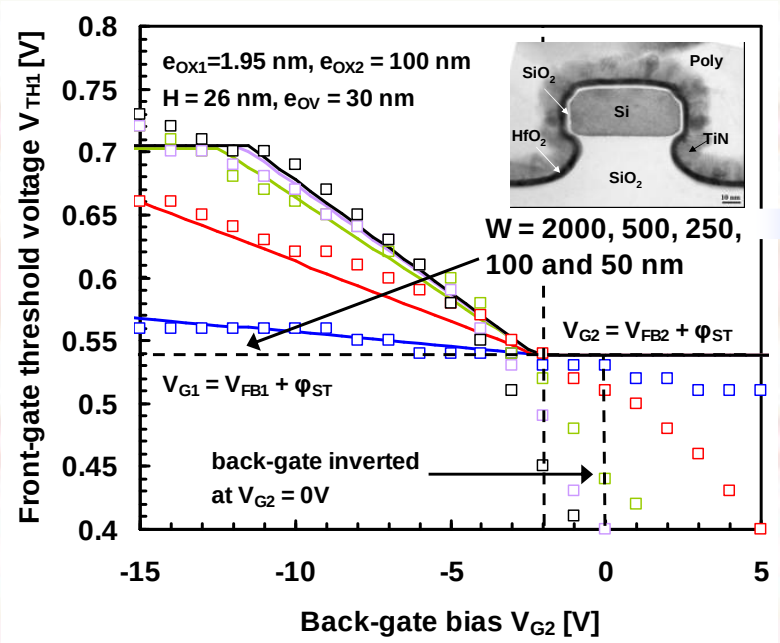
➢ Good agreement model/measurements for experimental ΩFETs (H = 26 nm, W from 2 µm down to 50 nm).

➢ Good modelling for both NMOS and PMOS devices.



Model vs. measurements for wide ΩFETs (W = 2 µm), and for channel thicknesses (t_{Si} or H) of 26, 13, and 7 nm.

Why is that so important to take into account the back-gate?



Comparison front-gate threshold voltage V_{TH1} vs. back-gate bias V_{G2} with model (lines) and experimental measurements (squares)

➢ Under 'normal' condition, with a grounded back-gate ($V_{G2} \approx 0$ V):

- Direction and amplitude of the $V_{TH}(W)$ curves driven by the position of the invariant point
- No amplitude at the invariant point. Not true elsewhere.
- Back-interface in accumulation, in depletion or in inversion?

➢ Experimental determination of the invariant point position with the $V_{TH1}(V_{G2})$ curves for several Fin widths W:

→ Determination of the back-gate regime at V_{G2} = 0 V

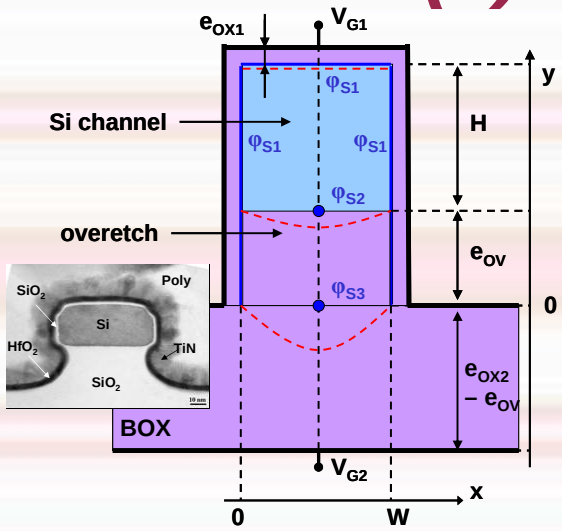
→ Determination of the correct $V_{TH1}(W)$ evolution

3D potential, TG and PiFETs (1)

- 3D Laplace's equation to solve:

$$\frac{\partial^2\psi(x,y,z)}{\partial x^2}+\frac{\partial^2\psi(x,y,z)}{\partial y^2}+\frac{\partial^2\psi(x,y,z)}{\partial z^2}\approx 0$$

- Boundary conditions
  - ✓ Influence of the 6 terminals (3 sides of the top-gate, back-gate, source and drain) considered separately.
  - ✓ Dirichlet (with constant or parababolic boundary conditions) or Neumann.
- 3D potential



Transversal cross-section TGFET/PiFET, with notations.

$$\psi(x,y,z)=\psi_{\text{Top-gate (TG)}}(x,y,z)+\psi_{\text{Back-gate (BG)}}(x,y,z)+\psi_{\text{Lateral-gates (LG)}}(x,y,z)+\psi_{\text{Source / Drain (SD)}}(x,y,z)$$

$$\psi_{TG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_p(m)F_p(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi y\right)\Big/\cosh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi(H+e_{OV})\right)\right]$$

$$\psi_{LG}(x,y,z)=(V_{G1}-V_{FB1})\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_p(m)F_n(n)\sin\left(\frac{m\pi z}{L_G}\right)\sin\left(\frac{(2n+1)\pi(H+e_{OV}-y)}{2(H+e_{OV})}\right)\left[\frac{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi(W-x)\right)+\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi x\right)}{\sinh\left(\sqrt{\left(\frac{m}{L_G}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi W\right)}\right]$$

$$\psi_{SD}(x,y,z)=\sum_{m=1}^{+\infty}\sum_{n=0}^{+\infty}F_p(m)F_n(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{(2n+1)\pi(H+e_{OV}-y)}{2(H+e_{OV})}\right)\left[\frac{V_S\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi(L_G-z)\right)+V_D\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi z\right)}{\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{2n+1}{2(H+e_{OV})}\right)^2}\pi L_G\right)}\right]$$

$$\psi_{BG}(x,y,z)=\varphi_{S3}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_p(m)F_p(n)\sin\left(\frac{m\pi x}{W}\right)\sin\left(\frac{n\pi z}{L_G}\right)\left[\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi(H+e_{OV}-y)\right)\Big/\sinh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi(H+e_{OV})\right)\right]$$

with:

$$\varphi_{S3}=(V_{G2}-V_{FB2})\Big/\left(1+\frac{\varepsilon_{Si}}{\varepsilon_{BOX}/(e_{OX2}-e_{OV})}\sum_{m=1}^{+\infty}\sum_{n=1}^{+\infty}F_p(m)F_p(n)\sin\left(\frac{m\pi}{2}\right)\sin\left(\frac{n\pi}{2}\right)\left[\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi\Big/\tanh\left(\sqrt{\left(\frac{m}{W}\right)^2+\left(\frac{n}{L_G}\right)^2}\pi(H+e_{OV})\right)\right]\right)$$

W being the fin width, H the fin height, L_G the gate length, e_{OV} the overetch depth, ε_{BOX} the BOX permittivity, ε_{Si} the silicon permittivity, V_{FB1} (resp. V_{FB2}) the front-gate (resp. back-gate) flat band voltage. The series coefficient F_p, F_n, and F_c are defined in the Appendix.

3D potential, TG and PiFETs (2)

➢ With the boundary coefficients:

- Constant potential boundary condition :

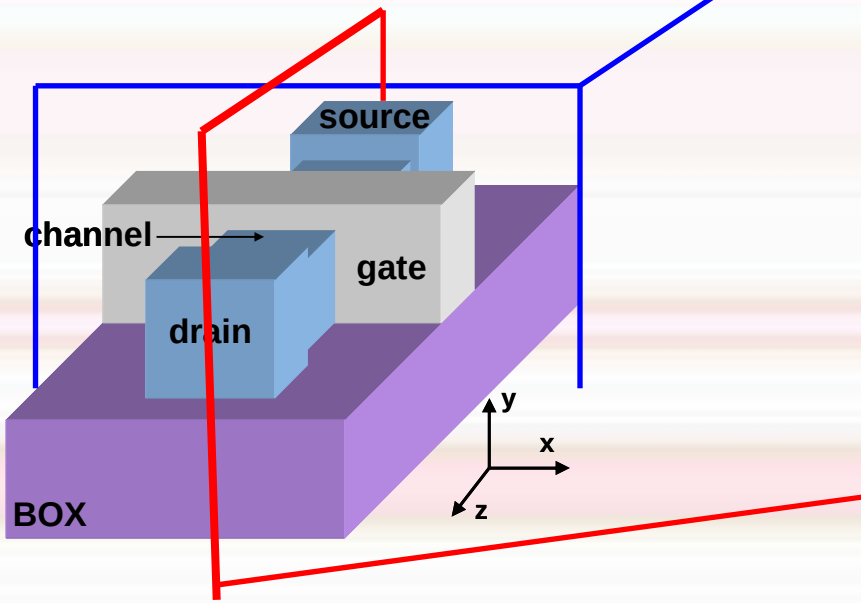
$$F_c(n) = \frac{2(1-\cos(n\pi))}{n\pi}$$

- Parabolic potential boundary condition

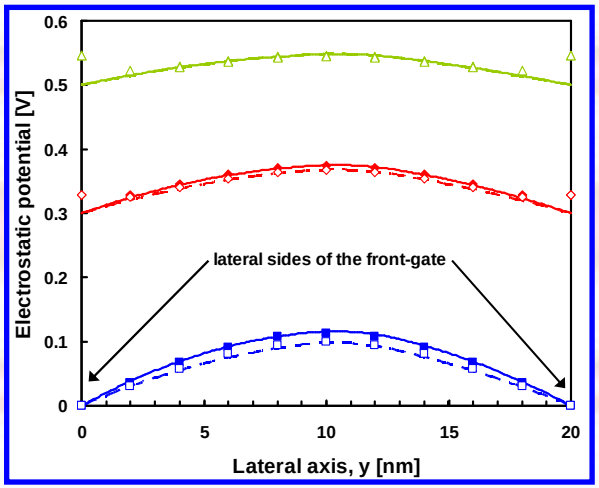
$$F_p(n) = \frac{2(1-\cos(n\pi)) - n\pi\sin(n\pi)}{(\frac{n\pi}{2})^3}$$

- Neumann boundary condition :

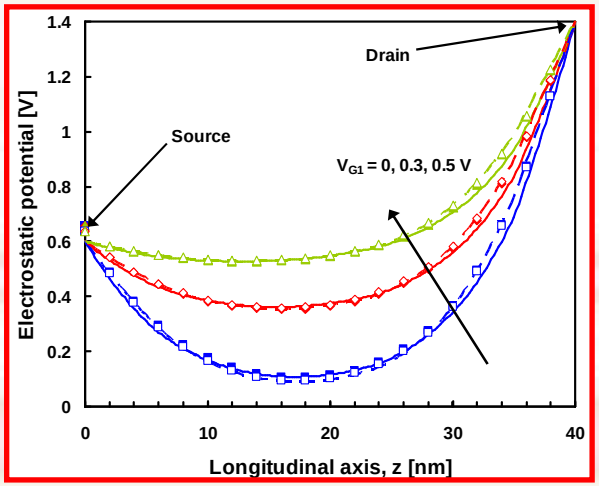
$$F_n(n) = \frac{4}{(2n+1)\pi}(1-\cos(\frac{(2n+1)\pi}{2}))$$



➢ **Validation** of the models:



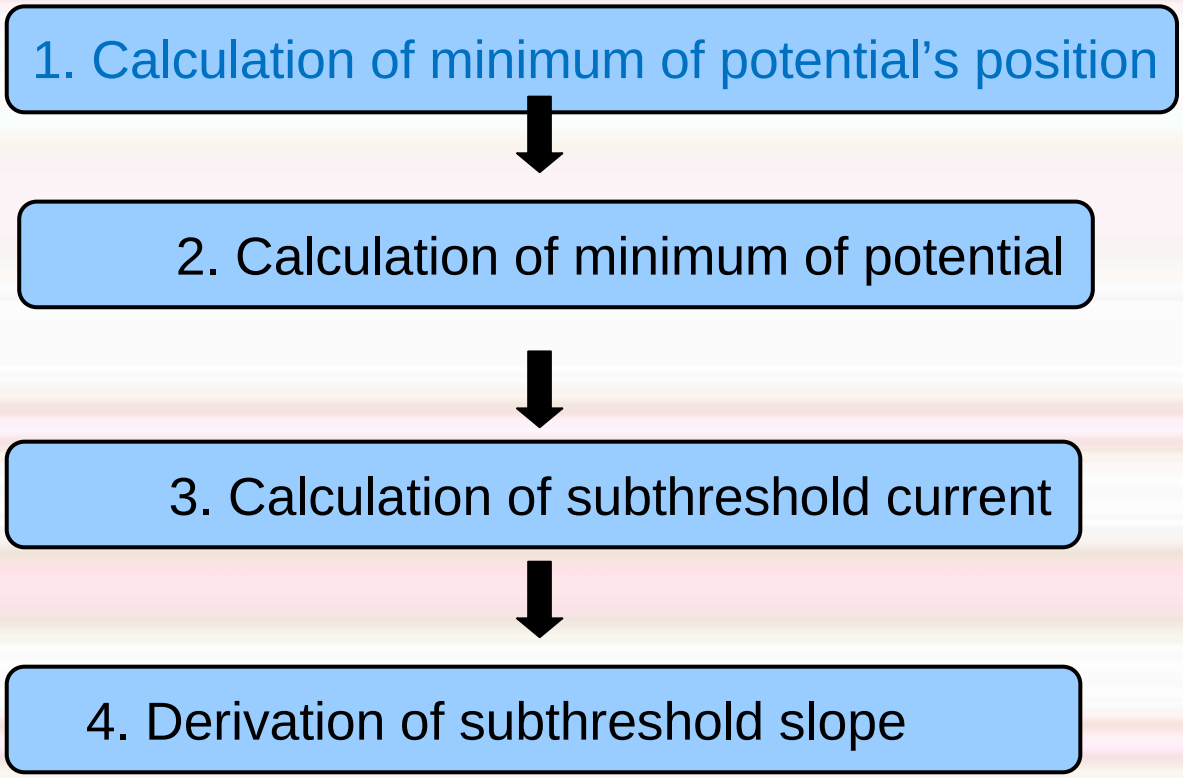
TGFET (closed symbols) and PiFET (open symbols)



TGFET (closed symbols) and PiFET (open symbols)

Model Flow Chart

- ✓ For undoped channels and deep subthreshold operation, the position of the most leaky path is determined mostly by the the device geometry (and gate biases boundary conditions)
- ✓ Most leaky path: approximation saying that the current flowing where the gate control is the weakest gives a good reproduction of the global device's behavior.



Calculation of the minimum potential

- ✓ Position of the 'most leaky path':
  - ✓ At mid-channel (y=W/2) for obvious symmetry considerations
  - ✓ At the body/BOX interface ($x = t_{OV}$): generally true, not necessarily for

L<(W,H) but is a correct approximation

  - ✓ Along the Source/Drain axis:
    - ✓ Low V_{DS}: $Z_C = L_G/2$
    - ✓ High V_{DS}: minimum of potential moving closer to the source
  - ✓ Formula from [Pei´02]:

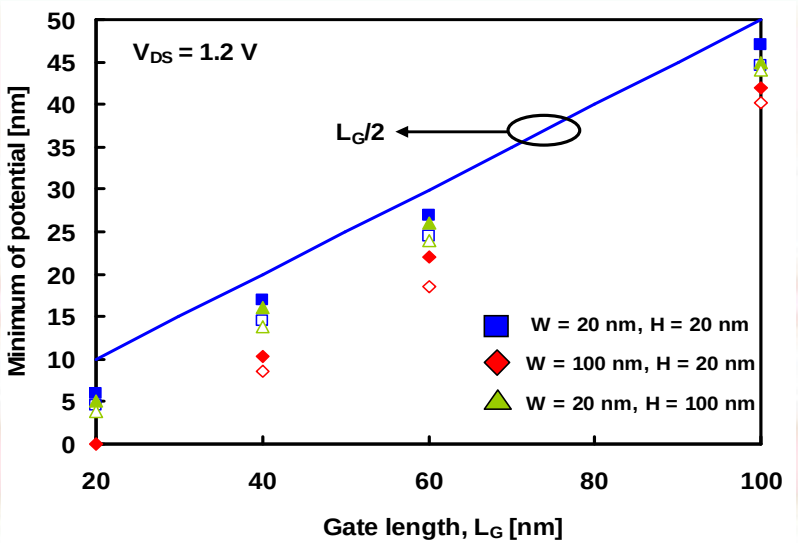
$$Z_C = \frac{L_G}{2} + \frac{L_D}{2\pi}\ln\left(\frac{-\varphi_{MS}}{-\varphi_{MS}+V_{DS}}\right)$$

with:

$$L_D = \left(\frac{1}{W^2} + \frac{0.5}{H^2}\right)^{-1/2}$$

➡ Simpler and acceptable approximation

- ✓ Finally: $\varphi_{MIN} = \varphi(t_{OV}, W/2, Z_C)$



Position of the minimum of potential along the S/D axis – comparison between the results given by the numerical simulations (closed symbols) and the analytical formula (open symbols)

[Pei'02] G. Pei et al., IEEE TED, 2002.

Calculation of the subthreshold current

- ✓ Assuming Drift-Diffusion transport, drain current written as:

$$I_{DS} = q\mu n_i \frac{\int_0^{V_{DS}} e^{-\varphi_F/V_T} d\varphi_F}{\int_0^{L_G} \frac{dz}{\int_{t_{OV}}^{t_{OV}+H} \int_{-W/2}^{W/2} e^{\varphi(x,y,z)/V_T} dxdy}}$$

- ✓ Using the most leaky path approach, current expressed as:

$$I_{DS} = \frac{\mu q n_i V_t}{L_G}(1-e^{-V_{DS}/V_t}) \int_{t_{OV}}^{t_{OV}+H} \int_{-W/2}^{W/2} e^{\varphi_{MIN}(x,y,Z_C)/V_T} dxdy$$

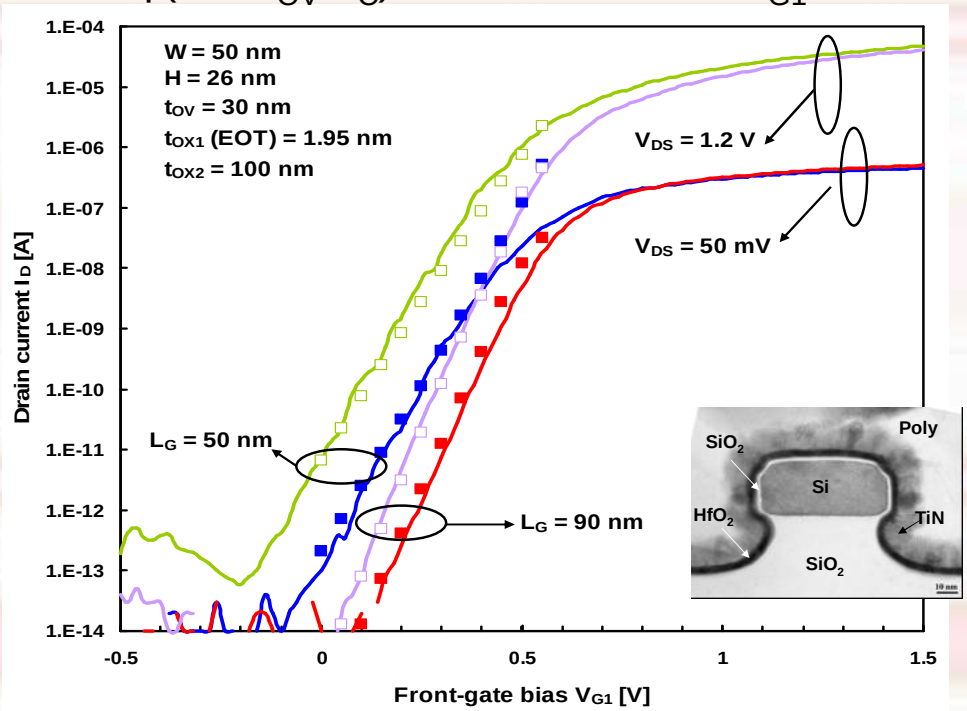
  - ✓ This work: approximation that the exponential of the potential can be described by a parabola in the width direction and is constant in the height direction.
  - ✓ Approximation amounting to say that a majority of carriers are located close to φ_{MIN}, i.e. in the vicinity of ($x=W/2$, $y=t_{OV}$)

Calculation of the subthreshold current

✓ Finally, after integration:

$$I_{DS} = \frac{\mu q n_i V_T}{L_G}\left(1 - e^{V_{DS}/V_t}\right) WH \frac{2e^{\varphi(W/2, t_{OV}, Z_C)/V_t} + e^{V_{G1}/V_t}}{3}$$

n.b.: $\varphi(W/2, t_{OV}, Z_C)$ also a function of V_{G1}

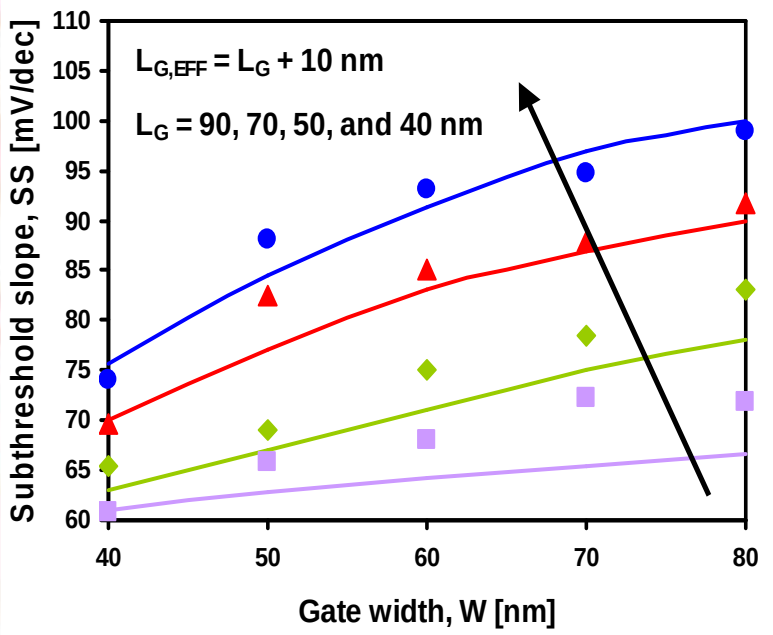


Subthreshold analytical (symbols) and experimental (solid lines) drain currents I_D vs. front-gate bias V_{G1} for gate lengths L_G of 90 nm (squares) and 50 nm (diamonds). Gate width W = 50 nm, H = 26 nm.

Good precision obtained compared to experimental measurements [Jahan'05]

Formula allowing to take into account the drain and short channels effect in the subthreshold regime

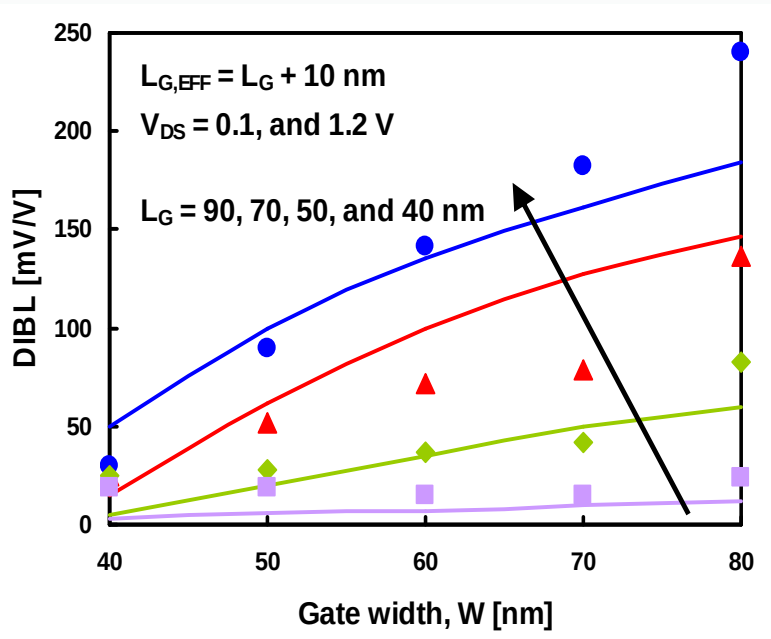
Subthreshold slope, DIBL



SS vs. gate width W and gate length L_G. Model (lines) and experimental measurements (symbols)

- Calculation of the potential minimum and derivation of the subthreshold slope and DIBL.

- Correct agreement model/experimental.
- Subthreshold characteristics improved with narrower devices.



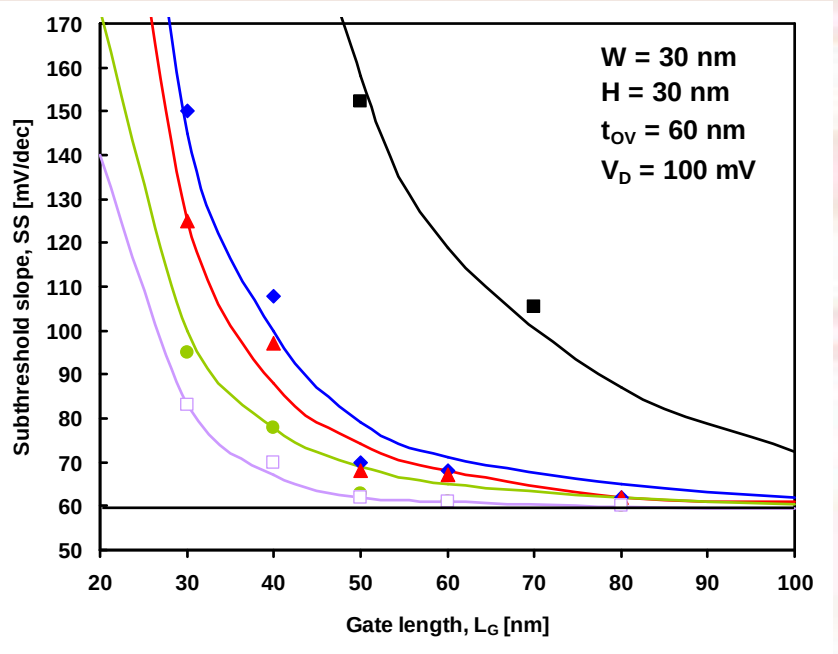
DIBL vs. gate width W and gate length L_G. Model (lines) and experimental measurements (symbols)

Device Scaling

- PiFET structure adaptable to TGFETs, DGFETs, planar FDSOI devices, and GAA transistors.
- Expressions extendible to a large number of MuGFETs.

Structure	Features
Pi-gateFET (core structure)	$t_{OV} \neq 0$
TGFET	$t_{OV} \approx 0$
Planar FDSOI	$t_{OV} \approx 0$, W>>H
DGFET/FinFET	$t_{OV} \approx 0$, W<<H
Gate All Around	$t_{OV} \approx 0$, $\varphi_{S3} = V_{G1} - V_{FB1}$

Variations of the core structure



SS vs. gate gate length L_G for GAA (open squares), PIFET (circles), TGFETs (triangles), DGFET (diamonds) and planar FDSOI (squares). Model (lines) and simulations (symbols)

Semi-Empirical Design-Oriented Model for Multi-Gate MOSFETs

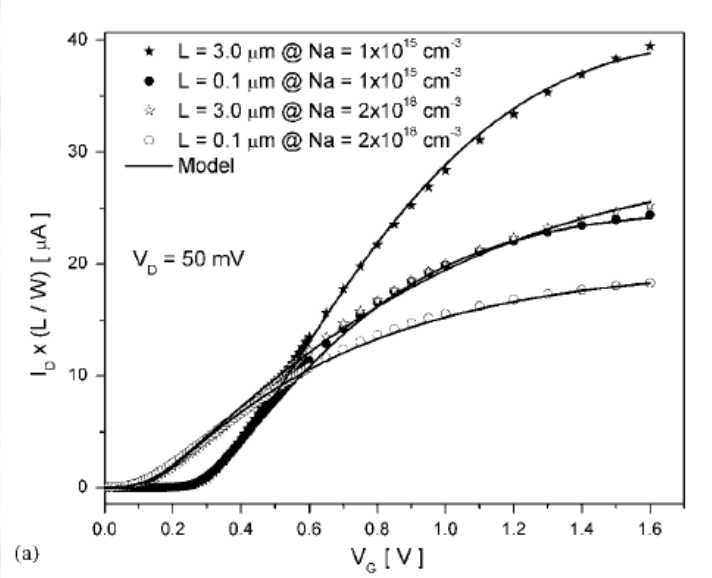
Model developed as a collaboration between UCL (Belgium), URV (Spain) and CINVESTAV (Mexico).

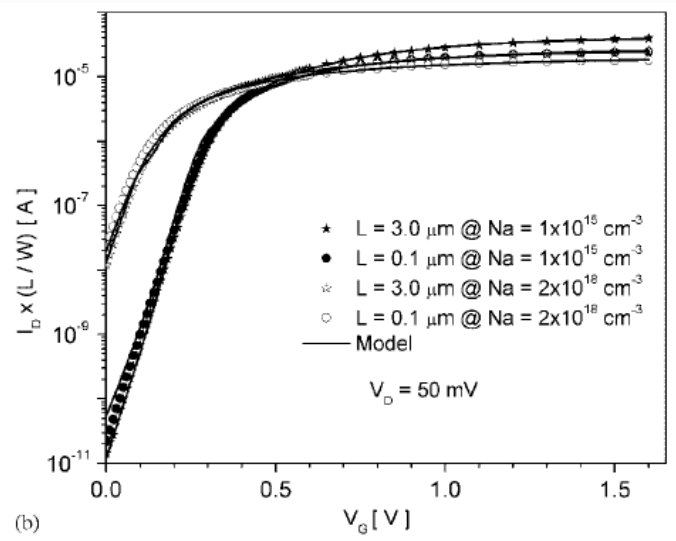
Model dedicated to the simulation of analog and mixed signal circuits using DG MOSFETs, than can also be applied to FinFET as well as trigates structures with a narrow width fin, by appropriately fitting the parameters.

The model equations are based on **analytical expressions of the potentials**, that allow continuity in all operation regions for undoped and doped silicon layers, up to $N_A=2\cdot10^{18}cm^{-3}$.

Several effects are taken into account in the model, like geometrical and process related aspects (oxide thickness, width fin, high fin, polysilicon and midgap metal gates), effects of doping profile, mobility effects due to the vertical and longitudinal fields, and short-channel effects due to velocity saturation, channel-length modulation, roll-off and DIBL and temperature effects, by means of semi-empirical equations.

Semi-Empirical Design Oriented DG MOSFET model





Simulated and modeled transfer characteristics for 3 mm and 100nm channel lengths at V_D=50 mV: (a) I-V curves and (b) semilog I-V curves.

Predictive Design Oriented Multi-Gate MOSFET Model

The UdS and EPFL teams developed a strongly physically-based and explicit compact model for lightly doped FinFETs, which has been extended to doped devices.

It is both a predictive and a design-oriented model valid for a large range of silicon Fin widths and lengths, using only a very few number of model parameters.

The model is based on a core charge control model derived from the 1D Poisson's equation, with extensions coming from the remaining 2D/3D Poisson's equation.

The quantum mechanical effects (QMEs), which are very significant for thin Fins below 15 nm, are included in the model as a correction to the surface potential.

Predictive Design Oriented Multi-Gate MOSFET Model

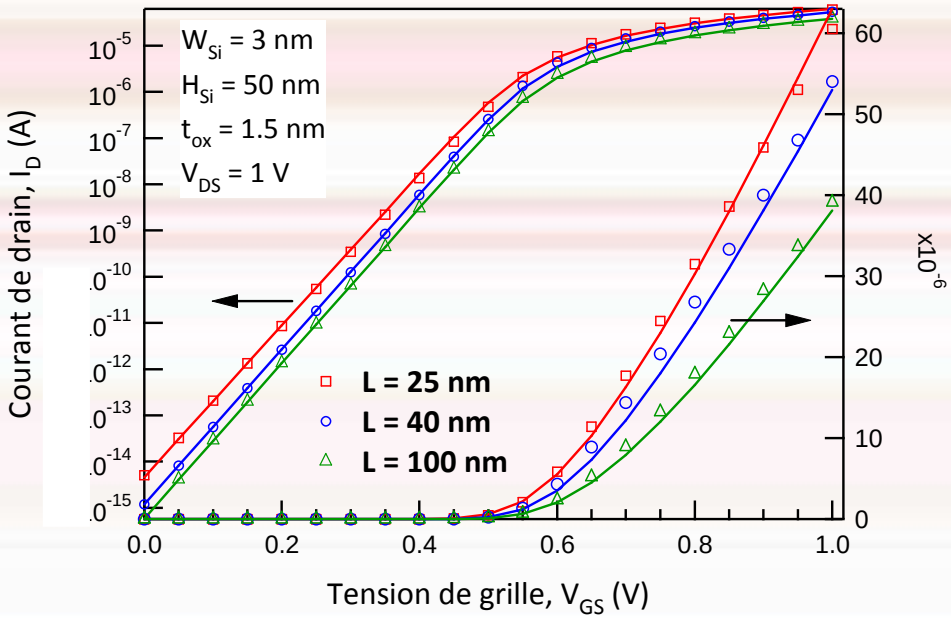
A physics-based 2D/3D approach is followed to model short-channel effects (roll-off), drain-induced barrier lowering (DIBL), subthreshold slope degradation, using hyperbolic functions.

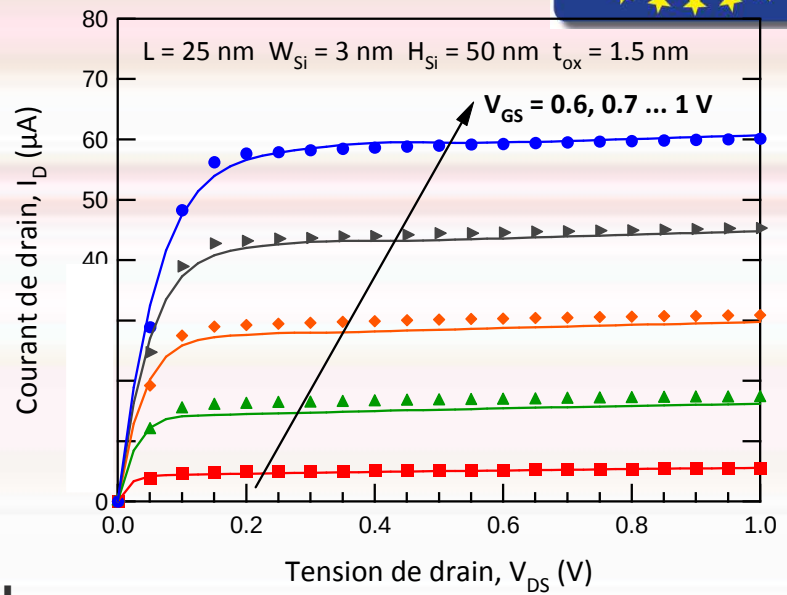
The cross section and back bias modeling scheme developed by URV, seen before, can be incorporated into this model

Velocity saturation, channel length modulation and carrier mobility degradation are also included.

The quasi-static model is then developed and accurately accounts for small-geometry effects as well.

Predictive Design Oriented Multi-Gate MOSFET Model





Validity of the extended model:

Gate length (L): down to 25 nm
Silicon width (W_{Si}): down to 3 nm
Silicon height (H_{Si}): down to 50 nm
Channel doping (N_a): intrinsic to 10^{17} cm^{-3}

nMOS and pMOS

2D/3D Technology-Oriented Multi-Gate MOSFET Modeling

Objectives:

• Establish unified analytical models for nanoscale MugFETs (multigate MOSFETs) including FinFET and GAA devices The model was developed by UniK and URV

Procedure :

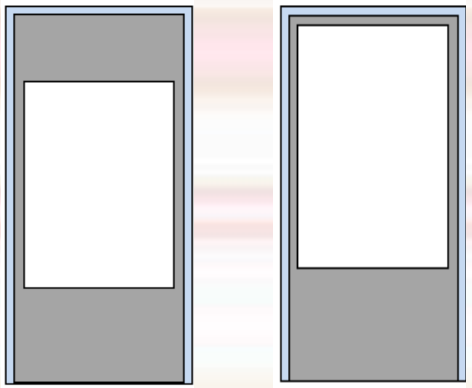
• Decompose Poisson's equation into a Laplace equation and a residual Poisson's equation (superposition principle)

Capacitive inter-electrode effects

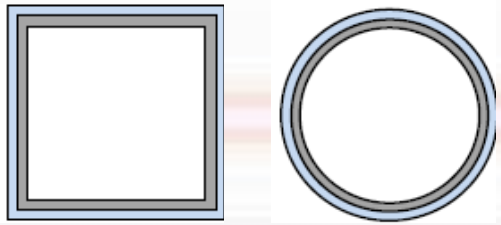
- From 2D/3D Laplace equation determine potential distribution associated with capacitive inter-electrode coupling.
- Use this to calculate *subthreshold* electrostatics, drain current and capacitances

Near and above threshold

- Apply residual Poisson's equation, boundary conditions, and modeling expressions to determine *self-consistent* device properties



Schematic representation of 2D cut-plane of DG FinFET and trigate FinFET respectively



Schematic representation of 2D cut-plane of quad- and cylindrical GAA devices respectively

2D/3D Technology-Oriented Multi-Gate MOSFET Modeling

The final model is based on the use of *isomorphic modeling* expressions for the potential distribution in (*x,y*) cross sections perpendicular to the source-drain *z* axis.

In subthreshold, this allows the complete potential distribution in the device body to be obtained based on the Laplace equation.

Short-channel effects are included by introducing auxiliary boundary conditions, such as the device center potential and the electrical field at the source center, derived analytically from the conformal mapping analysis

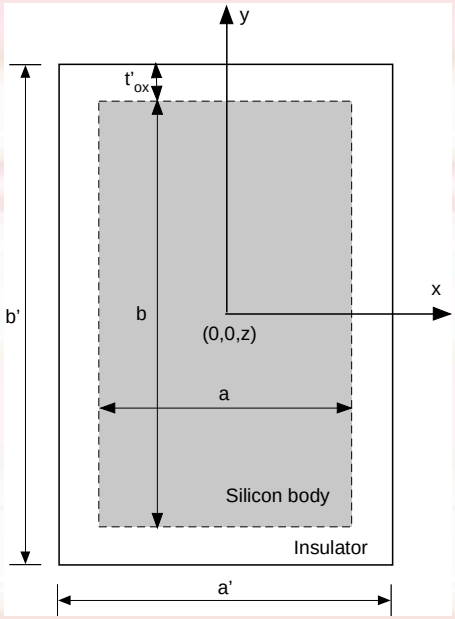
A similar procedure, again using isomorphic modeling expressions, can also be applied to strong inversion by invoking Poisson's equation.

Starting from a rectangular gate structure, the present modeling can be generalized to include FinFETs, trigate, square gate, DG, and even circular gate devices, laying the groundwork for a unified, compact modeling framework for a wide range of multigate MOSFETs.

2D/3D Technology-Oriented Multi-Gate MOSFET Modeling

We first consider a MugFET with a rectangular (x,y) cross-section of silicon widths a and b, for which we write the potential distribution as a 'power expansion' of the following isomorphic form,

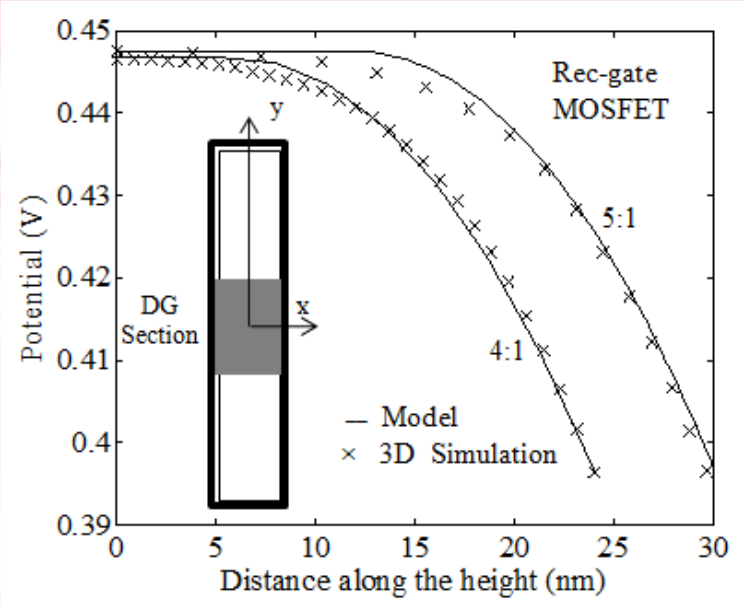
$$\hat{\phi}(x,y,z) = \hat{\phi}(0,0,z)\sum_{i=1}^{n}\alpha_i\left[1-\left(\frac{2x}{a'}\right)^{2i}\right]\left[1-\left(\frac{2y}{b'}\right)^{2i}\right]$$



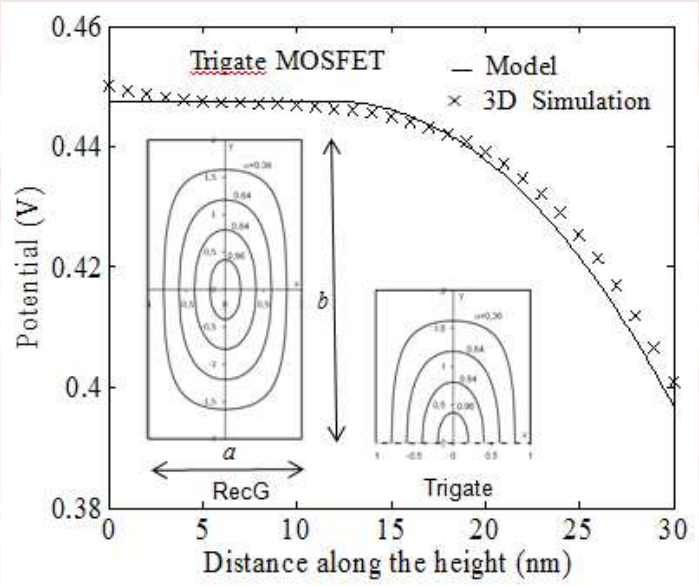
Here $a' = a + 2t'_{ox}$, $b' = b + 2t'_{ox}$ and $t'_{ox} = t_{ox}\varepsilon_{si}/\varepsilon_{ox}$ is an equivalent silicon layer that represents the electrostatic effect of the true gate insulator

$\hat{\varphi}(x,y,z)$ is the body potential relative to the gate interface.

FinFET modeling

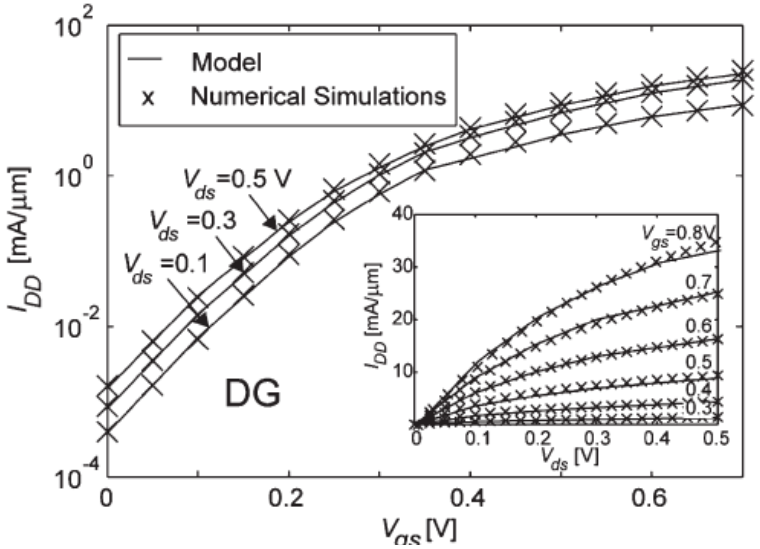


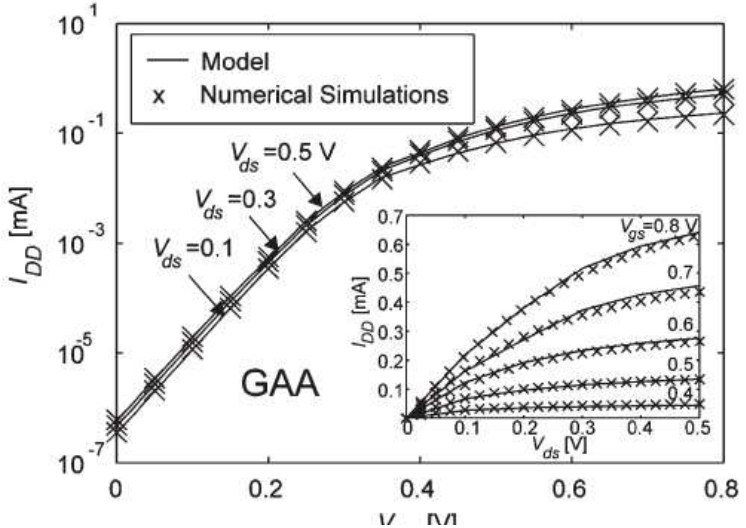
Modeled potential compared to numerical simulations along the height (y) direction for rec-gate devices with $\kappa = 4$ and 5, V_{ds} = 0 V, V_{gs} = – 0.1V.

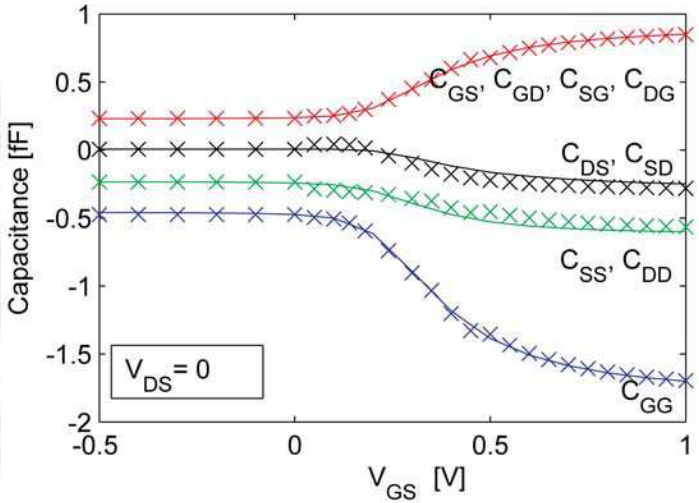


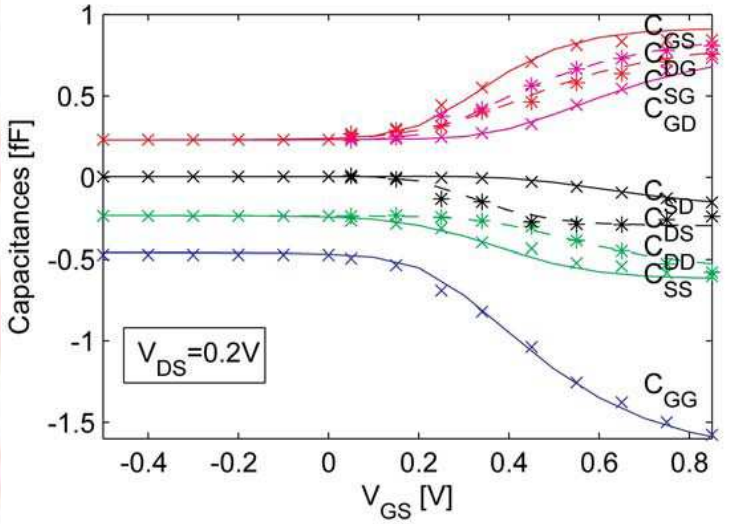
Modeled potential compared to numerical simulations along the height direction for a trigate device. Aspect ratio of original rec-gate device: 5:1. V_{ds} = 0 V, V_{gs} = – 0.1V

Drain current and capacitance results









Conclusions

- Analytical solution of the 2D Laplace's equation under threshold in the case of TGFETs, PiFETs, and OmegaFETs.
- Definition of a threshold voltage model for TGFETs/PiFETs/OmegaFETs, for all type of dimensions (excluding the quantum regime), for NMOS/PMOS, in all regimes of the back-gate (including the two threshold voltages in the 'back-interface inversion' regime).
- Validation of the model with numerical simulations and experimental measurements.

- Analytical solution of the 3D Laplace's equation under threshold in the case of TGFETs, and PiFETs.
- Analytical model for short channel characteristics (SS, DIBL).
- Expression for the device scalability of MuGFETs.

Conclusions

Under the framework of the “COMON” EU Project, compact models for Multi-Gate MOSFETs, HV MOSFETs and HEMTs have been developed.

By the end of “COMON” (Nov 2012) several models will be completed and ready for standardization:

Three Multi-Gate MOSFET models:

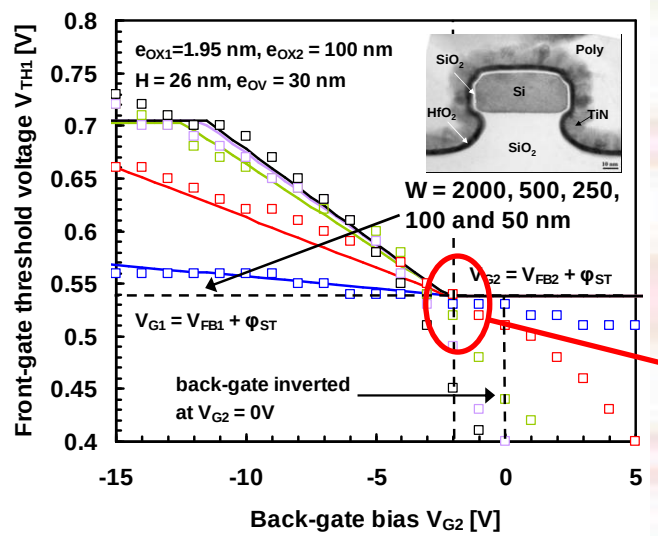
1) Purely design-oriented model

2) Predictive and design-oriented model

3) Predictive technology-oriented model

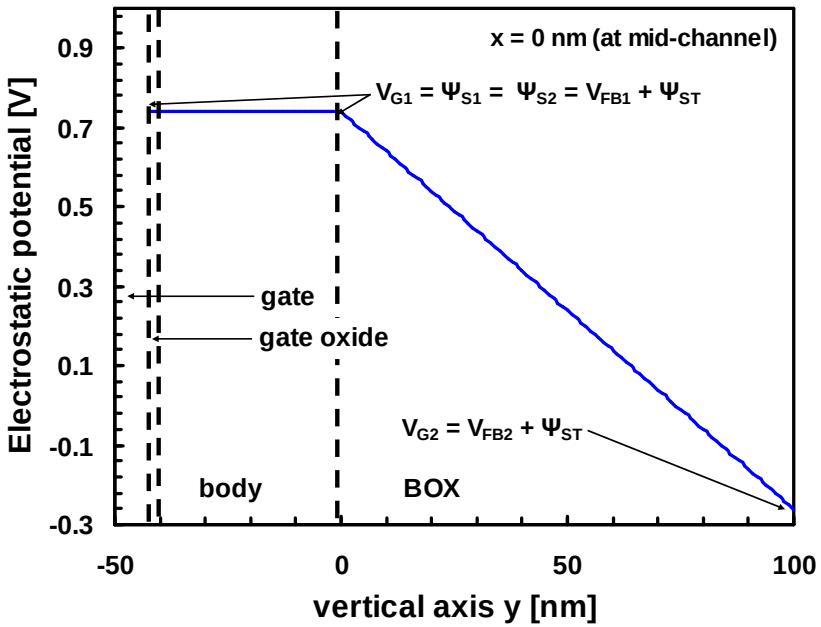
Thank you for your attention!

Invariant point



- Invariant point predicted by the model experimentally observed
- Invariant point occuring for $V_{G1} = V_{FB1} + \varphi_{ST}$ and $V_{G2} = V_{FB2} + \varphi_{ST}$

Invariant point



Model of the potential at mid-channel (x=W/2) for $V_{G2} = V_{FB2} + \varphi_{ST}$ and $V_{G1}=V_{TH1}=V_{FB1}+\varphi_{ST}$

- Compensation of the back-gate induced potential drop
- Flat potential in the channel
- Potential insensitive to channel width and height W and H

Interesting solution to alleviate the threshold voltage variations due to the process variability of W and H.