BSIM-IMG: Surface Potential based UTBSOI MOSFET Model

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UC Berkeley

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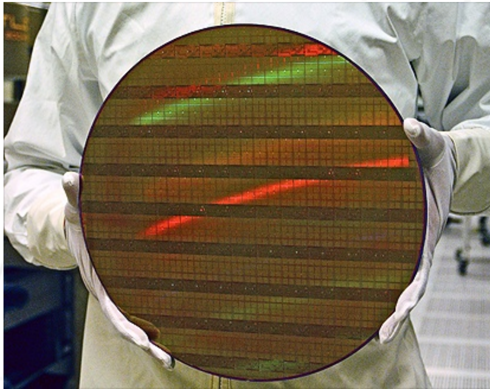
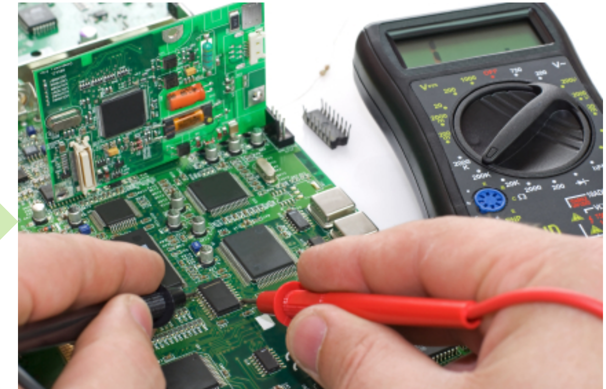
The Nano-Tera Workshop on the Next Generation MOSFET Compact Models, EPFL, Switzerland.

SPICE Transistor Modeling for Circuit Simulation



Medium of information exchange



- **Simulation Time**
  - **~ 10μs per DC data point**
  - **No complex numerical method allowed**
- **Accuracy requirements**
  - **~ 1% RMS Error after fitting**
- **Excellent Convergence**
- **Example: BSIM4**
  - **25,000 lines of C code**
  - **200+ parameters**
  - **Open-source software implemented in all EDA tools**

BSIM Family of Compact Device Models

1990 1995 1998 2000 2005 2010

BSIM3

BSIM4

Conventional MOSFET

New

BSIM6

Silicon on Insulator MOSFET

BSIMSOI

BSIM-MG

Multi-Gate MOSFET

L
Gate
Src
Drn
Substrate

L
Gate
Src
Drn

L
Gate
Src
Drn
Gate

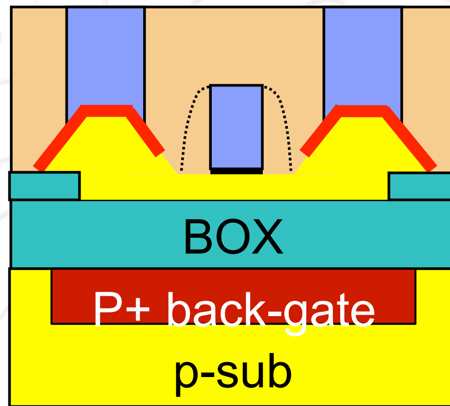
BSIM: Berkeley Short-channel IGFET Model

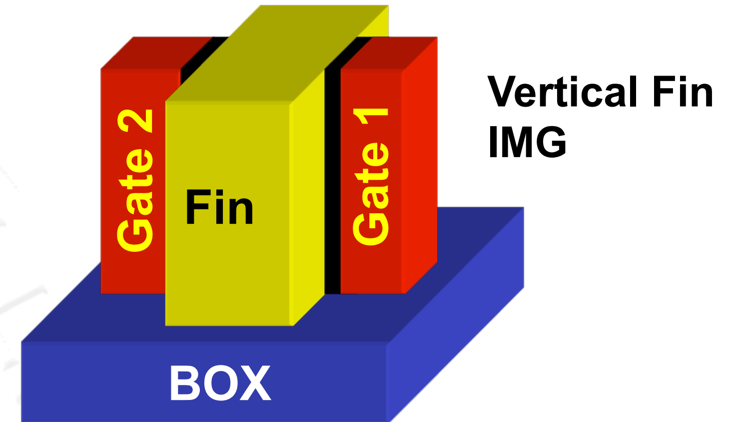
Versatile Multi-Gate Compact Model: BSIM-MG

BSIM-IMG

UTBSOI

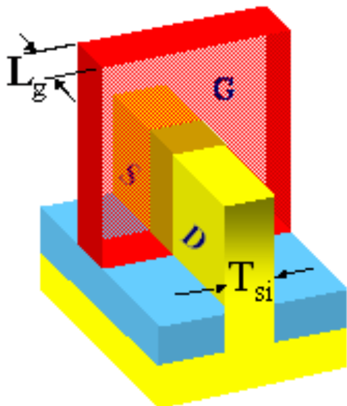
BG-ETSOI

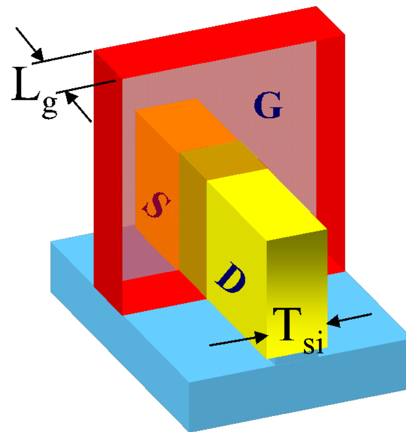




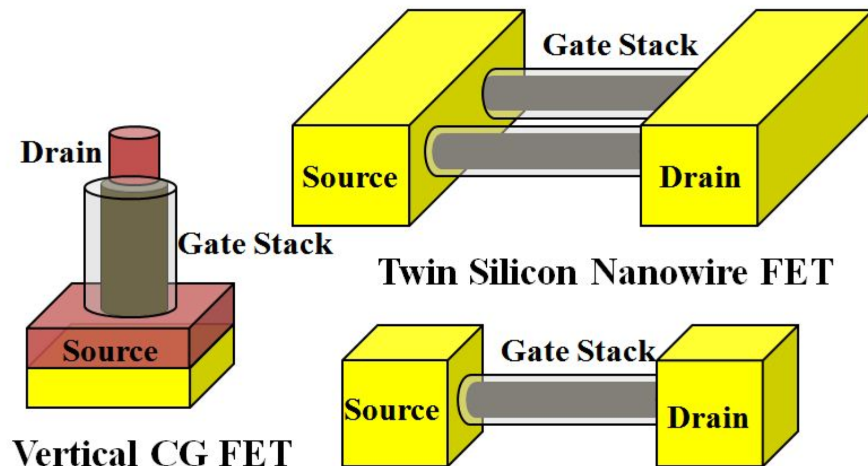
Vertical Fin IMG

BSIM-CMG

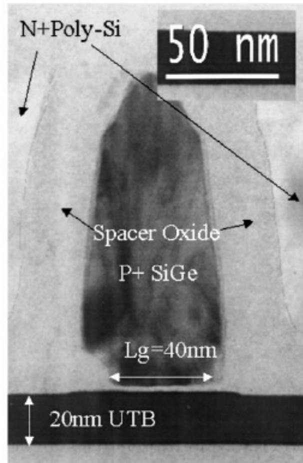


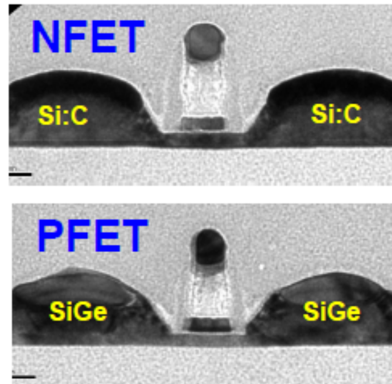


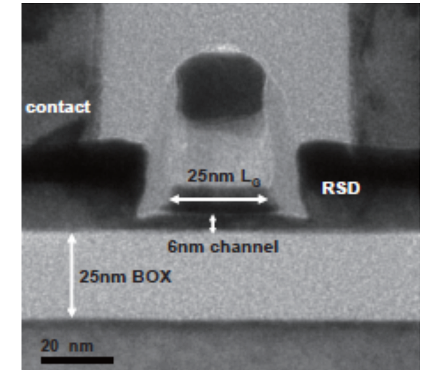
FinFETs on Bulk and SOI Substrates



Thin-body SOI Devices



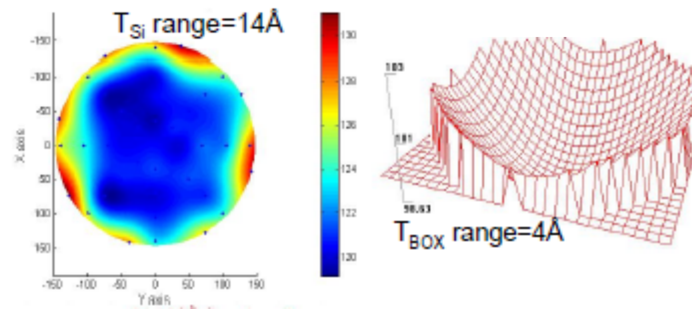




UTBSOI	**ETSOI**	**UT2B**	**UTBB**
Y. Choi et al. EDL 2000	K. Cheng et al. IEDM 2009	F. Andrieu et al. VLSI 2010	Q. Liu et al. VLSI 2011
(UC Berkeley)	(IBM)	(CEA-LETI)	(ST)

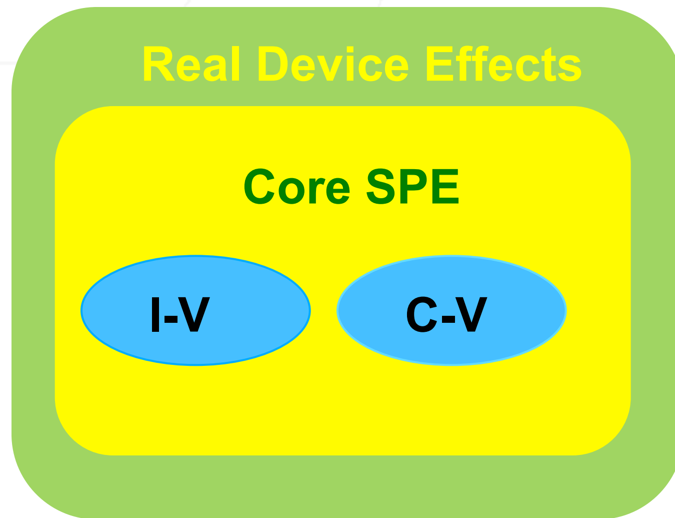
Wafer Uniformity (SOITEC):

F. Andrieu et al., VLSI 2010

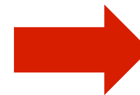


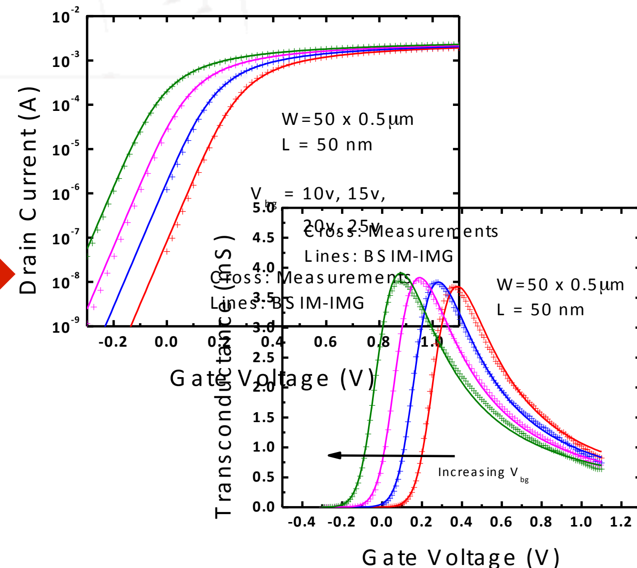
Executive Summary/ Outline : BSIM-IMG

- Production Ready Compact Model for FDSOI
- Physical Core Model
- Palette of Real Device Effects
- Validated to Hardware Silicon Data
- Synchronized with EDA Vendors Tools



BSIM-IMG





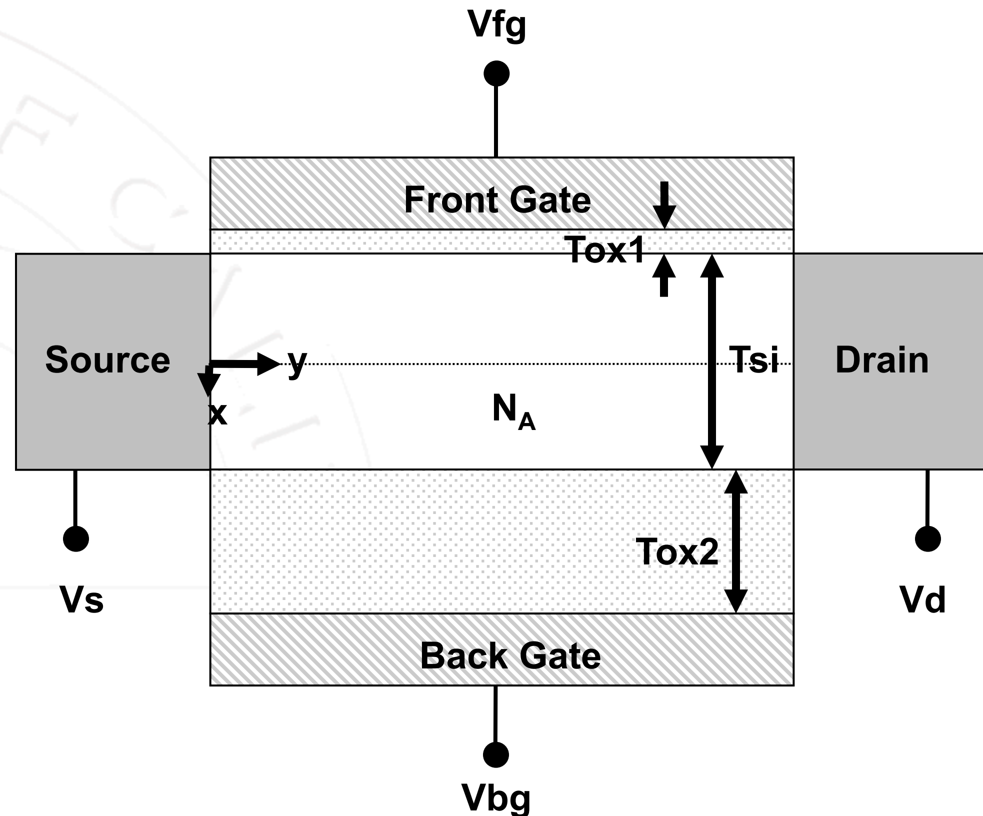
Validation

Outline

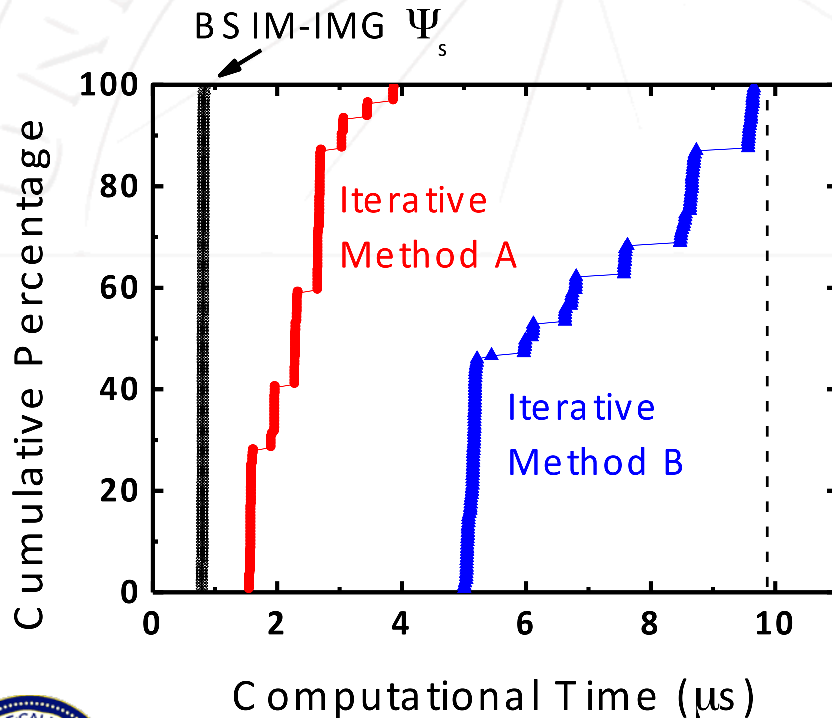
- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Model Validation & QA
- Future Research
- Conclusion

Independent-gate Device Structure: BSIM-IMG

- **Asymmetric structure**
  - Different Gate Work-functions
  - Allows dissimilar Gate Potentials
  - Different Oxide thickness and Material !
- **Captures important features**
  - Threshold Voltage tuning through Back-Gate
  - Multi-V_{th} technology



Computationally Efficient Core



- **Efficient Non-iterative Surface Potential calculation**
  - **Investigated NR, Shooting Secant etc.**
- **Surface potential needs to solved at least twice - Source and Drain side**
  - **Obtain ψ_s / Q_{is} and ψ_d / Q_{id}**

D. Lu et al., SSE 2011

Surface Potential Derivation

- Quasi-Fermi level at the source is taken as a reference for the potential (ψ).

$$\psi = -\frac{E_c - E_f(source)}{q}$$

- Start from the Poisson's equation

$$\varepsilon_{si}\frac{d^2\psi(x,y)}{dx^2} = qN_c \exp\left(\frac{q(\psi(x,y) - V_{ch}(y))}{kT}\right)$$

- The continuity of displacement field at the front and back interfaces gives the following relation of the surface electric fields $(E_{s1} = -\frac{d\psi}{dx}\Big|_{x=-Tsi/2}$ and $E_{s2} = -\frac{d\psi}{dx}\Big|_{x=Tsi/2})$ and surface potentials:

$$C_{ox1(2)}(V_{fg(bg)} - \Delta\Phi_{1(2)} - \psi_{s1(2)}) = \varepsilon_{si}E_{s1(2)}$$

Surface Potential Derivation (Contd.)

- Multiplying both sides of Poisson's Eq. by $\frac{d\psi}{dx}$ and integrating yields

$$E_{s1}^2 - E_{s2}^2 = \frac{2qN_c V_{th}}{\varepsilon_{Si}}\left\{\exp\left(\frac{\psi_{s1}-V_{ch}}{V_{th}}\right) - \exp\left(\frac{\psi_{s2}-V_{ch}}{V_{th}}\right)\right\}$$

- Replacing E_{s1} with ψ_{s1}

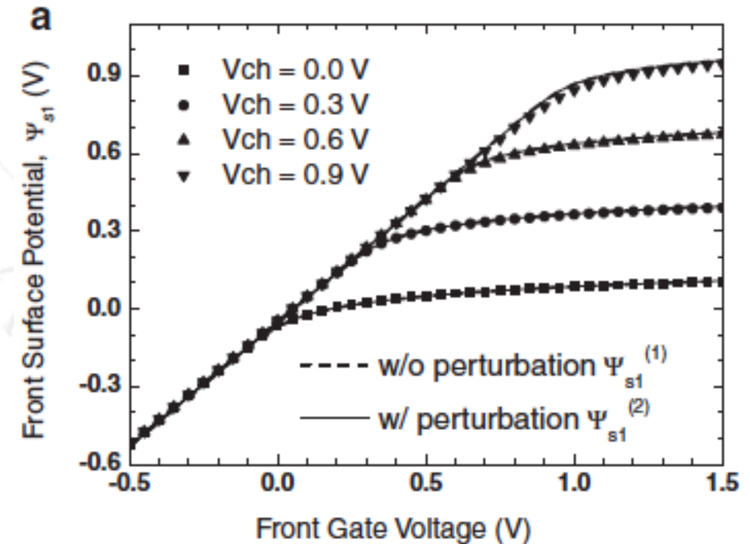
$$\left(\frac{C_{ox1}(V_{fg}-\Delta\Phi_1-\psi_{s1})}{\varepsilon_{si}}\right)^2 - E_{s2}^2 = \frac{2N_c kT}{\varepsilon_{si}}\exp\left(\frac{q(\psi_{s1}-V_{ch})}{kT}\right)$$

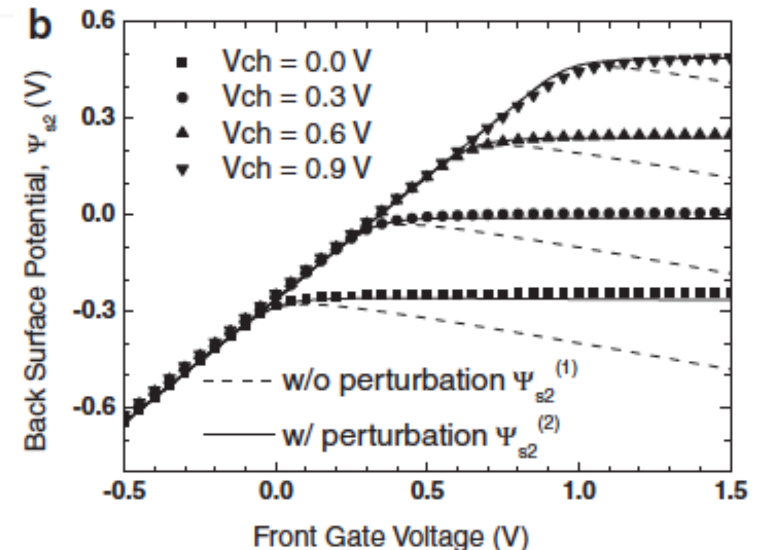
- E_{s2} approximation

$$E_{s2} = \frac{(V_{fg}-\Delta\Phi_1)-(V_{bg}-\Delta\Phi_2)}{\frac{\varepsilon_{si}}{\varepsilon_{ox}}(T_{ox1}+T_{ox2})+T_{si}}$$

- Using perturbation to improve accuracy at strong inversion

$$E'_{s2} = \frac{\psi_{s1}^{(1)}-(V_{bg}-\Delta\Phi_2)}{\frac{\varepsilon_{si}}{\varepsilon_{ox}}T_{ox2}+T_{si}}$$

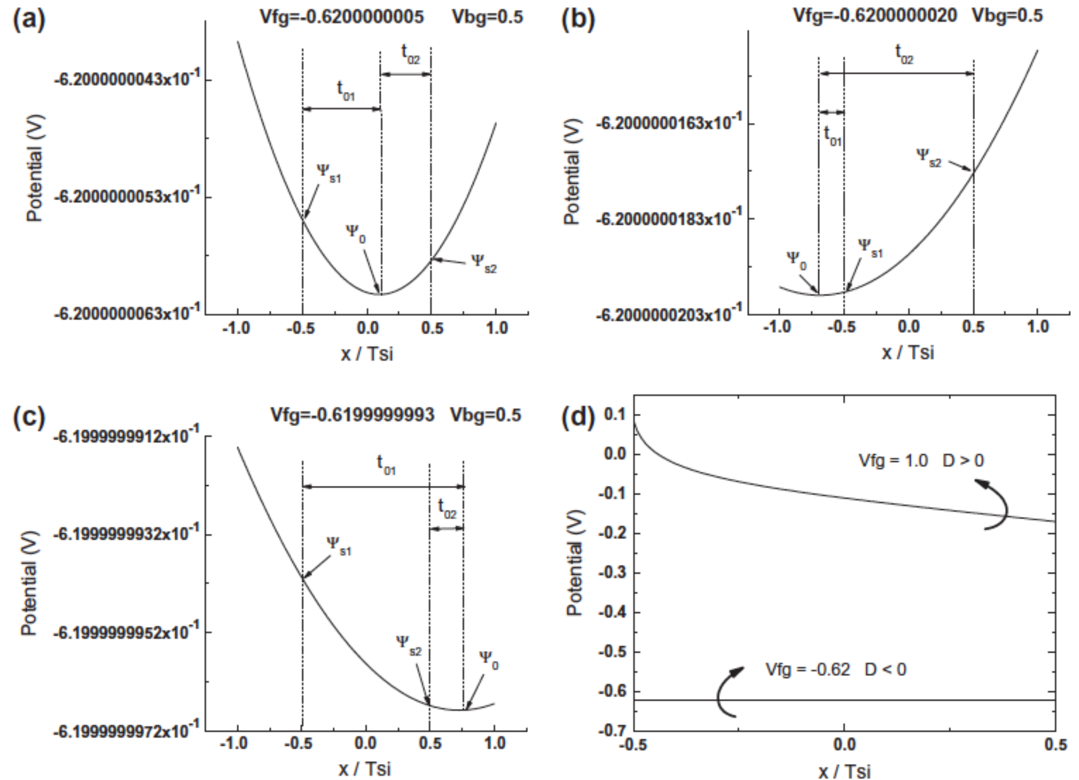




Relating ψ_{s2} with ψ_{s1}

Generalization of Poisson's equation

$$\left(\frac{d\psi}{dx}\right)^2 - A\cdot\exp\left(\frac{q(\psi - V_{ch})}{kT}\right) = D$$



D < 0

$$t_{01} = \left|\left(\frac{2kT}{q\sqrt{-D}}\right)\cos^{-1}\left[\sqrt{-\frac{D}{A}\exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT}\right)}\right]\right|$$

$$t_{02} = \begin{cases} |T_{si} - t_{01}| & E_{s1} > 0 \\ T_{si} + t_{01} & E_{s1} < 0 \end{cases}$$

$$\psi_{s2} = V_{ch} - \frac{kT}{q}\ln\left\{\frac{A}{-D}\cos^2\left[\left(\frac{q\sqrt{-D}}{2kT}\right)t_{02}\right]\right\}$$

$$E_{s2} = -\frac{\partial\psi_{s2}}{\partial t_{02}}$$

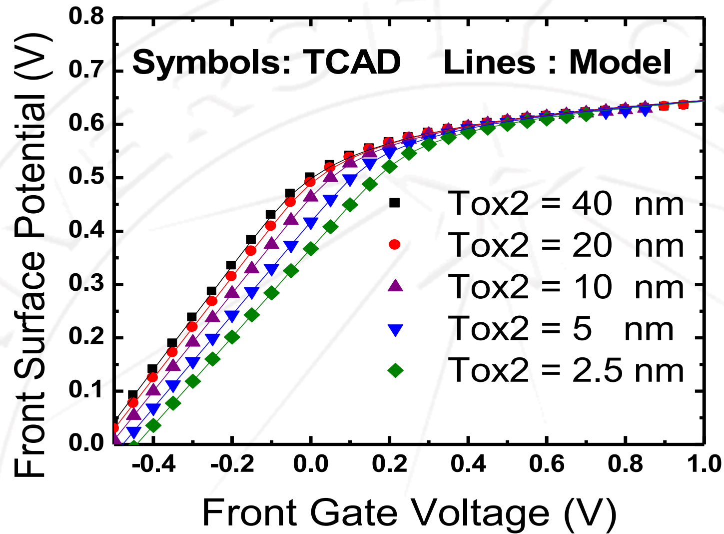
$$Q_{inv} = \varepsilon_s(E_{s1} - E_{s2})$$

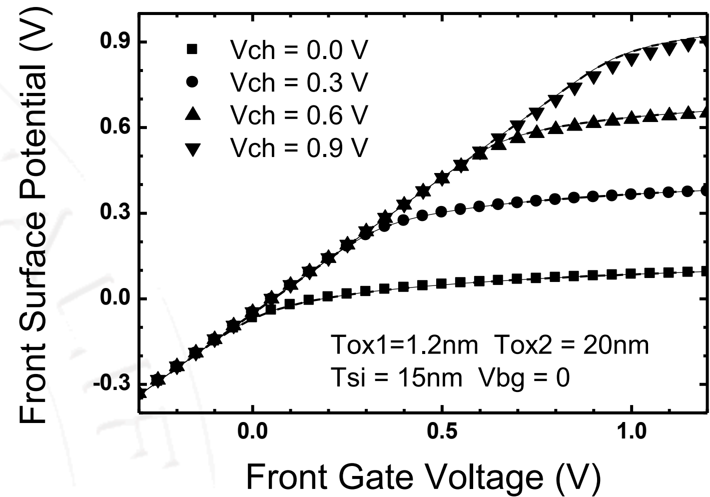
D > 0

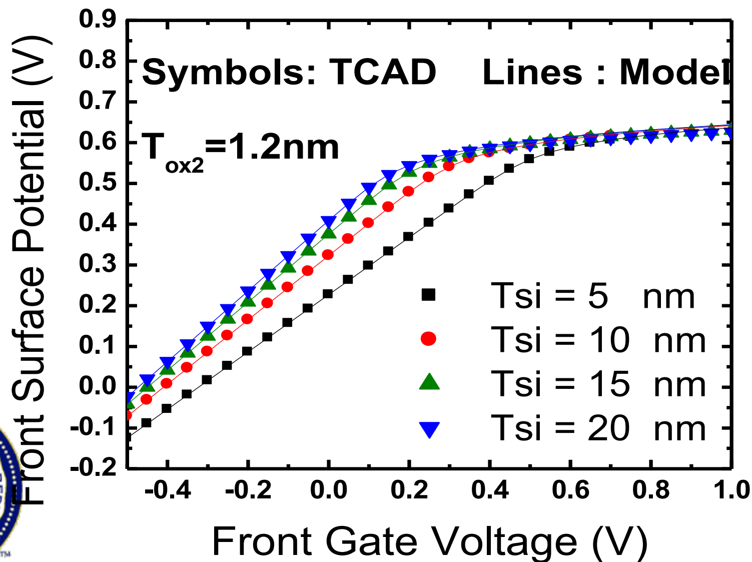
$$\psi_{s2} = V_{ch} + \frac{kT}{q}\ln\left[\frac{D}{A}\left(\frac{2C}{1-C^2}\right)^2\right]$$

$$C = \left[\sqrt{\frac{D}{A}\exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT}\right) + 1} - \sqrt{\frac{D}{A}\exp\left(-\frac{q(\psi_{s1} - V_{ch})}{kT}\right)}\right] \times \exp\left[-\mathrm{sgn}(E_{s1})\frac{q\sqrt{D}}{2kT}T_{si}\right]$$

Surface Potential: Verification with TCAD





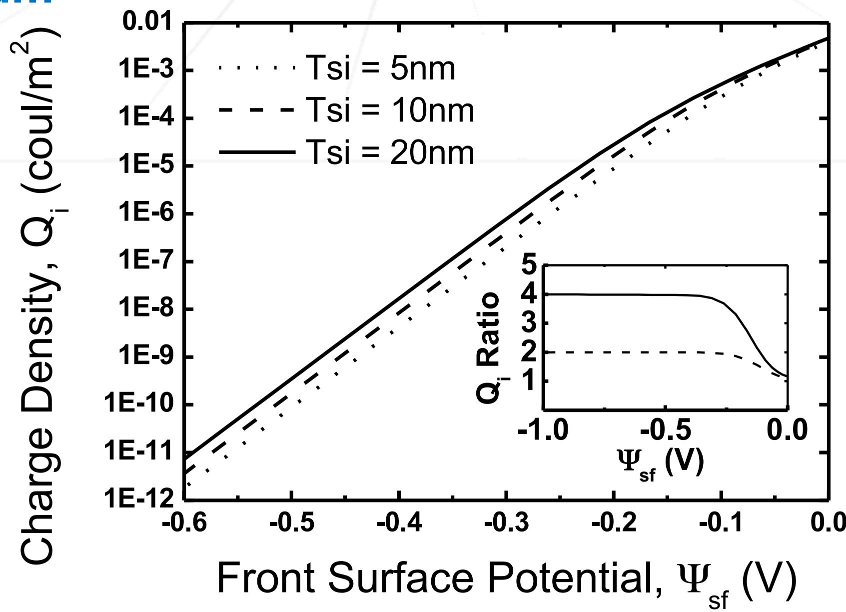


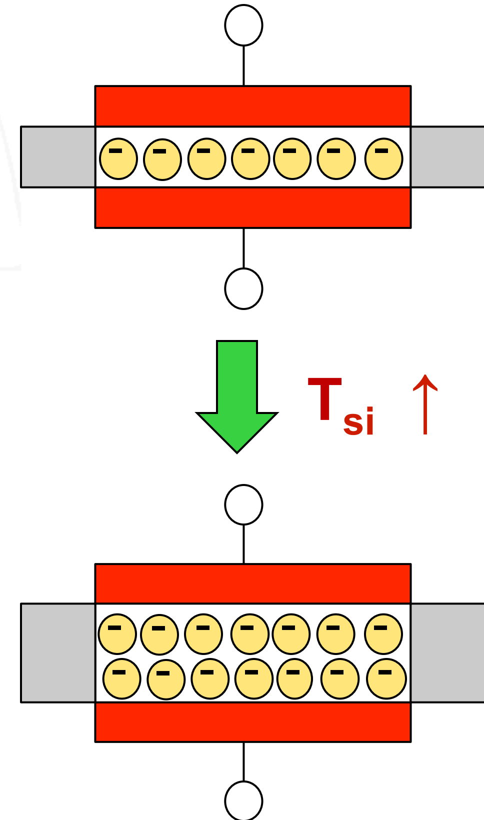
Scalable w.r.t. physical parameters like T_{si}, T_{ox} (front and back) and node voltages etc.

Volume Inversion

- **Preserves Important Property like Volume Inversion**
  - **In sub-threshold (Low field), the charge density Q_i is proportional to the body thickness T_{si}**

T_{oxb} = 10μm





Drain Current Model

- **Drain Current**

$$I_{ds} = \mu \cdot \frac{W}{L} \cdot \left[\frac{Q_{inv,s} + Q_{inv,d}}{2} \left(\psi_{s1,d} - \psi_{s1,s} \right) + \eta \cdot \frac{kT}{q} \left(Q_{inv,s} - Q_{inv,d} \right) \right]$$

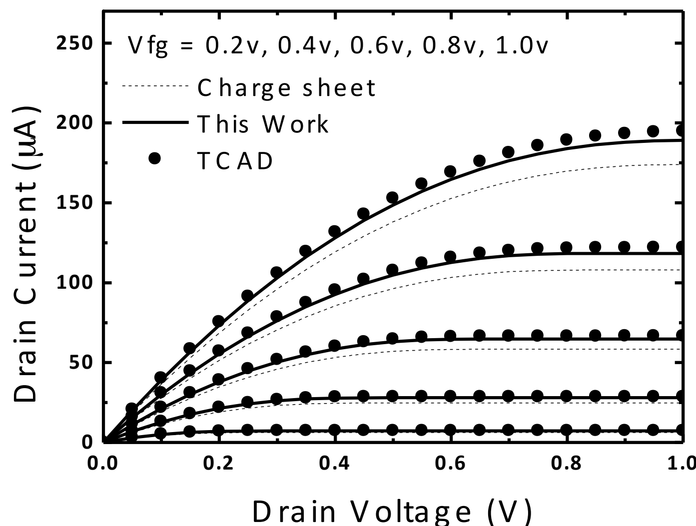
Drift **Diffusion**

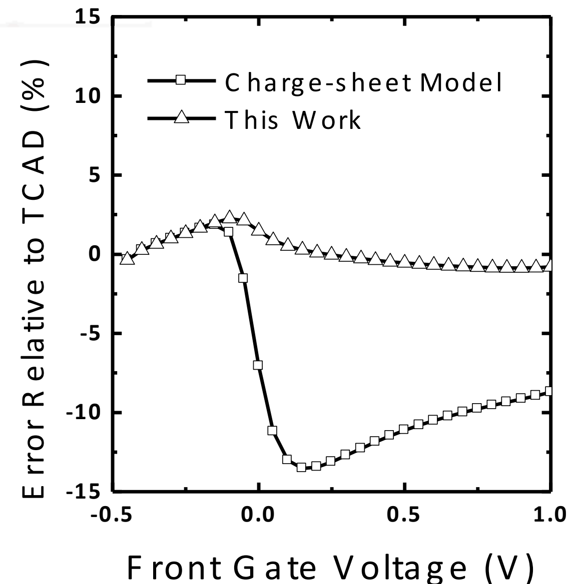
$$\eta = 2 - \frac{2\varepsilon_{si}\overline{E}_{s2}}{\overline{Q}_{inv} + 2\varepsilon_{si}\overline{E}_{s2}}$$

Q_{inv}: inversion carrier density
E_{s2}: back-side electric field
ψ_{s1}: front-side surface potential

No Charge-sheet Approximation

Very high accuracy

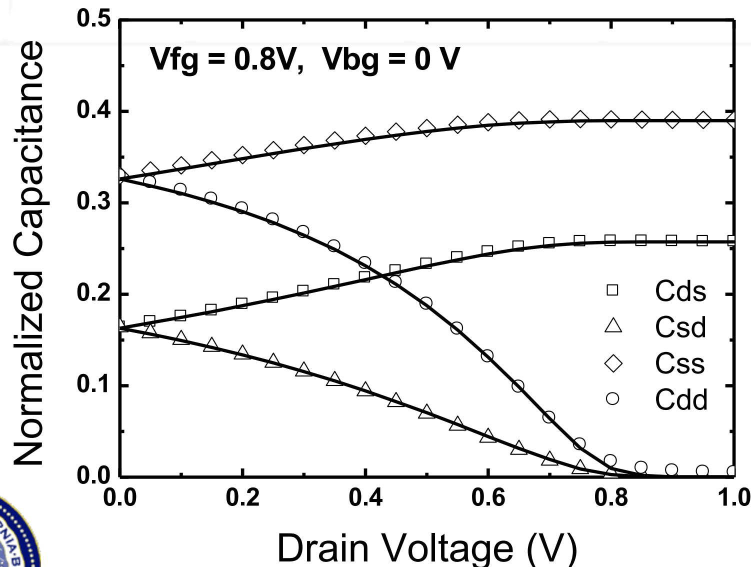


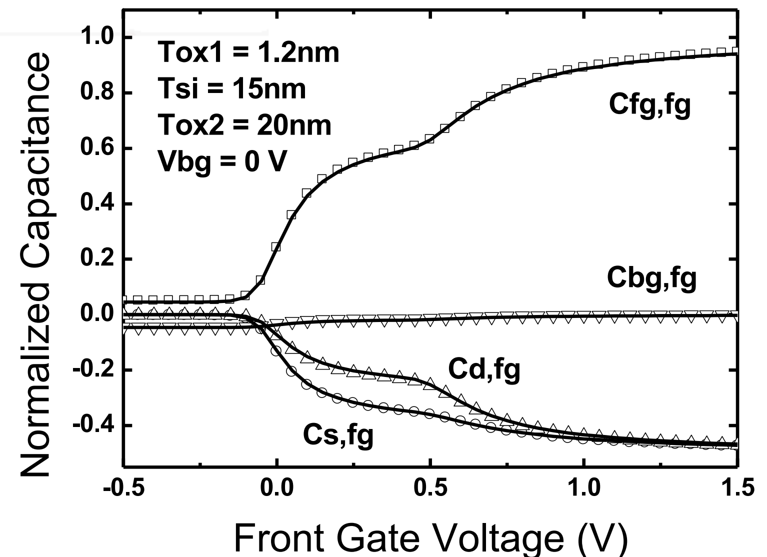


Capacitance Model

- **Model inherently exhibits symmetry**
  - **$C_{ij} = C_{ji}$ @ $V_{ds} = 0$ V**
- **Model overlies TCAD results**
  - **No tuning parameters used**

$T_{oxf} = 1.2$nm, $T_{oxb} = 20$nm, $T_{si} = 15$nm, $V_{bg} = 0$ V



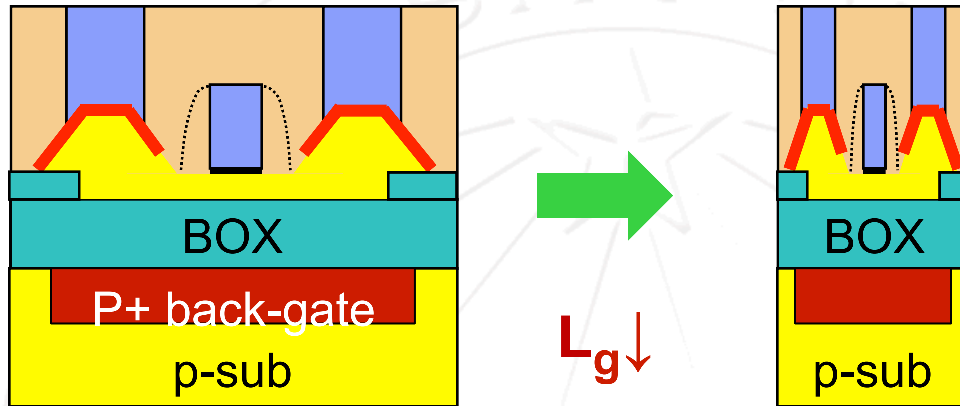


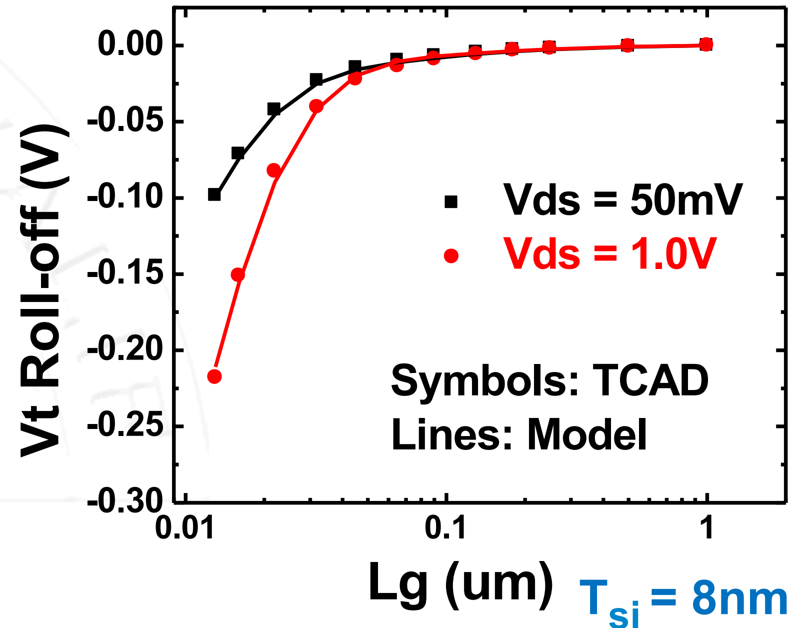
Symbols: TCAD Results; Lines: Model

Outline

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- **Real Device Effects**
- Model Validation & QA
- Future Research
- Conclusion

Short Channel Effects





T_{si} = 8nm

T_{box} = 4nm

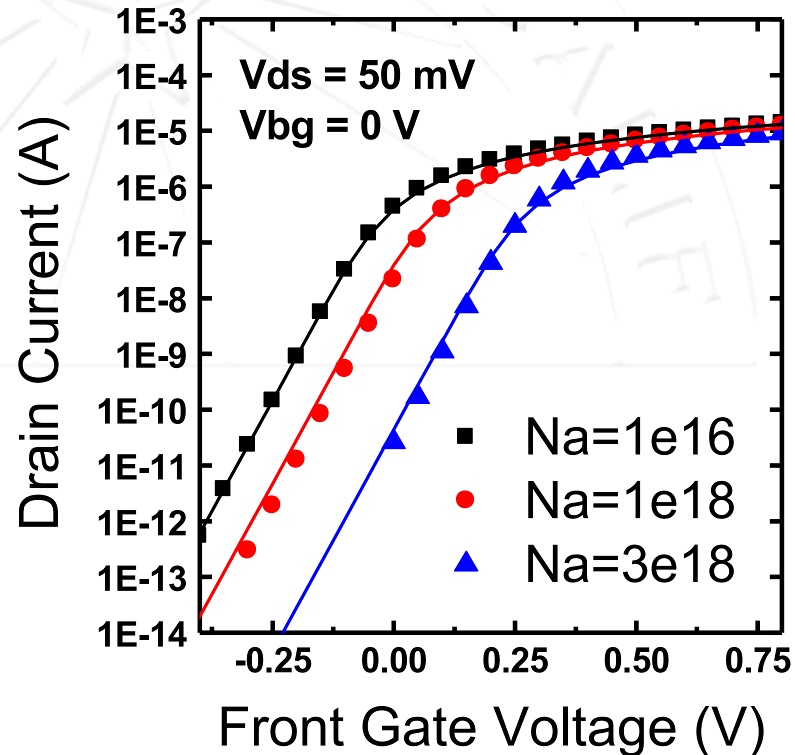
$$\Delta V_{th} = \frac{0.5 \cdot DVT0}{\cosh\left(DVT1 \cdot \frac{L}{\lambda}\right)} \times (V_{bi} - \phi_s) + \frac{0.5 \cdot ETA0}{\cosh\left(DSUB \cdot \frac{L}{\lambda}\right)} \times V_{ds}$$

Scale Length

$$\lambda = \sqrt{\frac{\epsilon_{si}}{2\epsilon_{ox}} \cdot T_{si} \cdot T_{ox1} \cdot \left[1 + \frac{T_{ox2} - T_{ox1}}{T_{ox1} + T_{ox2} + T_{si} \cdot \frac{\epsilon_{ox}}{\epsilon_{si}}}\right]}$$

Doping Dependence

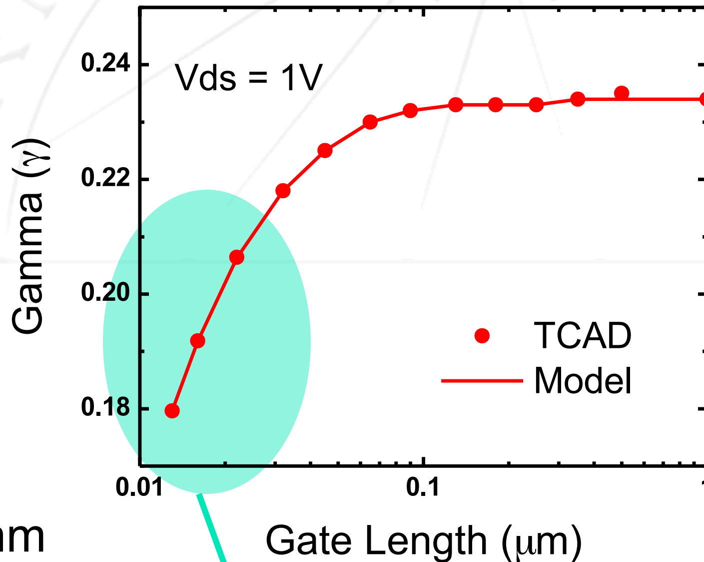
- Threshold voltage shift as function of doping is captured



Length Dependent γ Model

- **Capacitive coupling ratio**

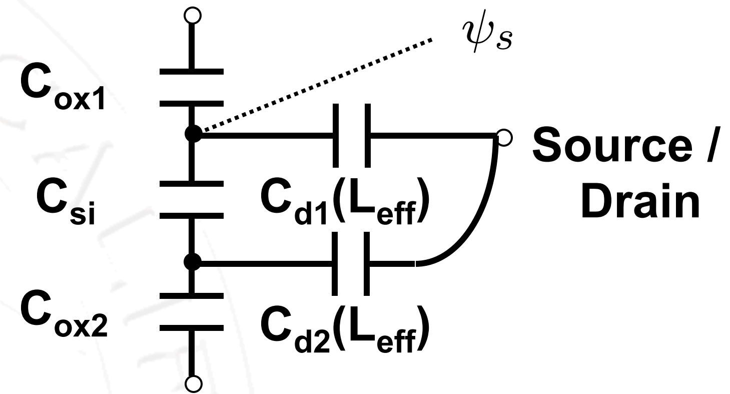
$$\gamma = -\frac{dV_{TH}}{dV_{bg}}$$

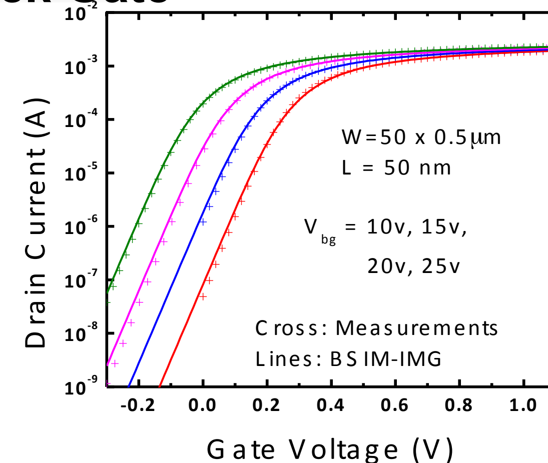


Tsi=8nm

Tbox=4nm

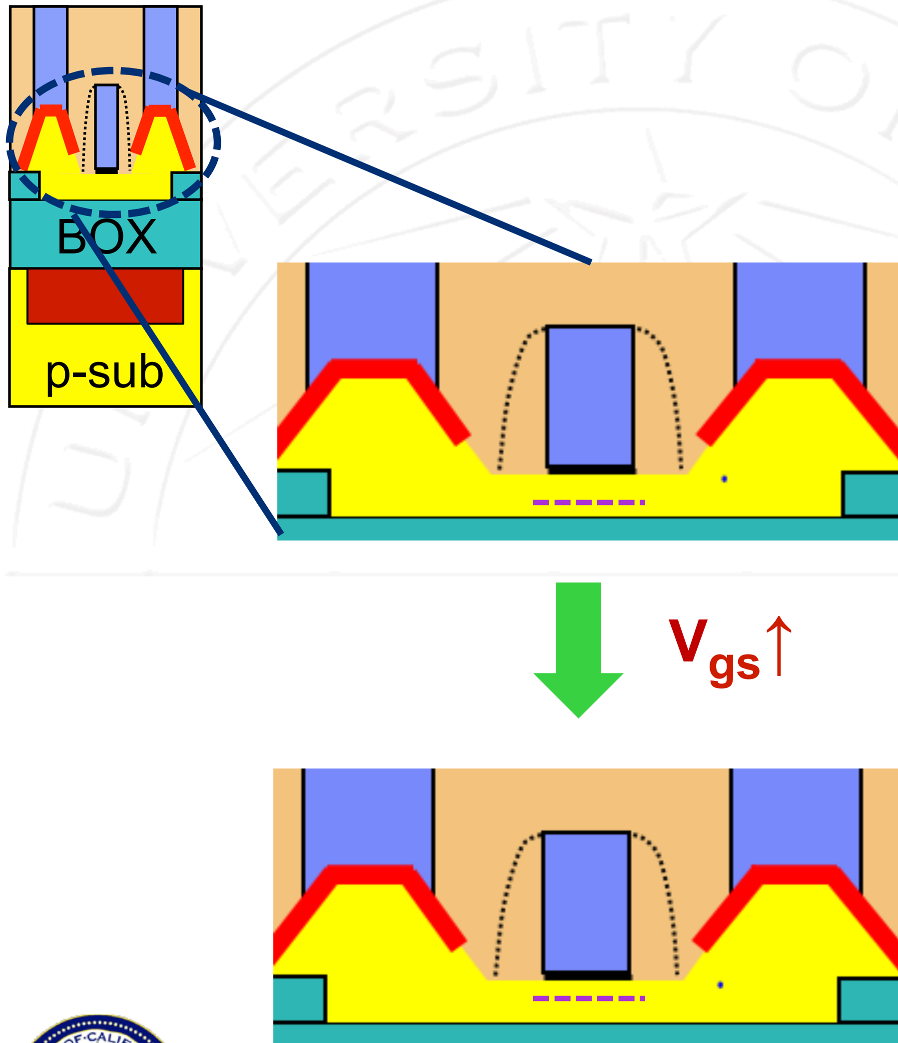
γ degraded at short channel





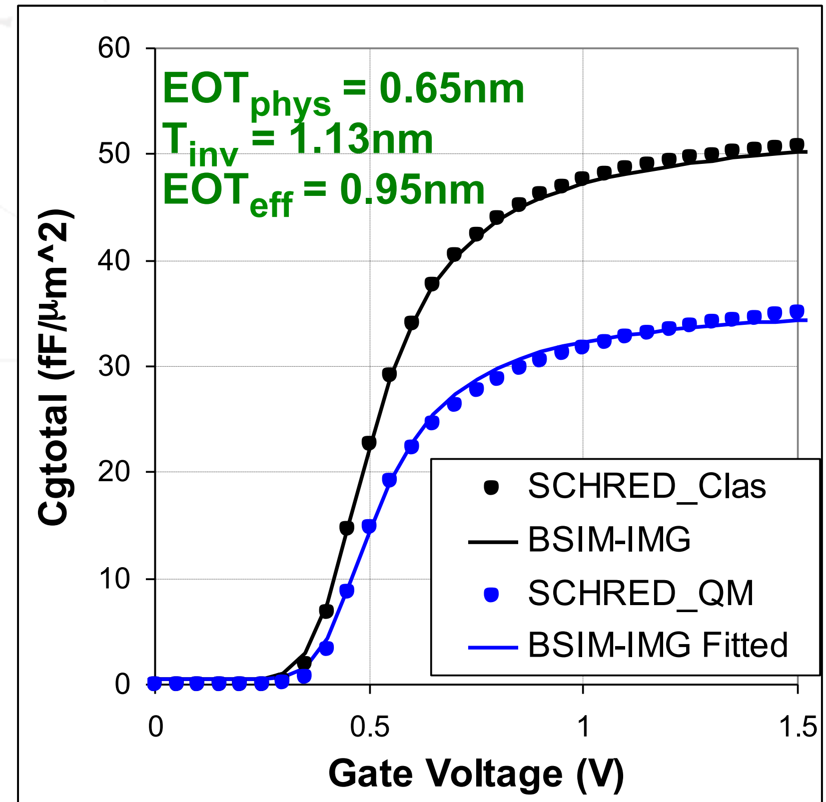
Captures V_{bg} effect in I-V

QM Effect: Inv. Charge Centroid Model



V_{dd} = 0.9 V ; V_{fb} = 28 mV

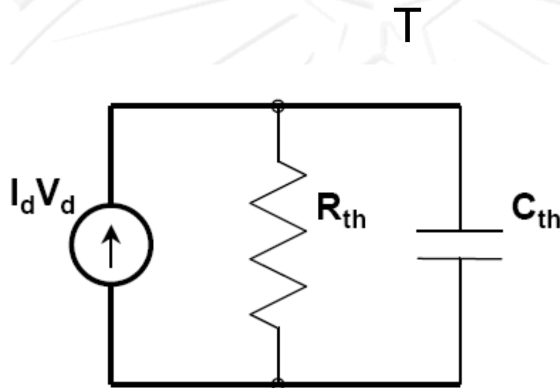
T_{BOX} = 140nm; T_{si} = 6nm; N_{sub} = 1e16 cm^{-3}



Self Heating Model

- **Thermal Node: R_{th}/C_{th} methodology**

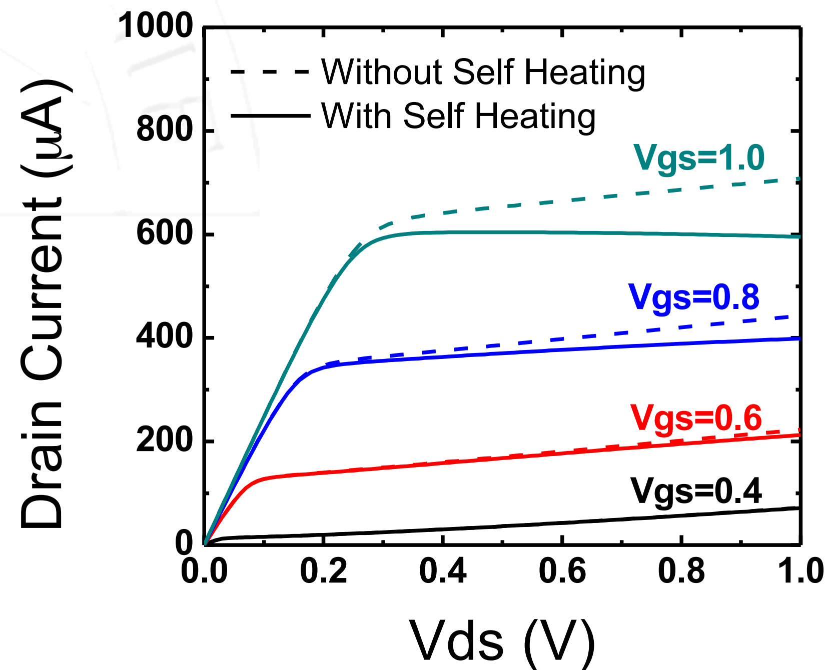
T



- **Relies on Accurate physical modeling of Temperature Effects in the model**

$$R_{th} = \frac{RTH0}{WTH0 + W_{eff}}$$

$$C_{th} = CTH0 \cdot (WTH0 + W_{eff})$$



Real Device Effects

More Effects?

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- Introduction
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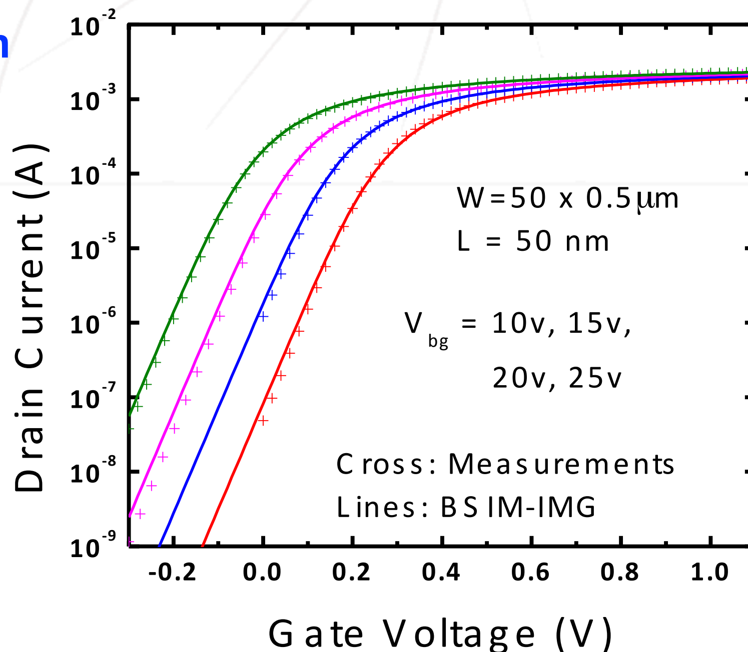
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- **Model Validation & QA**
- Future Research
- Conclusion

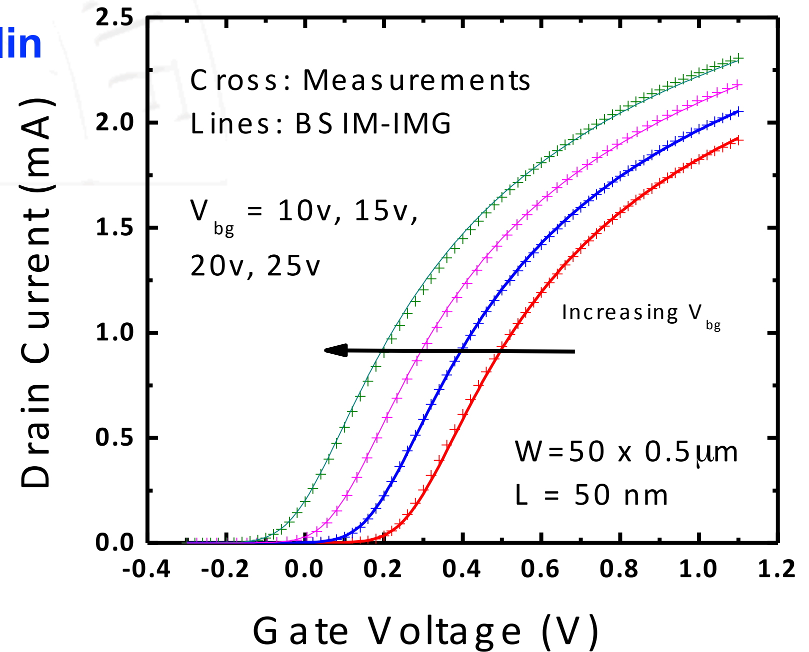
Validation to Hardware Data

- **Device from CEA-LETI**
  - **T_{box}=145nm EOT=1.6nm T_{si}= 8nm W=0.5um x 50**
    L = 50nm N_a=1e15 Φ_{g2} = 5.0 Φ_{g1} = 4.55 (fitted)
  - **V_{bg} = floating, 10V, 15V, 20V, 25V**

$I_{d,lin}$

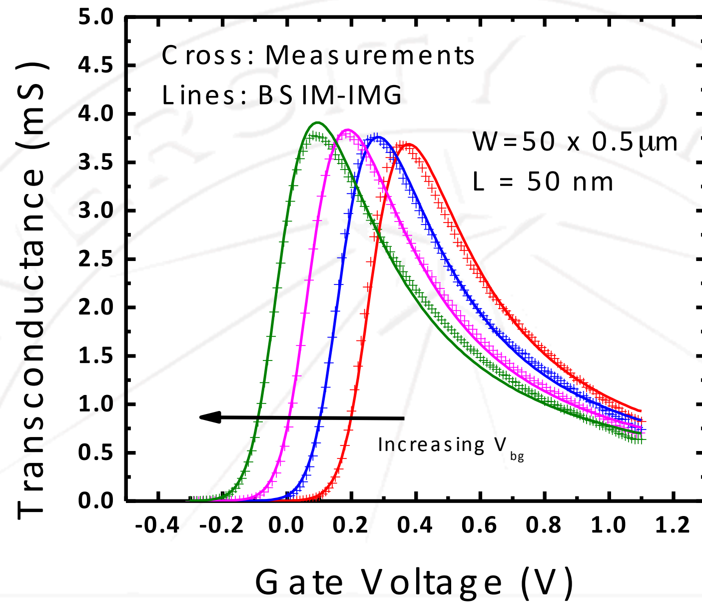


$I_{d,lin}$

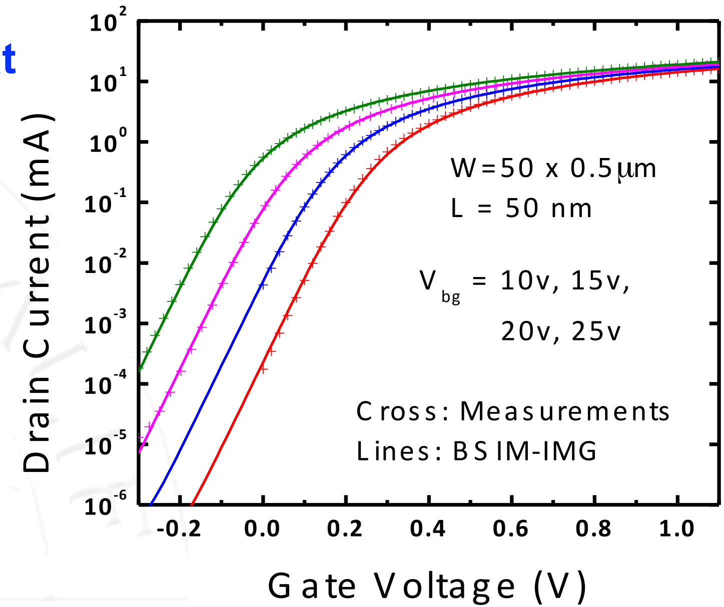


Validation Contd.

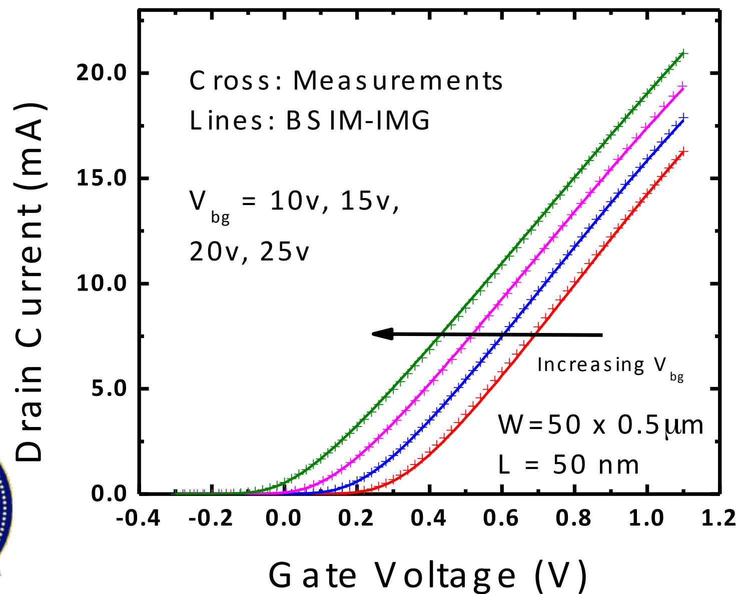
$G_{m,lin}$



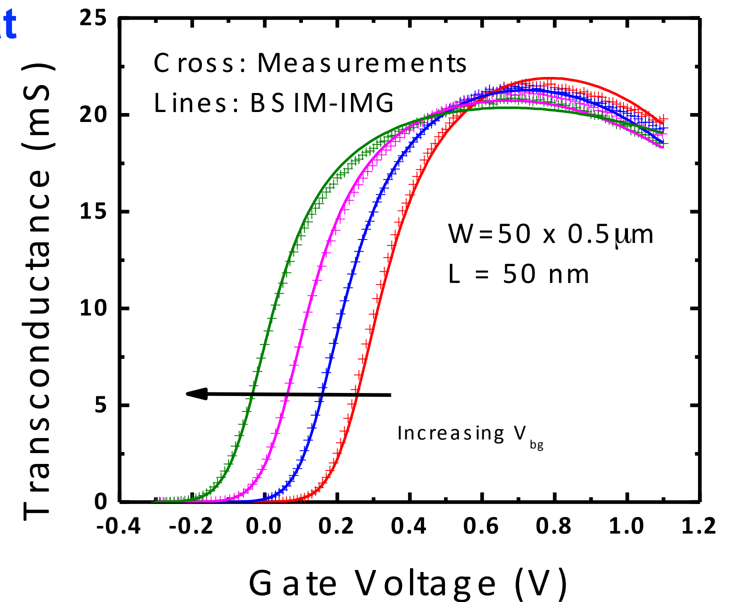
$I_{d,sat}$



$I_{d,sat}$

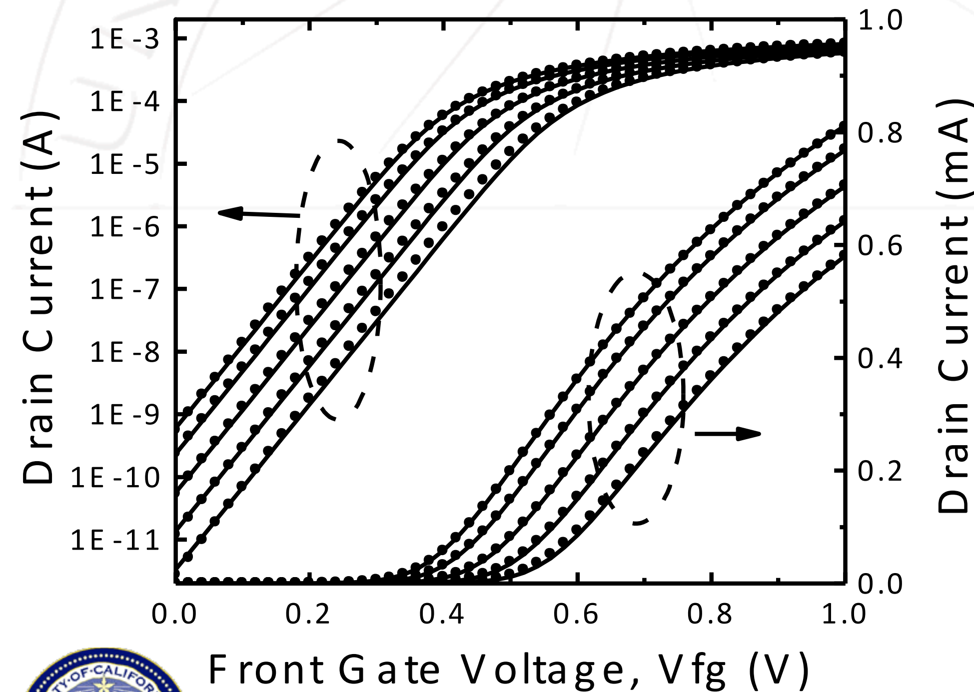


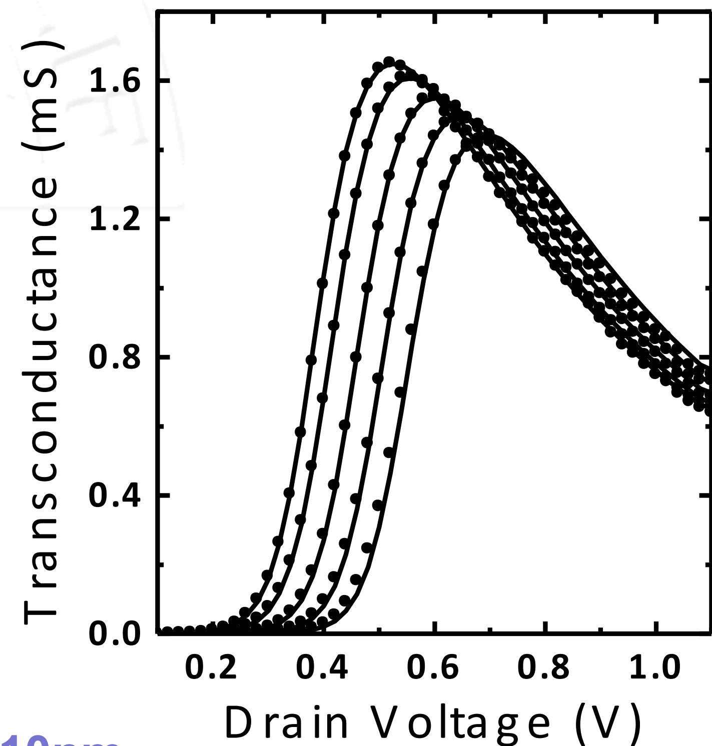
$G_{m,sat}$



Extraction Results : I_d-V_{fg} and G_m-V_{fg} with varying V_{bg}

- I_d-V_{fg} with varying back bias
  - V_{bg}=0, -0.2, -0.5, -0.8, -1.1 V
  - V_{ds}=50mV
- Transconductance (G_m)

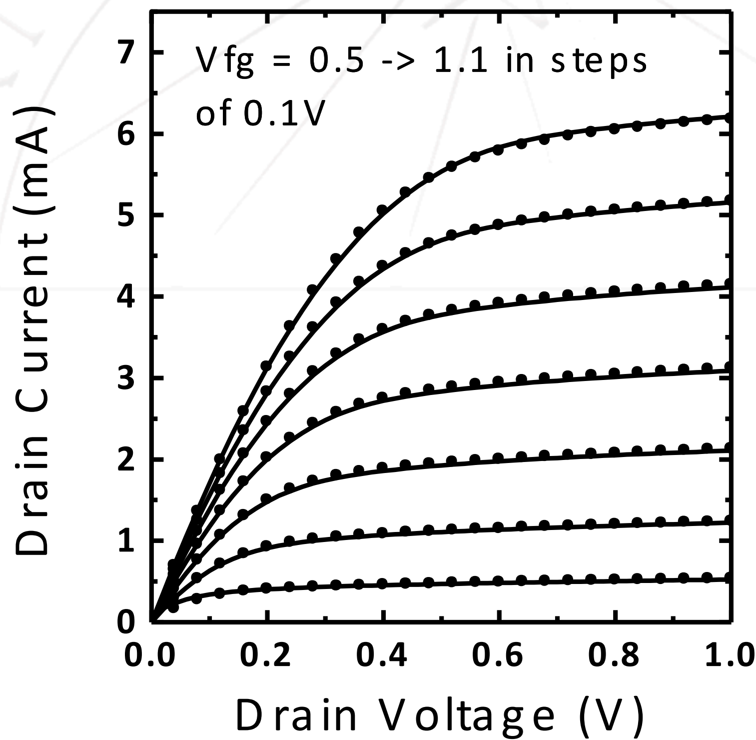




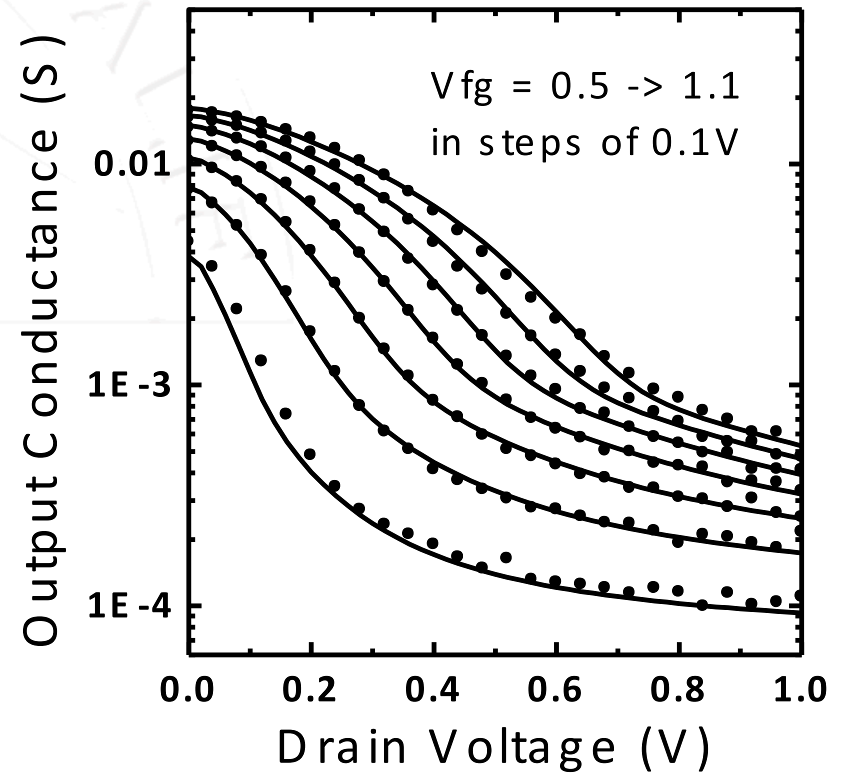
Lg=30nm TBOX=10nm

Extraction Results : I_d-V_{ds} and G_{ds}-V_{ds} with varying V_{bg}

- I_d-V_{ds} at V_{fg}=0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1 V

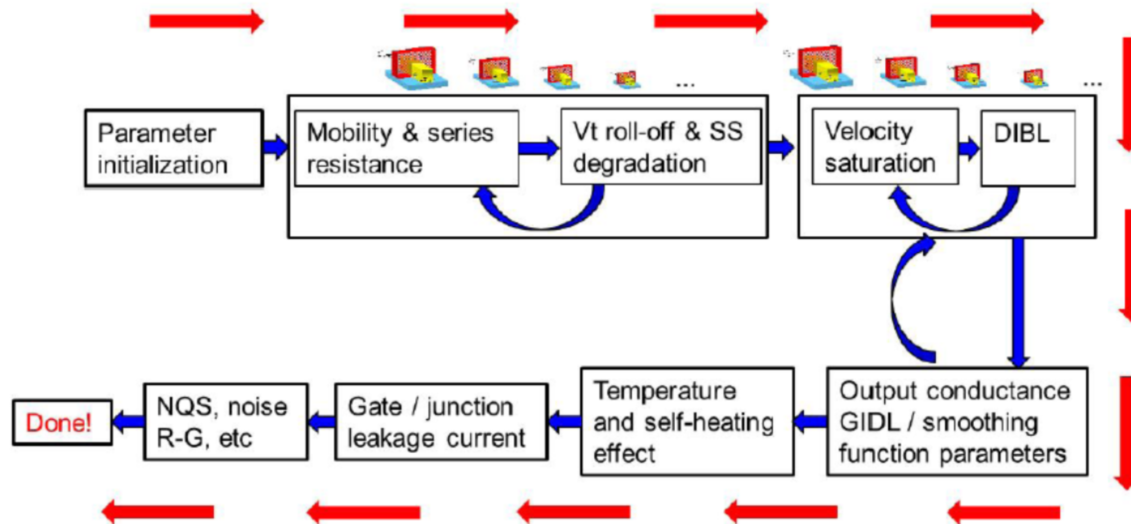


- Output Conductance (G_{ds})



Lg=30nm, TBOX=10nm

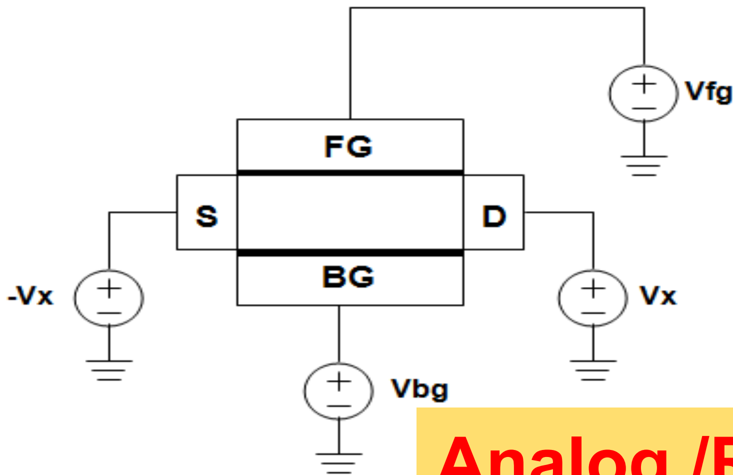
Global Parameter Extraction for ETSOI

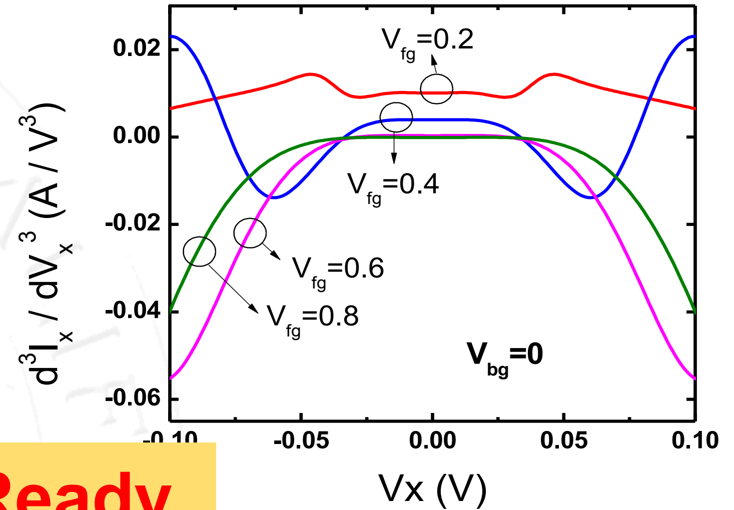


- **Calibration of the model**
  - **Through internship at IBM T.J. Watson**
    - **Work by Darsen Lu**
  - **Global Extraction performed for NMOS & PMOS at L=24nm …… 66nm**
  - **Excellent agreement for I-V across all gate lengths**
  - **C-V extracted and fine-tuned to match ring oscillator delay v.s. V_{dd}**

Gummel Symmetry Test

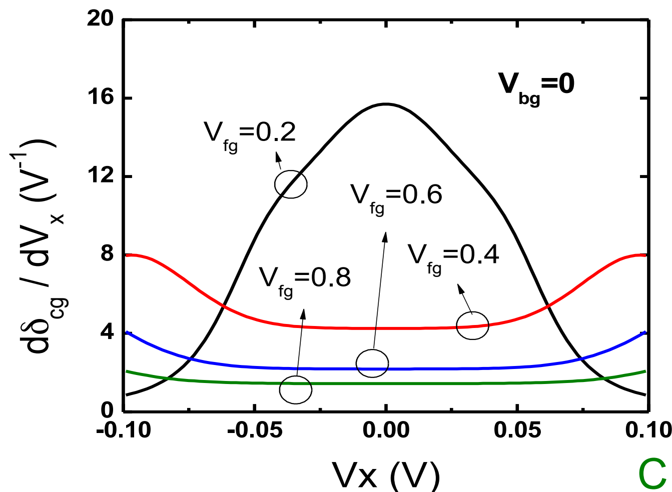
- **Drain Current Symmetry**

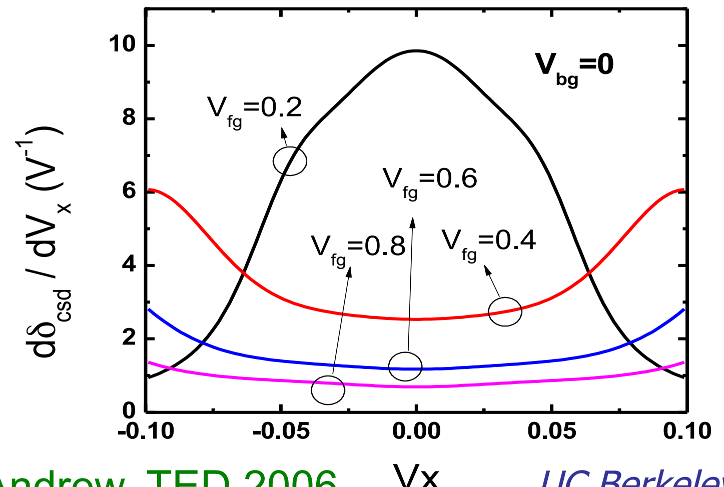




Analog /RF Ready

- **AC (charge) Symmetry**

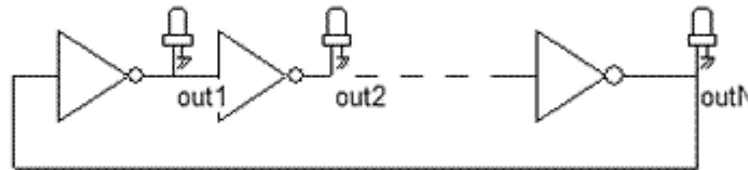




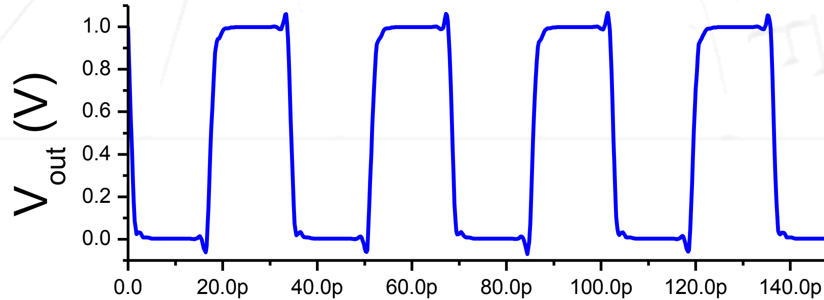
C. C. McAndrew, TED 2006

Convergence Tests

- **Excellent Convergence Properties**
- **Ex: 17-stage ring oscillator**

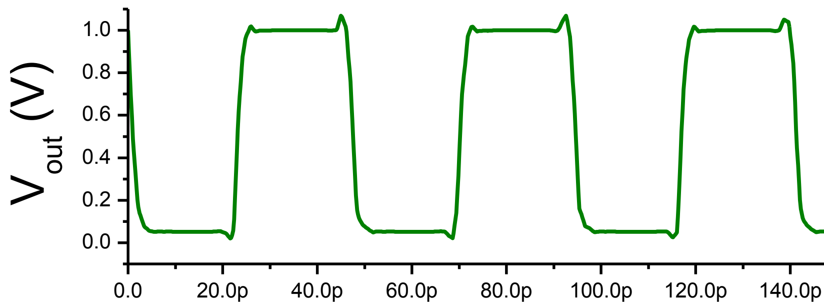


Various Back-Gate Potential Conditions



V_{bgn} = 0 V

V_{bgp} = 1 V



V_{bgn} = -3 V

V_{bgp} = 4 V

Speed Tests

Circuit	# MOSFETs	Model	Runtime per iteration per transistor (μs)
1-Transistor Id-Vds	1	BSIM4 IMG	40.7 29.1
17-Stage Ring	34	BSIM4 IMG	31.3 18.8
Coupled Rings	2020	BSIM4 IMG	41.0 22.6

- **Speed of BSIM-IMG v101 and BSIM v4.5 compared**
  - **Both model compiled with the in-built Verilog-A compiler of HSpice**
  - **Note: Each model uses its own default parameter. Parameters are not extracted for a real technology.**
  - **GIDL, I_g, Self-heating turned off.**

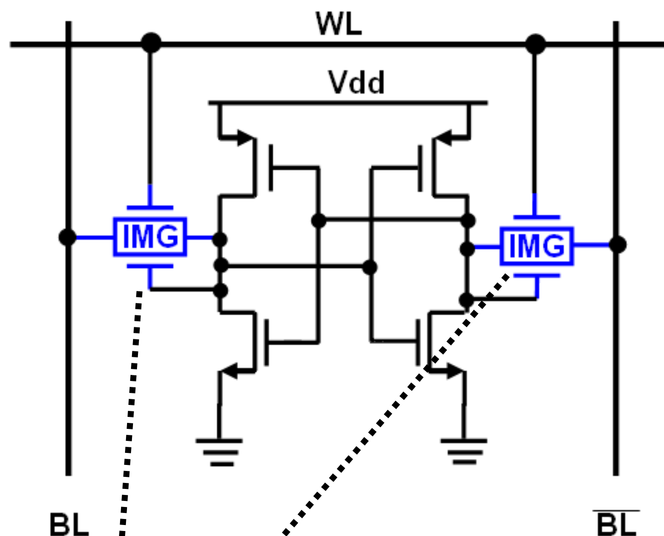
Averaged over 5 runs on a Linux box with a single-core AMD Opteron Processor (2.39GHz)

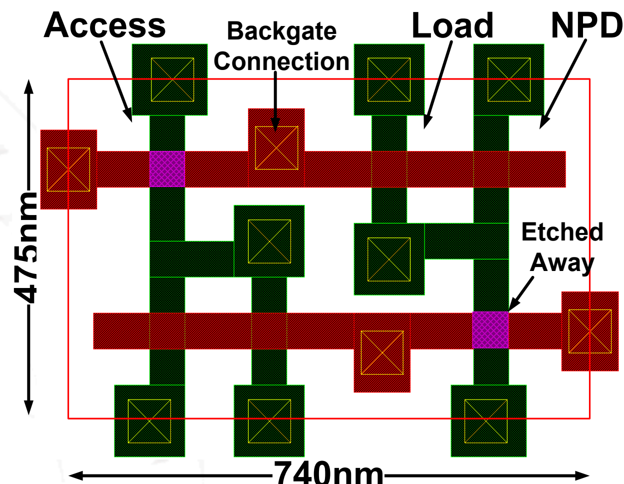
Outline

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Model Validation & QA
- **Future Research**
- Conclusion

Application Example: FinFET SRAM with Back-gate Dynamic Feedback

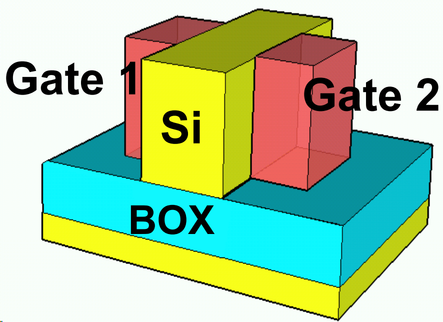
- **6T SRAM Cell using FinFETs**





Cell Area = $0.35um^2$

(Courtesy of Sriram Balasubramanian)

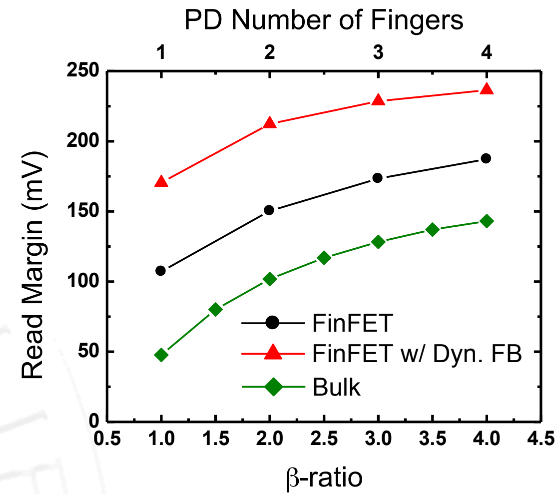


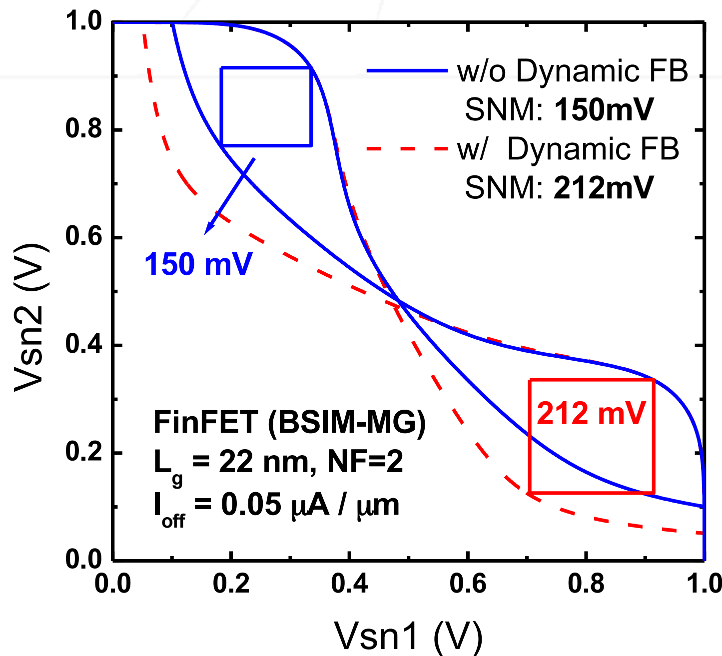
- **SNM improvement reported based on TCAD mixed-mode simulation.**

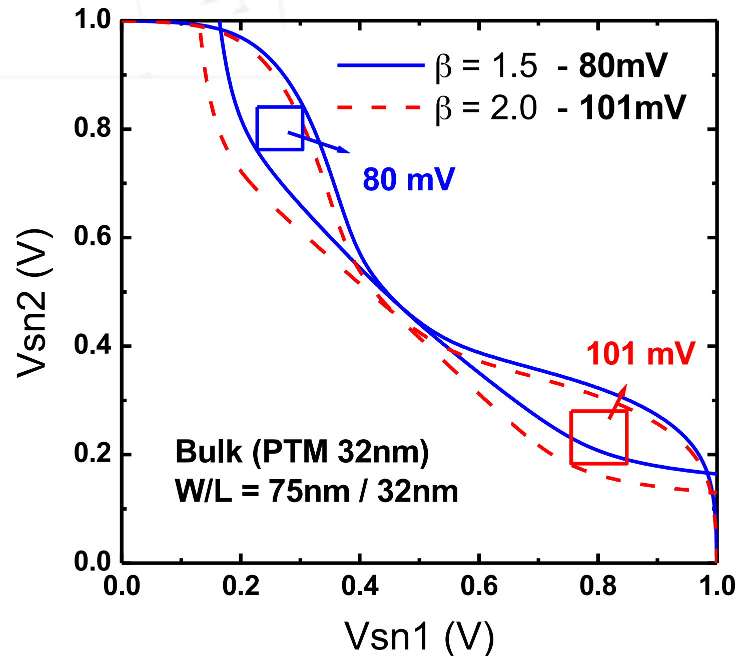
Z. Guo, S. Balasubramanian, R. Zlatanovici, T. King, B. Nikolic, "FinFET-Based SRAM Design," Proceedings of ISLPED, August, 2005.

BSIM-IMG Simulation of FinFET SRAM

- FinFET-based SRAM cells are simulated using BSIM-CMG and BSIM-IMG.
- Back-gate dynamic feedback enhances the read margin from 150mV to 212mV.
- Back-channel inversion required to simulate write margin.

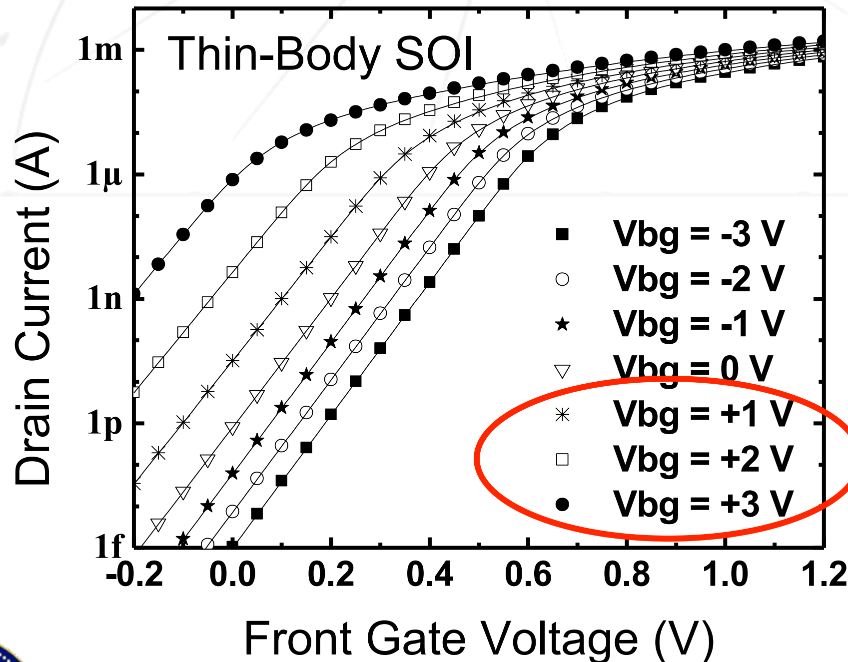






On-going research

- With a high back-gate bias, the double-gate SOI can enter depletion mode
  - Much higher leakage
  - But higher speed !



Symbols: TCAD

Lines: **New BSIM-IMG** with a novel iterative technique to compute the surface potential

Lg=10um
Tox=1nm, Tsi=8nm, Tbox=20nm
FG: midgap WF; BG: P+ WF

Where Are We!

- Introduction
- Core Model
  - Surface Potential Equation
  - Drain Current
  - Capacitance Model
- Real Device Effects
- Model Validation & QA
- Future Research
- **Conclusion**

Technology Transfer

- Release of BSIM-IMG 101 (April 2011)
  - Available in EDA tools: SimuCAD, ProPlus, Accelicon
  - Implementation In Progress @ Cadence, Synopsys
  - Package Ready for Technology Evaluation and Design under NDA
    - Verilog-A code and Well-documented Technical Manual
    - Provide some support and Commitment to improve the model

Summary

- **BSIM-IMG is a Turnkey , Production Ready model**
  - **Is submitted to the CMC for standardization**
- **Physical, Scalable Core Model for FDSOI devices**
- **Plethora of Real Device Effects modeled**
- **Advanced Device Effects – Quantum, Back-gate bias**
- **Validated on Hardware Data from two FDSOI/ UTBSOI technologies**
- **Available in major EDA tools**

Publications & Useful References

- **2005** *M. V. Dunga, C.-H. Lin, A. M. Niknejad and C. Hu, "BSIM-MG: A Compact Model for Multi-Gate Transistors," a chapter in FinFET and Other Multi-Gate Transistors edited by J. P. Colinge.*
- **2007** *D. D. Lu, M. V. Dunga, C-H. Lin, A. M. Niknejad and C. Hu, " A Multi-Gate MOSFET Compact Model Featuring Independent-Gate Operation", IEDM, December 2007*
- **2010** *D. D. Lu, C-H. Lin, A. M. Niknejad and C. Hu, " Multi-Gate MOSFET Compact Model BSIM-MG", a chapter in Compact Modeling Principles, Techniques and Applications, Springer 2010*
- **2011** *D. D. Lu, M. V. Dunga, C-H. Lin, A. M. Niknejad and C. Hu, " A Computationally Efficient Compact Model for fully-depleted SOI MOSFETs with independently-controlled front- and back-gates", Solid-State Electronics, vol. 62, no. 1, pp. 31--39, Aug 2011*

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  - IBM
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  - EDA Vendors and Users