MOSFET Compact Model Extensions for Circuit Simulation: A Perspective from Industry

Workshop on Next Generation MOSFET Compact Model

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Presenter: André Juge

Abstract

- MOSFET Compact Model Extensions for Circuit Simulation: A Perspective from Industry

- While CMOS Technology scaling has been steadily pursued to offer deca-nanometer devices, Circuit Design Community has benefited from successful development of core compact models able to capture important aspects of MOSFET electrical behavior in Circuit simulation tools. While BSIM4 models is still widely used within Industry for planar Bulk and SOI CMOS technologies, new MOSFET model generation (PSP, HiSIM…) has enabled high accuracy for design of Analog-Rf Circuits. Last, innovative modeling solutions are coming to Industry for new devices like planar FDSOI or 3D Finfet transistors.

- Beyond the successful development of core device models from Academia, model extensions need to be developed in Industry for a bunch of Technology and Design dependent effects, in close interaction with the Design tool providers to enable adaptation of Design flow.

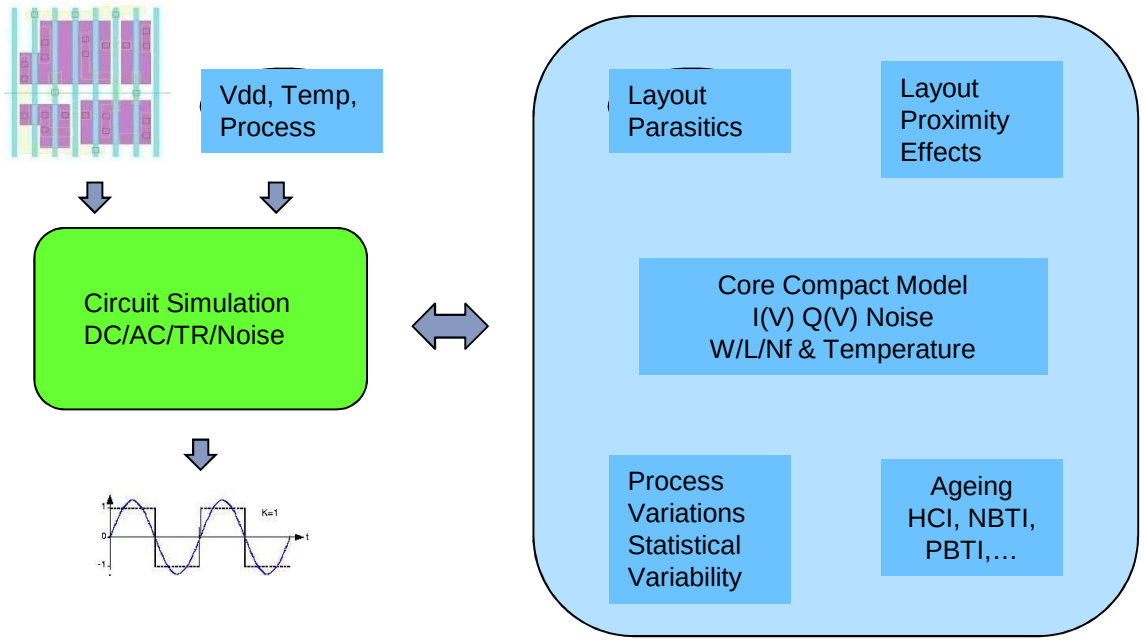
- *Presentation will overview and highlight examples of modeling extensions developed in Industry to account for realistic conditions in device operation, considering device design and circuit operation; examples of applications dealing with modeling of MOSFET Parasitics, Layout Proximity effects, Process variations, and Simulation of Degradation will be presented. The presentation is intended to bring compact modelers with a survey of such effects through their potential impact, and examples of implementation.*

Contents

- MOSFET Compact Model Extensions for Circuit Simulation: A Perspective from Industry

- Objective
- Parasitic capacitances
- Layout Proximity effects
- Process variations and Statistical Variability
- Reliability aware Design
- Summary and Perspective

Objective



❑*Core* models primarily account for Bias, Geometry (W/L/NF) and Temperature dependences of devices characteristics, and need information from other tools to account for real Design, Manufacturing, and Operating conditions.

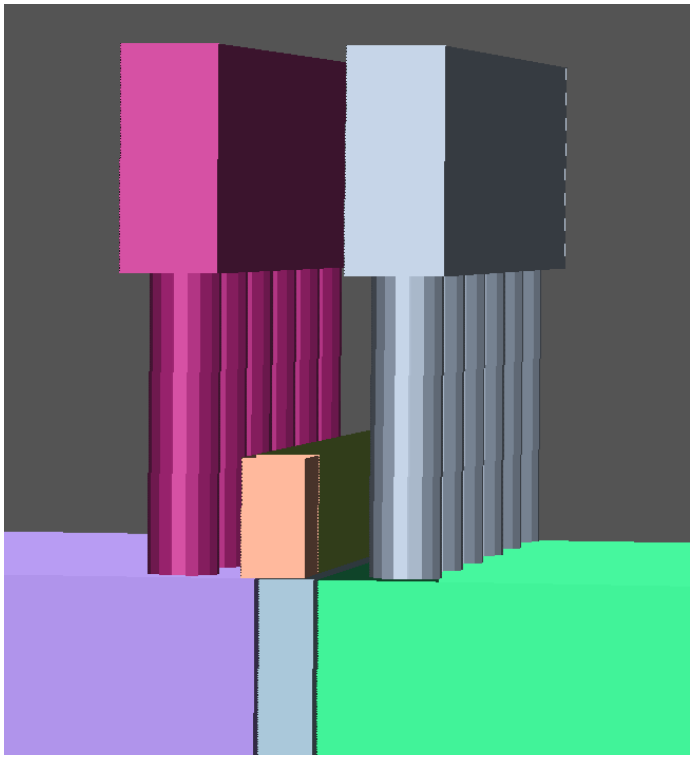
❑ *Extended* models are developed in Industry to account *for MOSFET Parasitics, Layout Proximity effects, Process Variations, Statistical Variability,* met by individual components after circuit integration, and *Ageing effects* considering device operation conditions.

❑*Circuit simulation methodologies* need to be developped concurently with modeling effort to allow manufacturing of high yield and reliable products. Integration of Solutions in Design flow is a must.

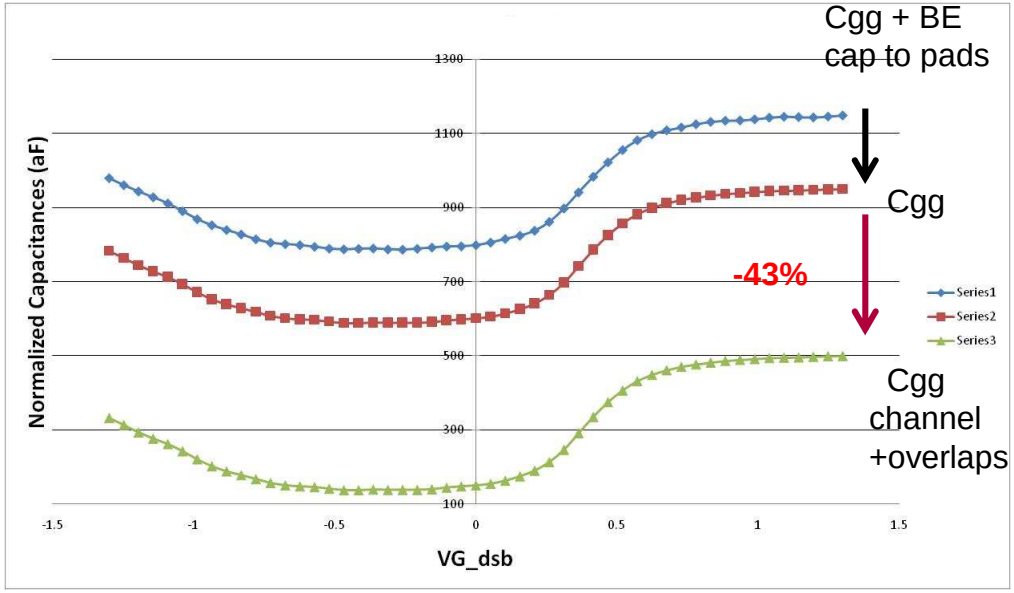
MOSFET Parasitic effects

- Extrinsic Parasitic capacitances
- Dependences to Layout
- Modeling/Simulation approach
- Perspective and ITRS

MOSFET Parasitic Capacitances



MOSFET with 3D view of fully contacted SD access

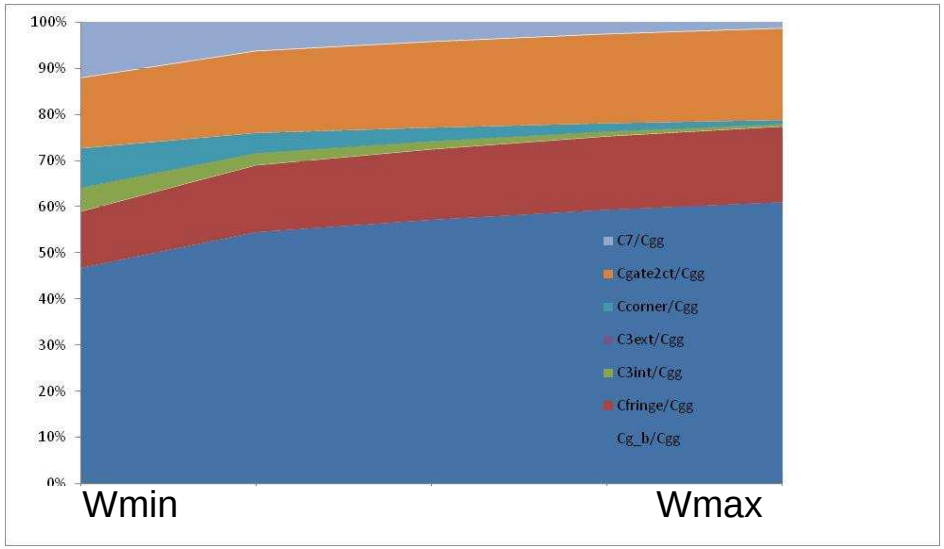


Nmos Lnominal Gate Capacitance

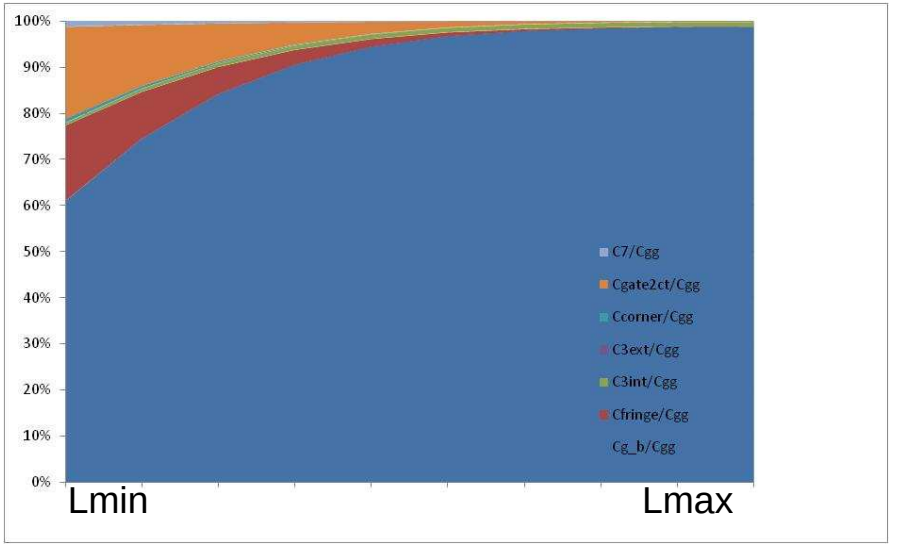
- Even for Planar Mosfets, Parasitic Capacitances surrounding gate is a 3D problem
- Cgg @Lnom almost x2 through lateral coupling between Gate and SD regions
- Cgg depends on W/L, S/D cts number/pitch, distance between gate and S/D cts

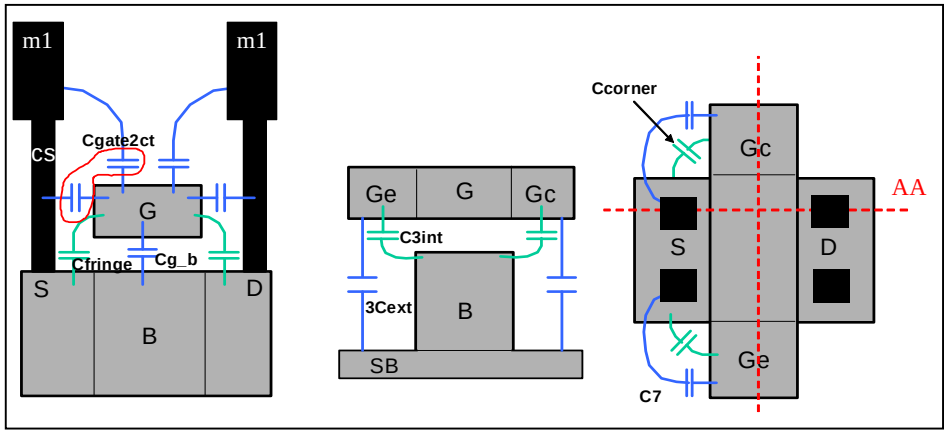
Scaling of MOSFET Capacitance partitioning on gate W/L

W dependence @Lmin



L dependence @Wnominal

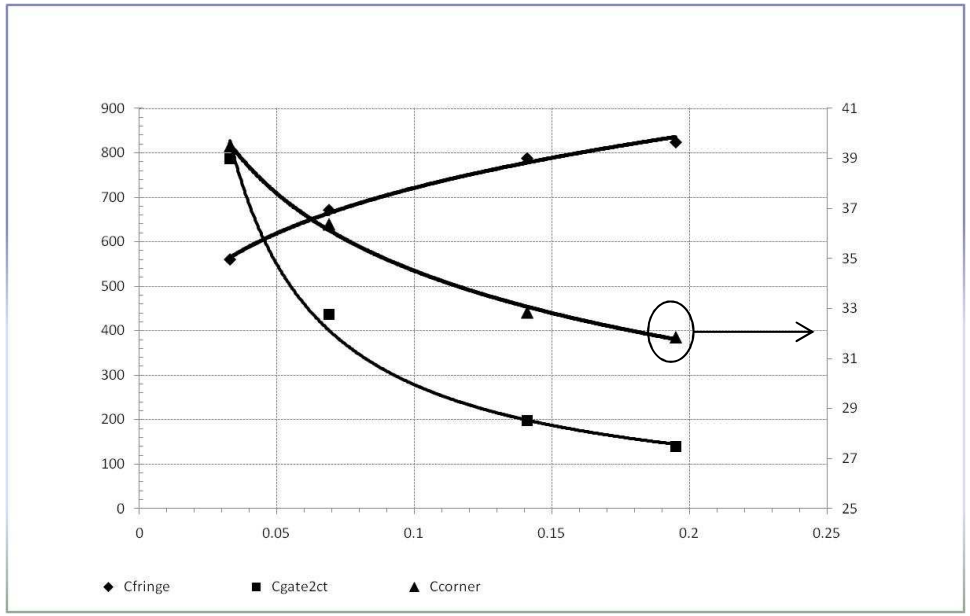




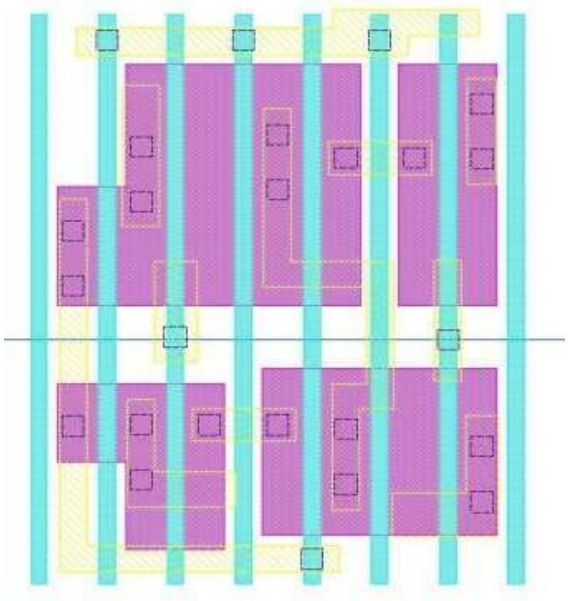
J.Mueller, SSE 2006

- Capacitances Wscaling @Lnom (left)
  - 40 %Cgg for large W is extrinsic; up to to 53% Cgg for Narrow W
  - Gate to S/D Diffusion and Contact capacitances as prime contributions
  - Corner capacitances remain significant contributions for Narrow W
- Capacitances scaling vs Gate length (right)

MOSFET capacitances in real Design (S/D Contact Position vs Gate)



Scaling Capacitances vs distance S/D Cts to Gate

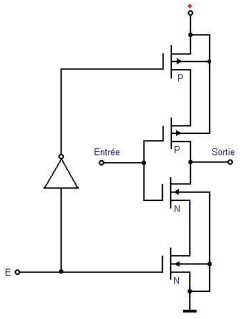


Semi-regular Std cell layout (Example)

- Capacitance dependence on SD contact position and number of contacts is significant and must be accounted in real designs
- Solutions:
  - Core models or PEX tools, provided number of Mosfet instance parameters is kept minimum for large size circuit simulation
  - Pre-Layout design phase: compact core model, with limited layout assumptions
  - Post-Layout design phase: PEX tool more adaptative to deal with variations in Layout style.

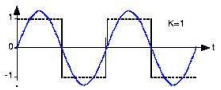
MOSFET capacitances in real Design (Adaptative simulation flow)

- Pre-layout simulation (default layout)



circuit netlist

simu

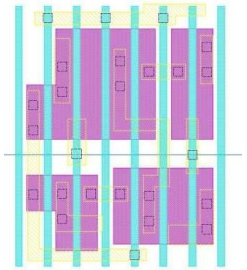


contains:
- network
- device instantiation
- device parameters (As/Ad/Sa/Sb/…) for default layout

- Mosfet R C parasitics for default layout , computed by SPICE model

Simulation results

- Post-layout simulation (real layout)



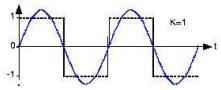
LVS step

circuit netlist

PEX

back annotated circuit netlist

simu

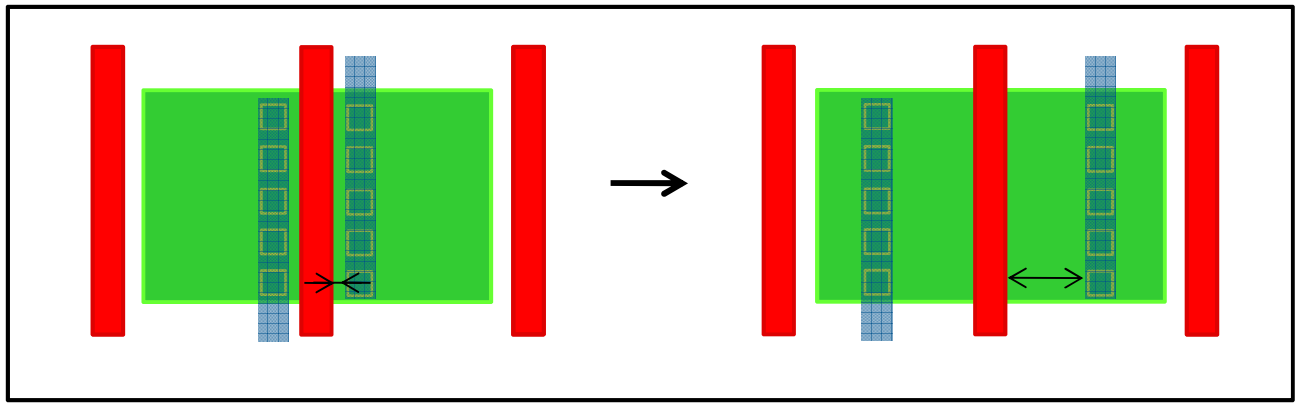


contains:
-network
- device instantiation
- device parameters (As/Ad/Sa/Sb/…) computed from layout
- device parameters can be "geometrical" or "electrical"

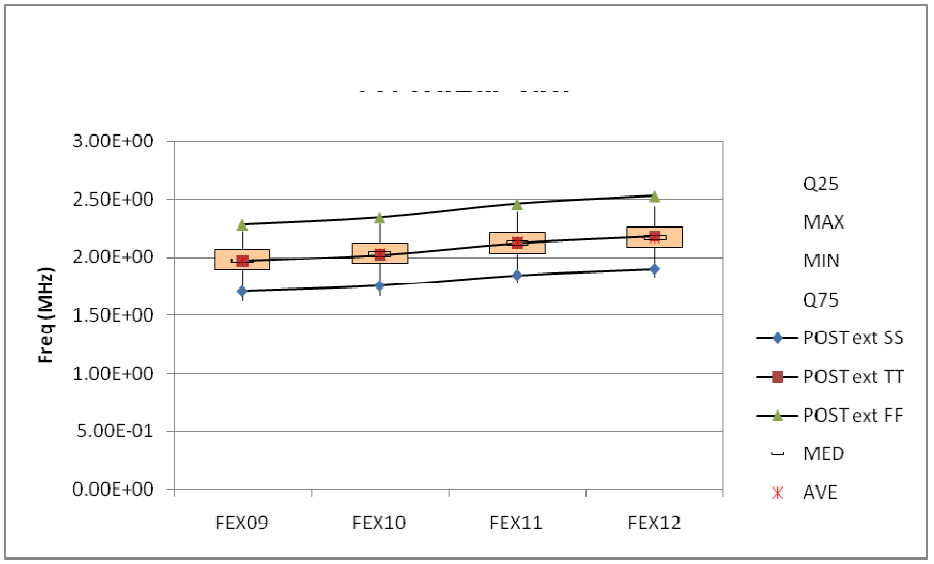
Addition of R C parasitics, computed from layout Applies to MOSFET devices and interconnect

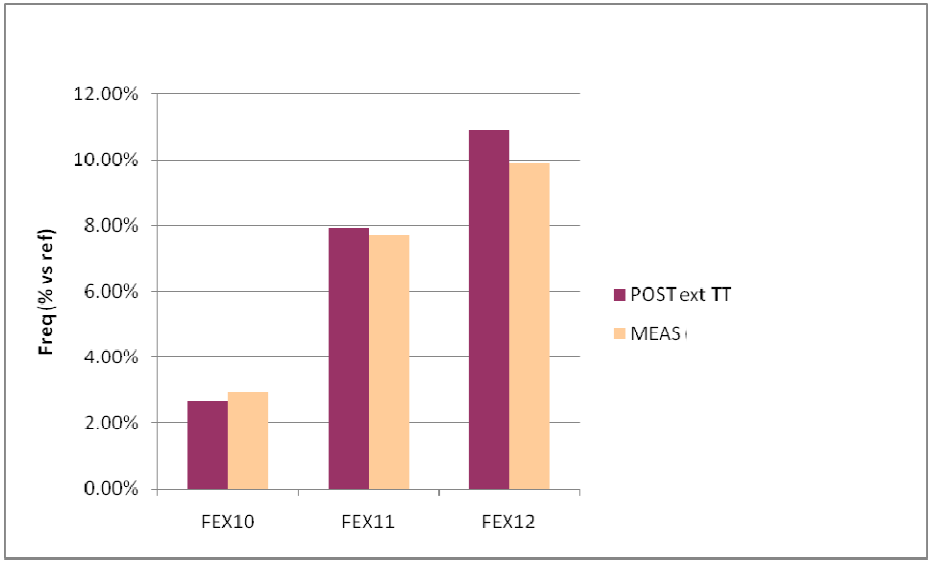
Simulation results

Verification DOEs: Impact on RO frequency



RO	dgc
FEX09	Min
FEX10	X 1.43
FEX11	X 2.5
FEX12	X 5





- F increase vs dgc: benefit of extrinsic capacitance reduction
- Efficient CAD accuracy monitoring methodology.

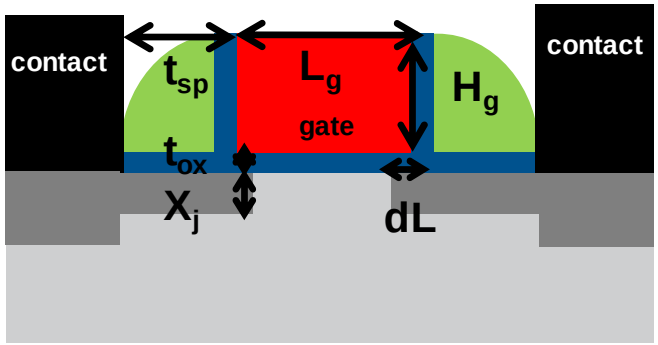
MOSFET Parasitics vs ITRS roadmap

- From ITRS, we have for each year and each device structure the following parameters:
  - **L**
  - **CPP (contacted gate pitch)**
  - **t_{inv}**
  - X_j for Bulk devices
  - **t_{si}** for FDSOI or multigate devices
- Structural parameters are derived =>

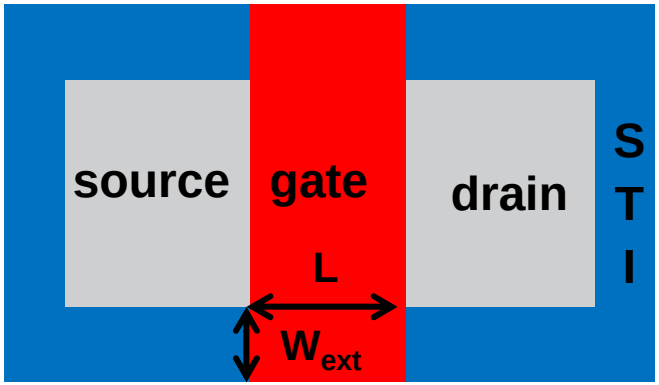
Parameters	Evaluation
t_{sp}	(CPP-L)/3
H_g	2L
W_{ext}	L
W	3xCPP
dL	L/4
t_{ox}	$2t_{inv}$
W	3xCPP
H_{si}	$3xt_{si}$
FP	$t_{si} + H_{si}$
N_{fin}	W/FP
t_{mask}	t_{si}

- Parasitics impact have been evaluated for each year for the following devices: Bulk, FDSOI, planar DG and FinFET (J.Lacord, SSDM 2011)

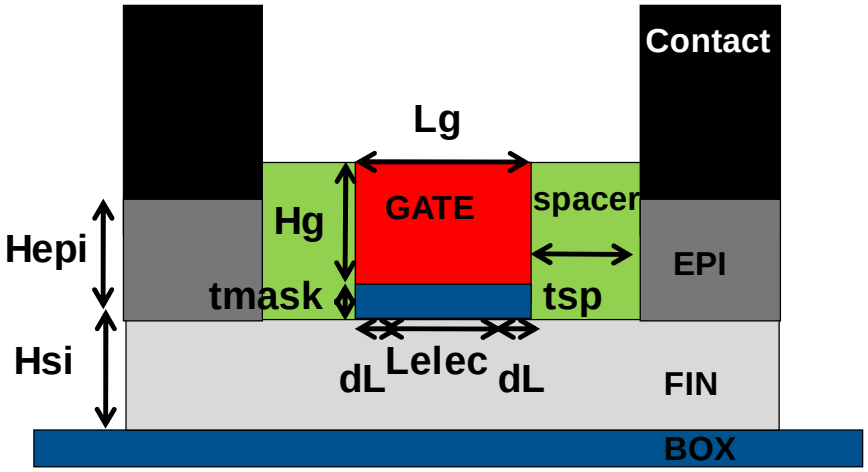
MOSFET Parasitics vs ITRS roadmap



Bulk FET cross-section

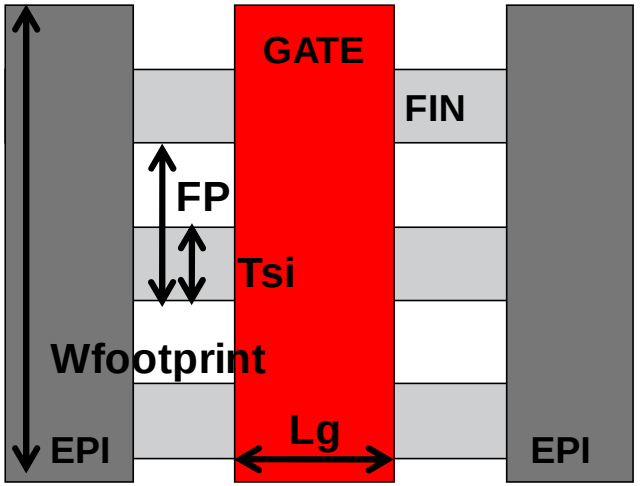


Bulk FET top view (wo contact)



FinFET cross-section

Courtesy of J.Lacord, SSDM 2011

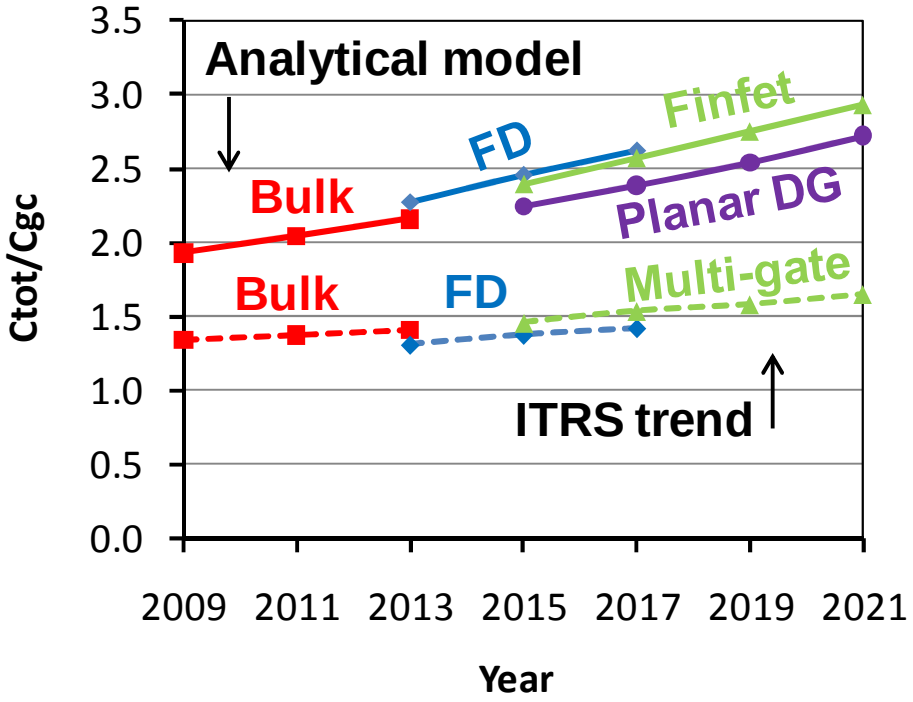


FinFET top view

MOSFET Parasitics vs ITRS roadmap

Total Gate + Parasitics over Gate cap. Ratio

$= C_{par}+C_{gc}$ ↘



Courtesy of J.Lacord, SSDM 2011

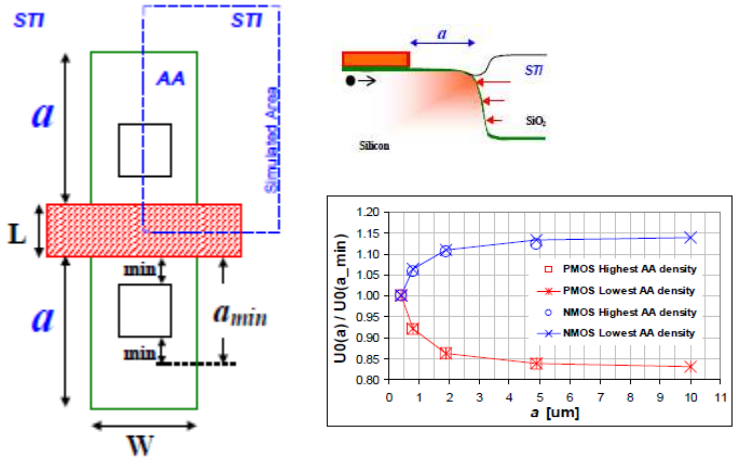
- ITRS Parasitics weight and evolution below FS simulation
- Planar DG presents a lower C_{tot}/C_{gc} ratio than FinFET

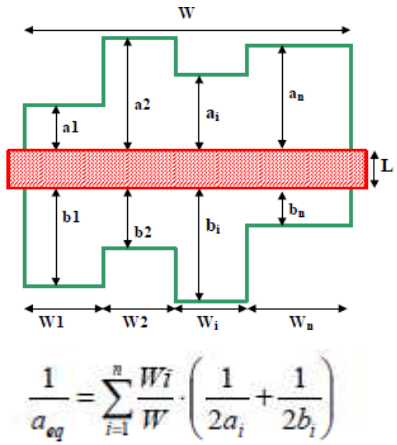
Layout Proximity effects

- Overview
- Modeling approach
  - STI example
- Modeling Accuracy dilemna
- Simulation flow
- CAD Accuracy

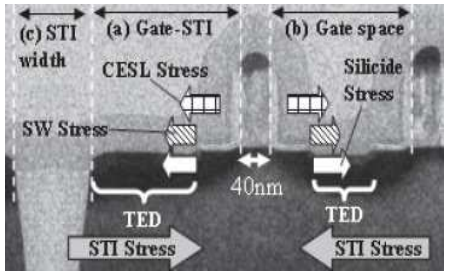
Layout Proximity effects: STI example

STI stress effect on Mobility (RA Bianchi, IEDM 2002)

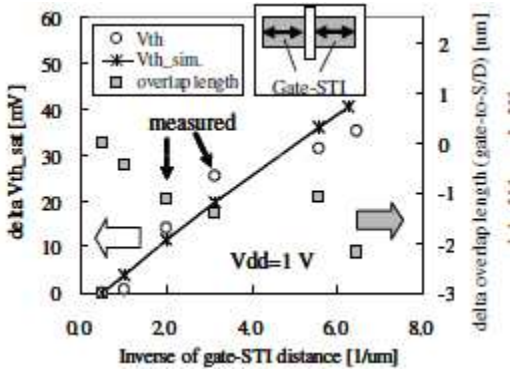




STI stress effect on Mobility and VT (Tsuno, VLSI 2007)



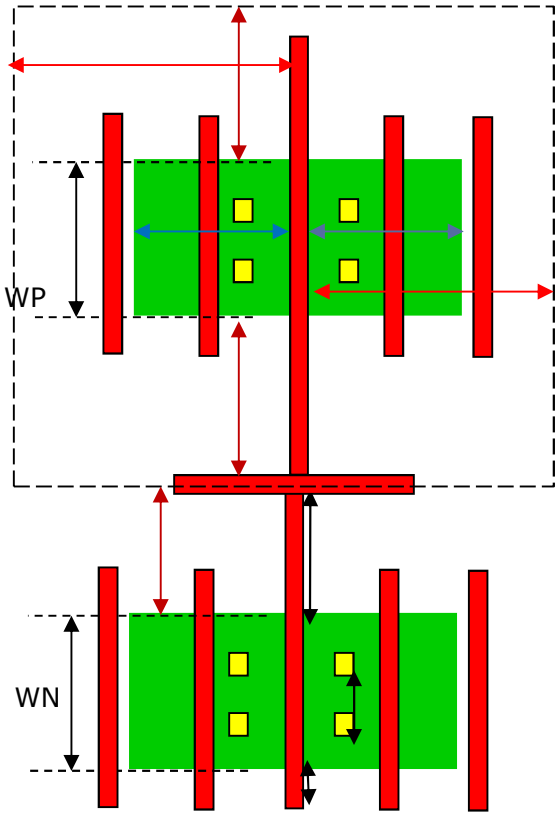
Tsuno, VLSI 2007



- Regular Layout: Mobility impacted by Stress, VT impacted by SD diffusity (modulated by stress)
- Handling Complex Layout in Design flow requires approximations:
  - Implementation shared bw Netlisting (Geometrical parameters) and Model (Electrical parameters)
  - Accuracy verification is challenging

MOSFET Layout Proximity effects overview

Effect	Contributions	Critical distance	Post-Layout Per Instance parameters
WPE	Ion scattering on well photoresist	>1um	SCA, SCB, SCC
STI(LOD)	STI Stress SD diffusion	1um Local	SA, SB
STI (OD2OD)	Litho and Etch STI stress	Context 1um	VT and Mu correction
Active corner rounding	Litho and Etch	Local	Weff correction
Gate pitch	Litho and Etch CESL Stress SD diffusion	Context Context up to 1 um Local	VT and Mu correction
Gate corner rounding	Litho and Etch	Local	Leff correction
Contacts position	SD Rseries Channel stress	Local	Rs and Cs correction
Others …			



- A bunch of Design dependent effects related to distances between Well, Gate, Active, Contact layer patterns and related density context
- Different physical effects interplay; impact, amplitude are technology dependent
- Each transistor sensitivity to each effect also depends on instance W/L

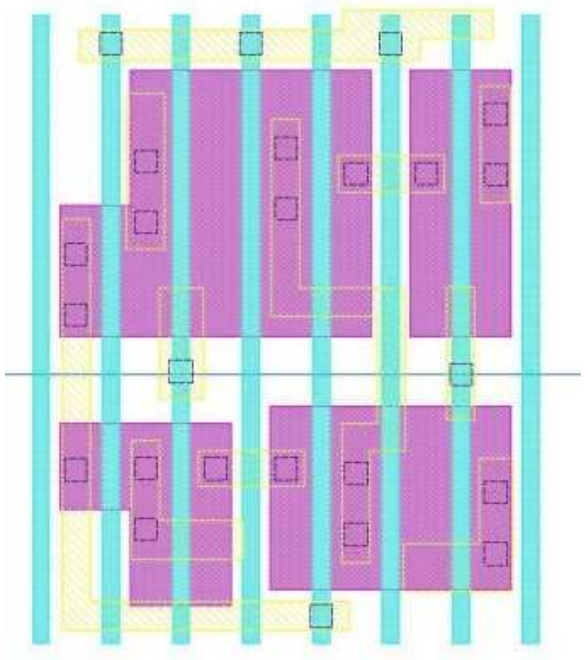
MOSFET proximity effects: Accuracy dilemna

- A bunch of effects with 1-10% impact of performance (Low Power technology), and more (High Power technology , where Stress effect is dominant)

- **Characterization dilemna: Layout DOEs**
  - WPE: 4W x 4L x 6 distances x 2 orientations x 2 N/P devices= 394 DUTs
  - Overall about 2K DUTs per N/P device, not considering interaction between effects!

- **CAD Netlisting dilemna : Post Layout extraction**
  - Nb Geometrical instances > 100, loss of simulation efficiency
  - Pre-processing of geometrical/ electrical parameter variation through LVS: a must!

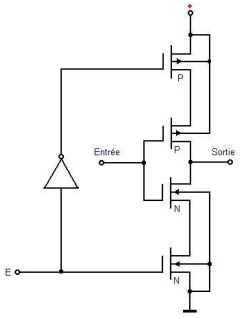
- **Modeling:**
  - Compact modeling of all effects with interactions is not experimentally applicable
  - Focus on first order layout effects and their dependence with W/L
  - Monitoring of CAD + Models accuracy through test structures offering efficient test methods



Layout example

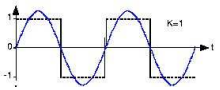
MOSFET capacitances in real Design (Adaptative simulation flow)

- Pre-layout simulation (default layout)



circuit netlist

simu



contains:
- network
- device instantiation
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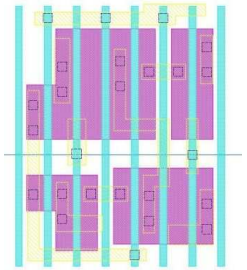
- device parameters (Sa/Sb/Sc…) for default layout

- Mosfet R C parasitics for default layout , computed by SPICE model

Simulation results

- Post-layout simulation (real layout)



LVS step

circuit netlist

PEX

back annotated circuit netlist

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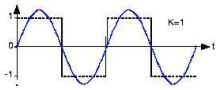
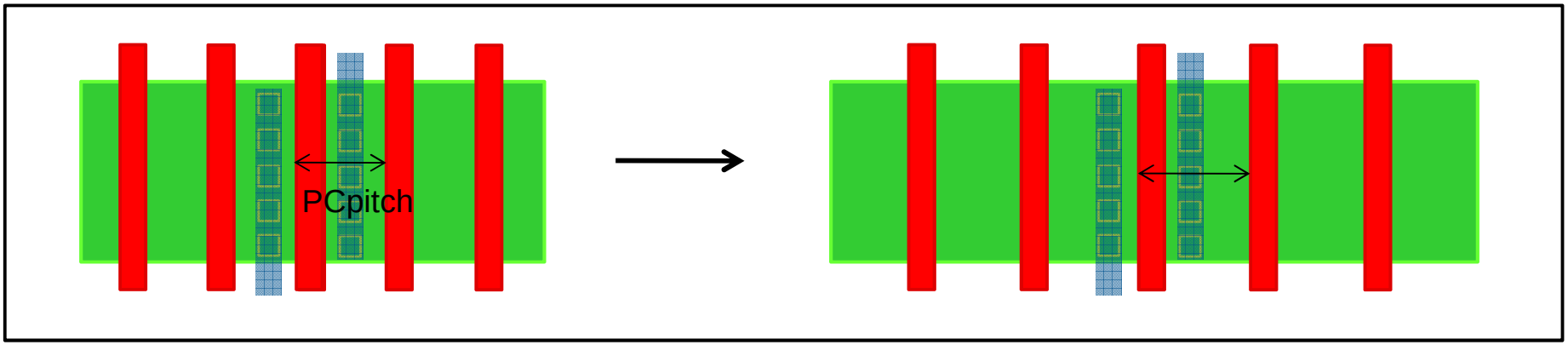


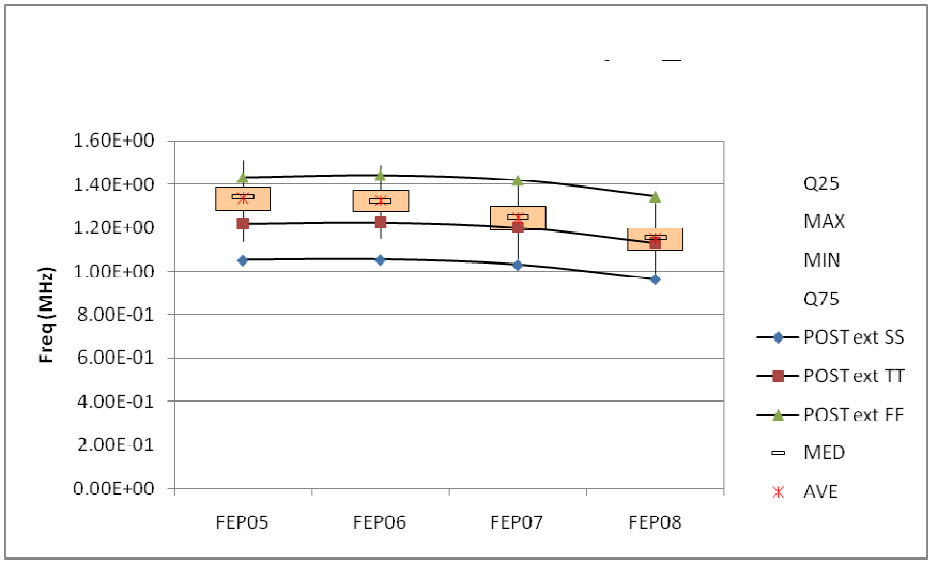
contains:
-network
- device instantiation
- device parameters (computed from layout
-
- device parameters can be "geometrical" (Sa/Sb/Sc…) or "electrical" (dvt, dmu)

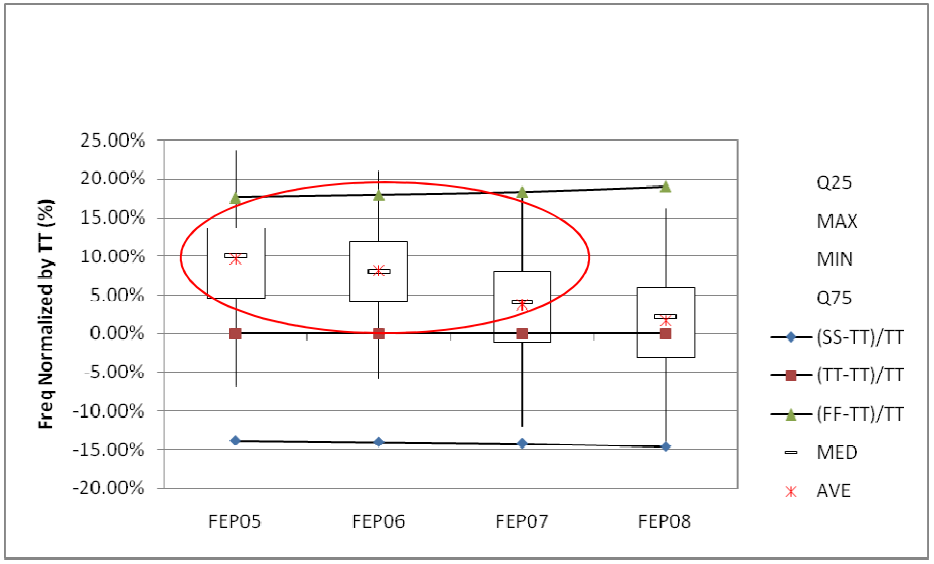
Addition of R C parasitics, computed from layout Applies to MOSFET devices and interconnect

Simulation results

MOSFET Layout Proximity effects: CAD Accuracy







- Example of Monitoring Gate Pitch effects with Ring Oscillator: CAD to Silicon mismatch can be depicted

Process Variations/ Statistical Variability

- Classification
- Sources of variations
- Model requirements
- Impact of Global/Local Variations: RO example
- Corner vs Statistical models

Classification of Variations

		Process	Environment	Temporal
Global		<L_g> and <W> <layer thicknesses> <R>'s <doping> <V_{body}>	T environment range V_{dd} range	<NBTI> Hot electron shifts
Local	Systematic	OPC Phase shift Layout mediated strain Well proximity	Self-heating IR drops	Distribution of NBTI Voltage noise SOI V_{body} history Oxide breakdown history
	Statistical	**Random dopants** **Line Edge Roughness** **Poly Si granularity** **Interface roughness** **High-k morphology**		
Across-chip		Line width due to pattern density effects	Thermal hot spots due to non-uniform power dissipation	Computational load dependent hot spots

Variations Sources at Circuit scale

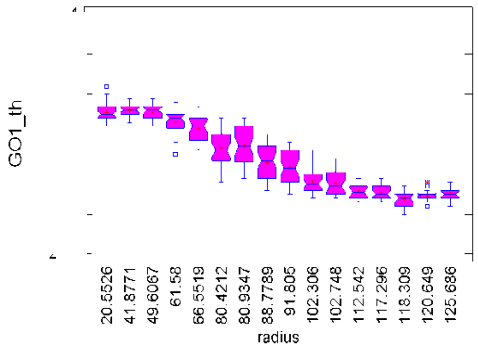
Classification from D.J.Frank (IBM)

Where Compact Model Extensions can help

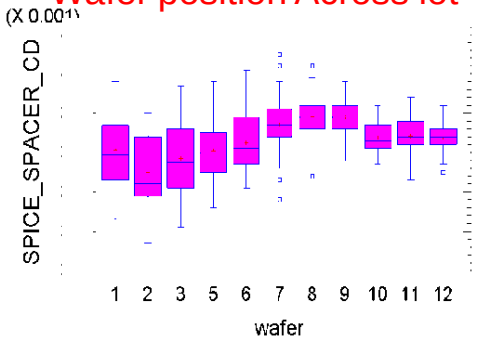
Variations in statistical models: sources

Global Process

Systematic Across wafer



Wafer position Across lot



- *Technology p*erspective: Process dependent Systematic effects
- *Design* perspective: global variations

Across Chip

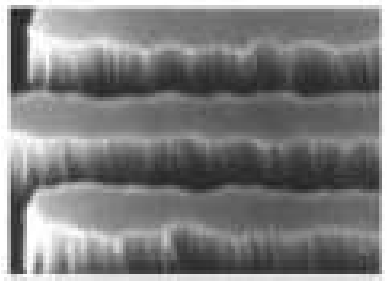
Mask tolerance

Litho/Etch

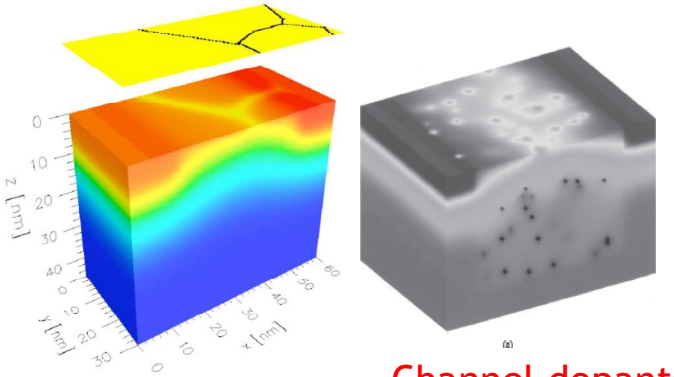
...

Local Statistical

Line edge roughness



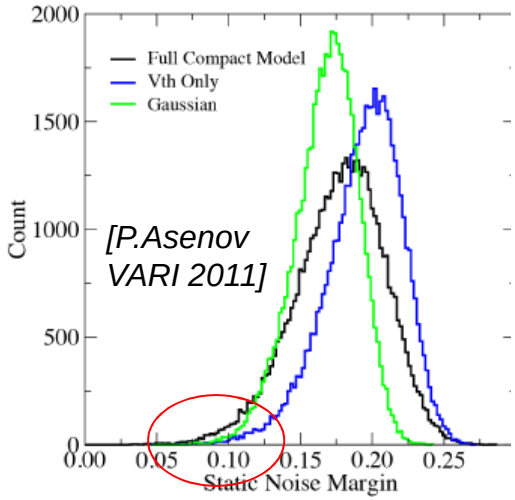
Poly Si granularity

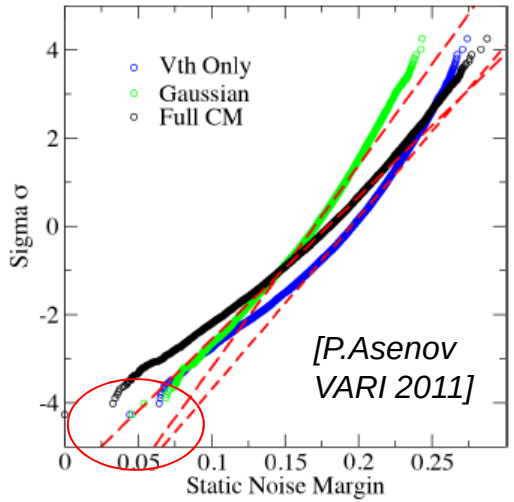


Channel dopants

Source: University of Glasgow, Device Modeling group, A.Asenov

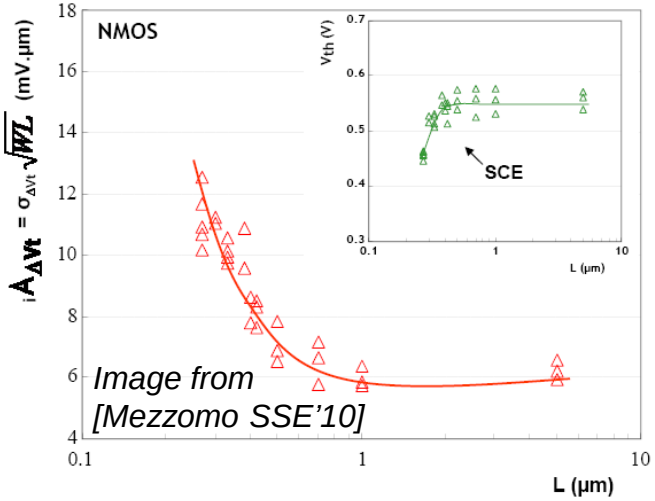
Modeling Improvements for Local Statistical Variations (Mismatch)

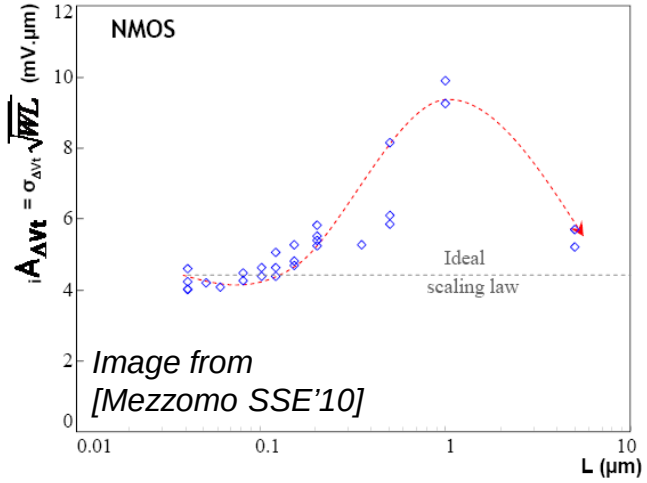




- **Sram SNM:**
- Full statistical Compact Model
- Moments up to 4th order

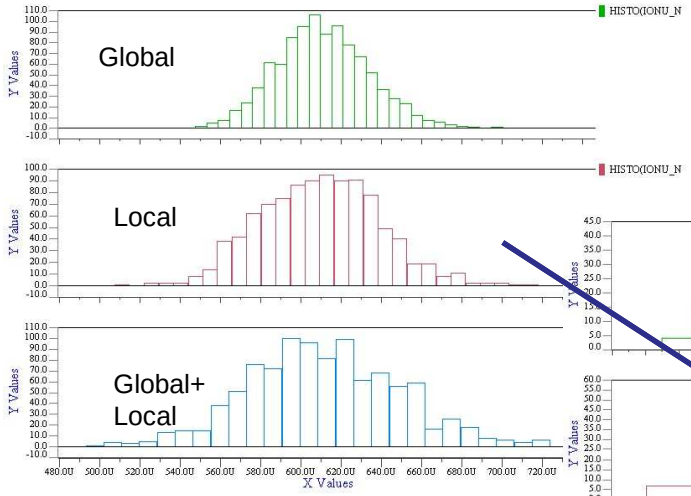
- **Analog:**
- SCE effect
- AVT scaling on L
- (pocket implants)





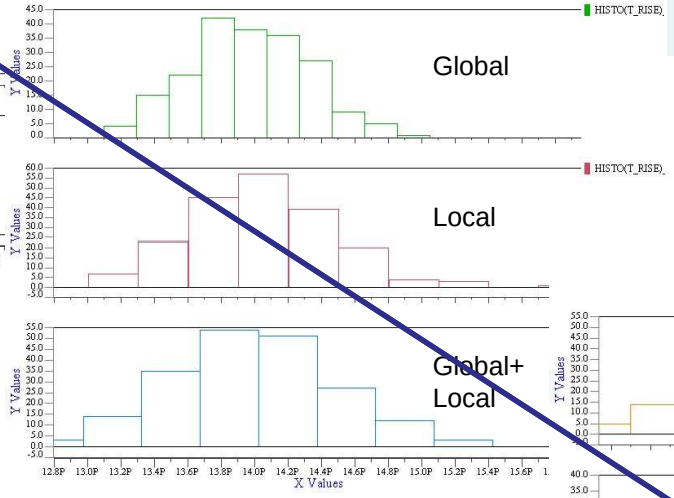
Impact Global/Local Variations impact: RO example

W ref: Idsat

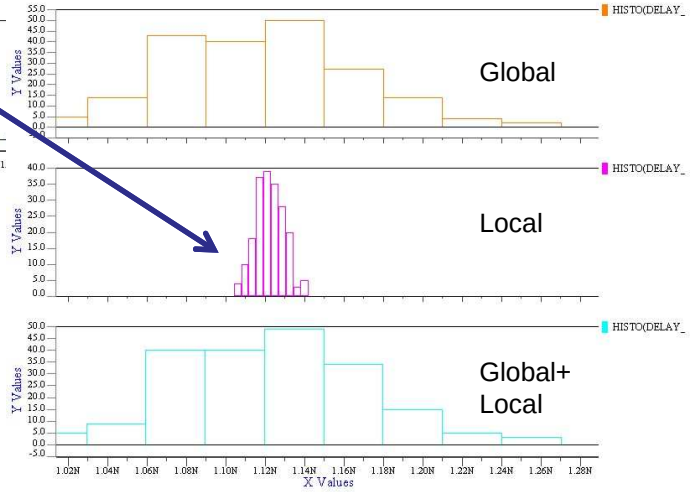


σ	Idsat (a.u)	Trise (a.u)	Period (a.u.)
Global	1	1	1
Local	1	1	0.16
All	1.4	1.4	1.02

Inverter: Trise



Inverter ring: Period

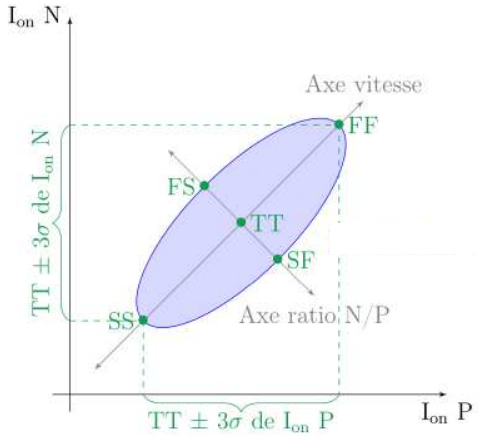


- Variations impact :
  - Transistor: Local ~ Global
  - Inverter Rise time : Local ~ Global
  - Inverter Ring Period: Local << Global

- Circuit design needs:
  - Accurate compact statistical models
  - Accurate and Efficient simulation methods

Corner Models vs Statistical Models

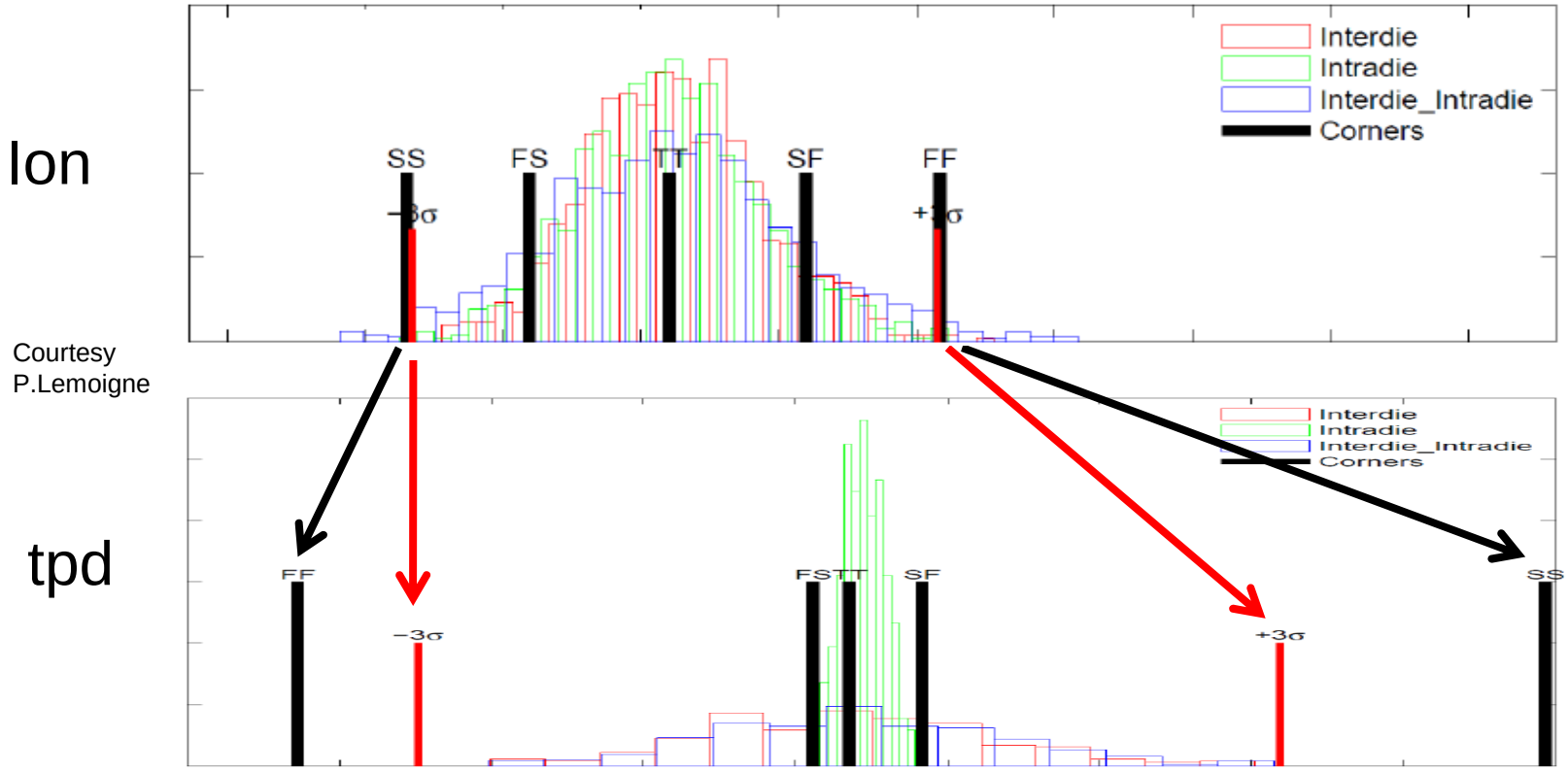
- Principle: simulate circuit tolerance with combinations of pre-defined +/- nσ deviations of model independent parameters to minimize computational effort
- Example (PSP inputs, Speed criteria):



M	SS	SF	TT	FS	FF
dLvar	+nσ	0	0	0	-nσ
dWvar	-nσ	0	0	0	+nσ
dtox	+nσ	0	0	0	-nσ
dnsub_n dnsub_p	+nσ +n	+nσ -nσ	0 0	-nσ +nσ	-nσ -nσ
dphibl_n dphibl_p	+nσ +nσ	+nσ -nσ	0 0	-nσ +nσ	-nσ -nσ
dmu_n dmu_p	0 0	-nσ +nσ	0 0	+nσ -nσ	0 0

- Method *simple* and *computationally* efficient, but …
- Corners are Performance specific . Ion, Ileakage, Speed, N/P ratio,…
- Suited to Global variations (Local deviations expected to average to 0 at circuit scale)
- Therefore requires validation against Statistical simulation

Corner vs Statistical Models: RO example



- Corners ΔIon ~ +/- 3σ, Δtpd > +/- 3σ

Perspectives

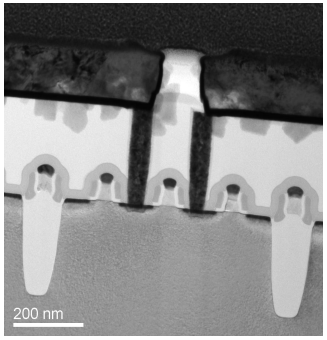
- New devices (FDSOI planar, Finfets)
- Methodologies
  - Statistical model accuracy
  - Corner model methodology
  - Efficient /Accurate MC simulation

Reliability Aware Design

- Reliability aware design
- Reliability aware modeling
- Results: Std Cells

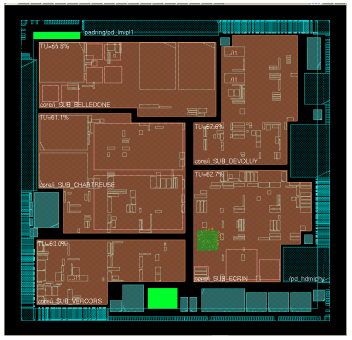
Reliability-aware design

DEVICE LEVEL



All degradation modes impact?

CIRCUIT LEVEL



Reliability impact on circuits is a function of

- ❑ operating modes of circuits,
- ❑ operating conditions faced by devices as a combination of these modes and the various input stimuli
- ❑ sensitivity of the performance of the circuit in the context of its place in design hierarchy

  E.g., a small shift in differential pair could affect the product, while a big shift in transistors in a power-down control block may affect nothing

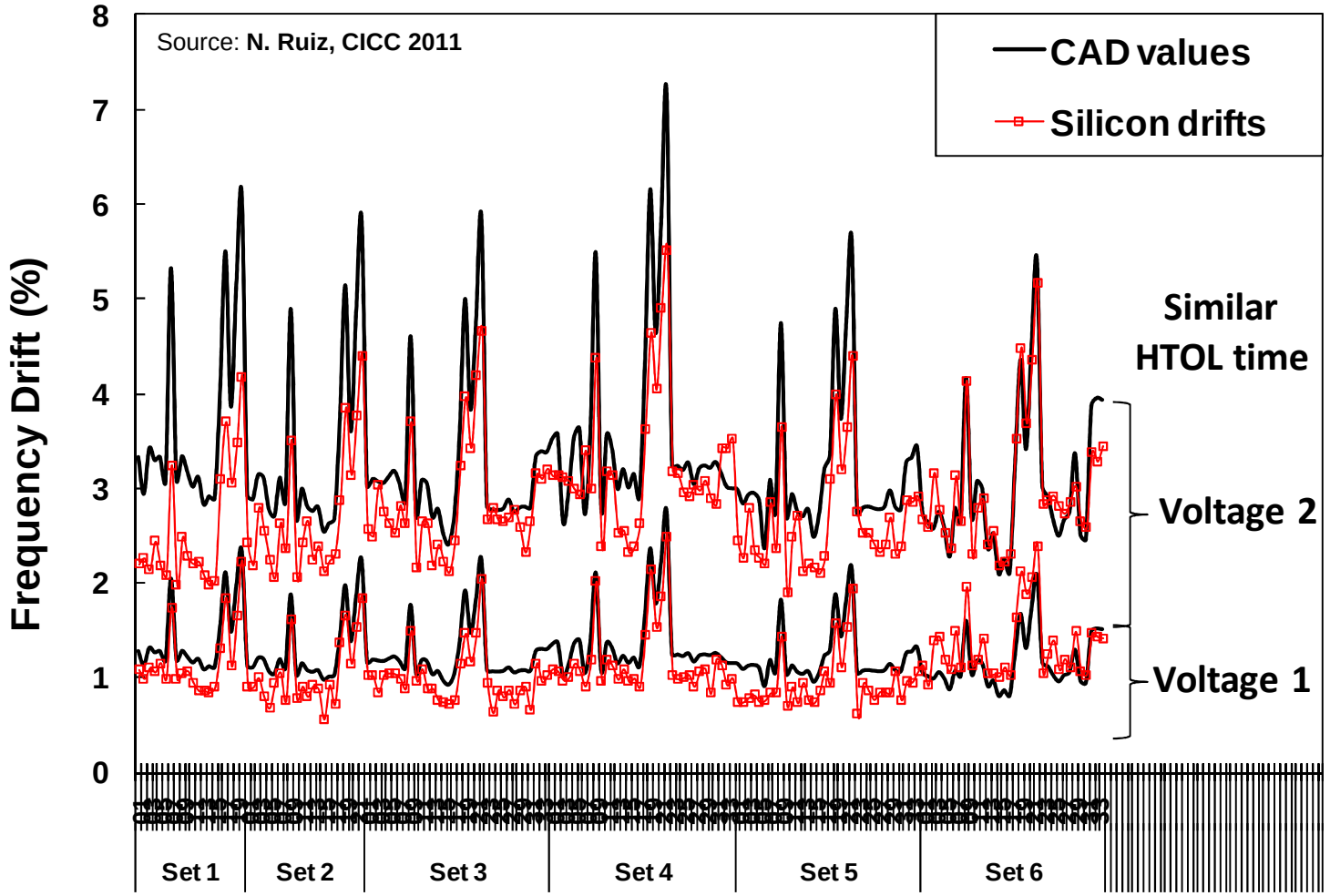
Design-in Reliability (DiR) =

set of methodologies and tools enabling **quantitative reliability assessment** at design-level

- Translate device reliability information for use by circuits
  - Library reliability information is requested by system designers
- Identify potential reliability problem conditions
  - Take into account the actual operating conditions of a design library
    - mode, stimuli, ambient conditions
- **Secure without over-design**

Reliability-aware modeling – Std cells results

- Reliability CAD values must be compared to drifts observed during HTOL test campaigns on library qualification testchips.



Summary

- Mosfet parasitics are performance limiting factors
  - Extrinsic cap may exceed ~x2 intrinsic cap for coming device generations
- Impact of Layout effects is difficult to estimate for coming technologies (as long as impact of each individual effect is less than 10 %) .
  - The experimental methodology learnings to account for these effects in current technologies will help
- Statistiscal Variability has raised from an Analog concern to a limiting factor for SRAM yield (Vddmin,…)
  - Both Process Variations and Statistical Variability remain concerns for modeling new devices for Low Power / High Performance applications
- Reliability aware Design is coming: requires a set of methodologies and tools enabling quantitative life-time assessment at circuit-level
- In Industry, those subjects will keep attention from the Modeling and Reliability expert communities from now and through the coming years.

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