Ultra Low Power:

Emerging Devices and Their Benefits for Integrated Circuits

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Outline

- **Power Challenge & Subthreshold Swing**
- **Sub-thermal Swing devices:**
  - Tunnel FETs
  - Negative Capacitance FETs
- **Novel Nano-Electro-Mechanical-Devices:**
  - Vibrating Body Fin-FETs
  - Suspended Body Double-Gate CNT FETs
- **Conclusion**

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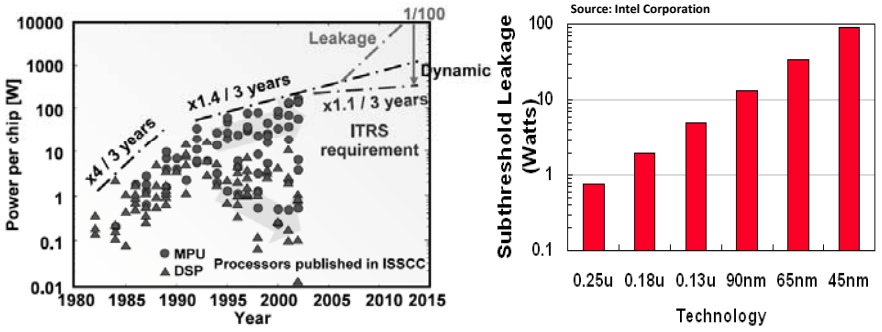
Power challenge

- Power per chip continues increasing.
- Leakage power dominates in advanced technology nodes.
- V_T scaling saturated by 60mV/decade physical limit.
- Voltage scaling slowed: 45nm=1V, 22nm=0.8V?



T. Sakurai, IEICE Trans. Electron., Vol.E87-C, April 2004, pp. 429-436.

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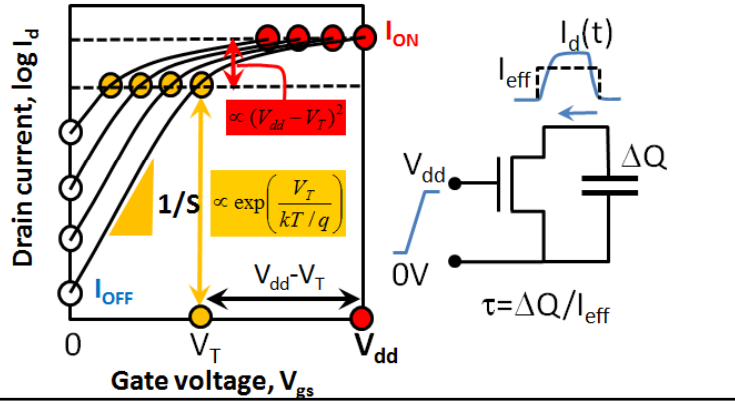
Leakage power & swing

Reducing threshold voltage **by 60mV**
increases the leakage current (power) **by ~10 times**

Performance metrics: I_{ON}, I_{ON}/I_{OFF}, S, V_T, V_{dd}, τ ←



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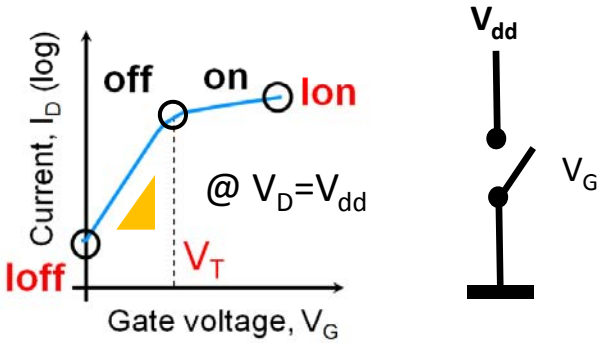
MOSFET: Vdd scaling & swing



Important: average subthreshold swing

$$S_{avg} = (V_T - V_{Goff}) / \log(I_T / I_{off}) \approx V_{dd} / \log(I_{on} / I_{off})$$

(mV/decade)

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Energy limits and swing

$$E_{total} = E_{dynamic} + E_{leakage} = \alpha L_d C V_{dd}^2 + L_d I_{off} V_{dd} \tau_{delay} \approx$$

$$\approx L_d C V_{dd}^2 (\alpha + \frac{I_{off}}{I_{on}}) \approx L_d C V_{dd}^2 (\alpha + 10^{-V_{dd}/S})$$

$$P = \alpha L_D C V_{dd}^2 f + I_{off} V_{dd} \approx K C V_{dd}^3 + I_{off} V_{dd}$$

voltage scaling by 5x (from 1 V to 0.2 V) with a negligible leakage power could offer a power reduction of 125x.

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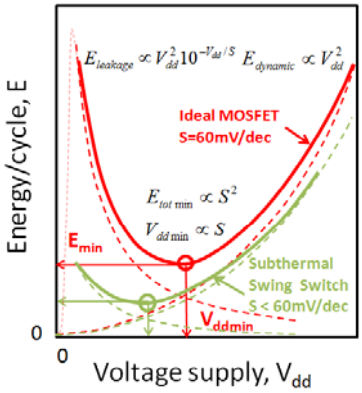
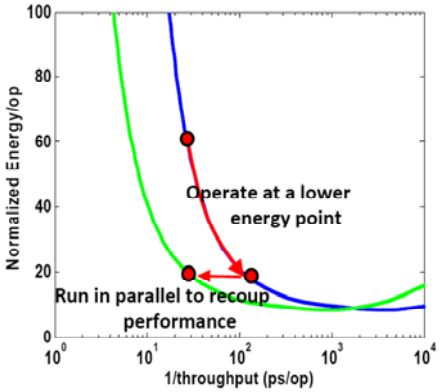
Swing vs. parrallelism

Lower CMOS fundamental limit in energy/op by **subthermal S devices**



Source: A.M. Ionescu, H. Riel, Nature, Nov. 2011.

Parallelism (multi-core): improves system performance under power constr.



Source: T.J. King, UC Berkeley.

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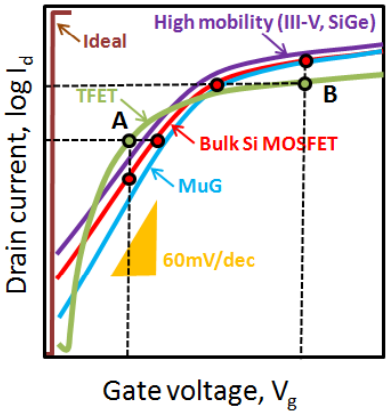
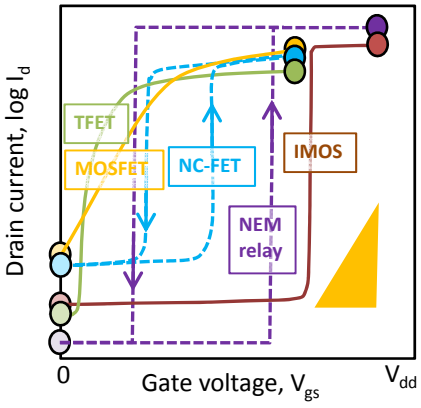
Subthermal swing switches

Tunnel FET vs. future FET



 # Small swing switches



Today, Tunnel FET is the most promising small swing switch for V_{dd} scaling.

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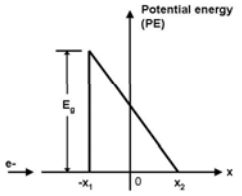
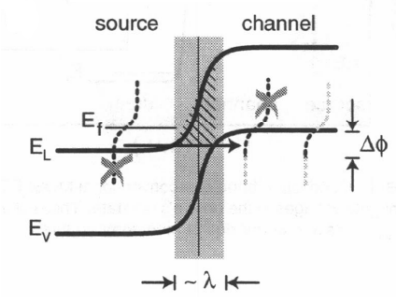
Tunnel FET physics: BTBT



$$I_{BTB} \propto T_{WKB} \approx \exp\left(-\frac{4\lambda\sqrt{2m^*}E_g^{1.5}}{3\hbar(\Delta\Phi + E_g)}\right)$$



Parameter	Means of improvement
m*	Small effective tunnel mass, SiGe, III-V, CNT
E_G	Source in SiGe, III-V heterostructures, strain CNT
λ	3D geometry (wrap gate), high-k gate dielectric, thin gate dielectric

Source: W. Haensch, H. Riel, IBM.

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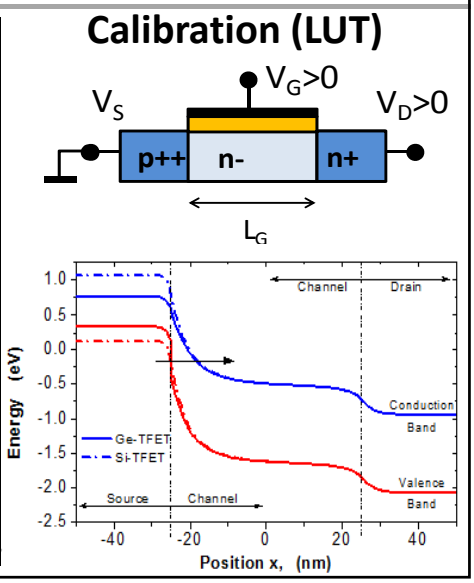
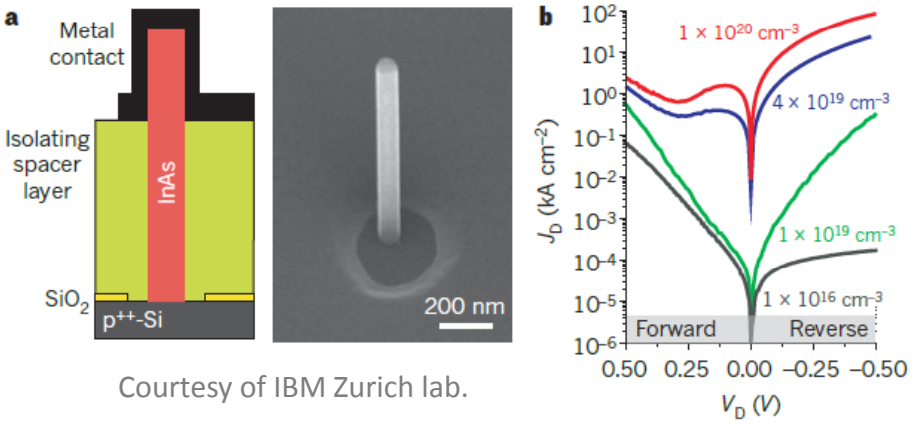
All-Si, Ge- & InAs-Source C-TFETs

TFET parameters	All-Silicon	Ge-source	InAs-Source
Gate Length, LG [nm]	50	50	50
Tox [nm]	2.5	2.5	2.5
εox	22	22	22
TSi	20	20	20
Source doping [cm^{-3}]	$3x10^{20}$	$3x10^{20}$	$1x10^{19}$
Channel doping [cm^{-3}]	$1x10^{15}$	$1x10^{15}$	$1x10^{15}$
Drain doping [cm-3]	$1x10^{20}$	$1x10^{20}$	$1x10^{20}$
Doping decay @ source/channel [nm/dec]	3	3	3
Gate Work Function [eV]	4.02 | 5.46	3.97	5.1
Apath [cm^{-3}s^{-1}]	$4x10^{14}$	$9.1x10^{16}$	$1x10^{19}$
Bpath [V/cm]	$1.9x10^{7}$	$4.9x10^{6}$	$1x10^{6}$
Phonon Energy [meV]	37	37	0
m_v/m_c	--	--	27



Ex: Calibration of InAs TFET on InAs-Si heterojunction diodes



Courtesy of IBM Zurich lab.

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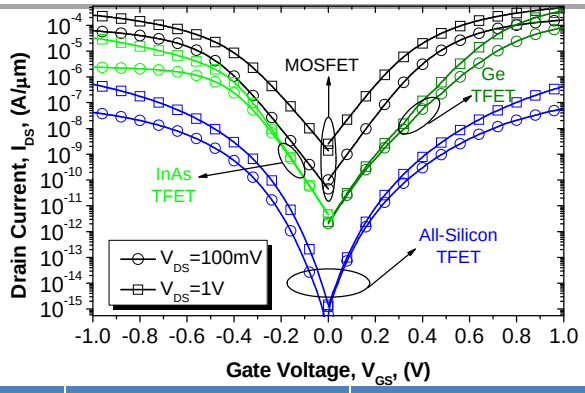
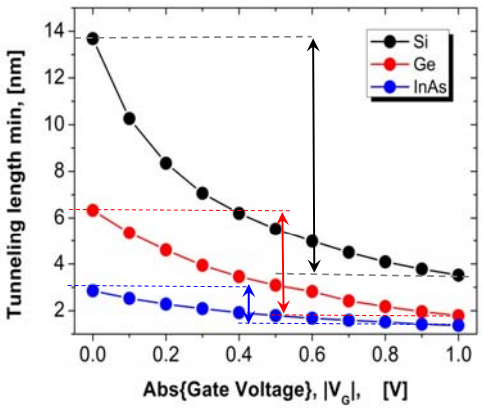
Comparison @Vdd=1V: C-TFETs

Ge/InAs C-TFET offers interesting performance trade-off.



	CMOS		Si-TFET		Ge/InAs TFET	
	n	p	n	p	n	p
Ion (uA/um)	483	246	0.426	0.520	364	32.9
Ioff (nA/um)	2.52	1.39	1.22×10^{-6}	1.46×10^{-6}	0.0024	0.00468
Ion/Ioff	1.92×10^5	1.77×10^5	3.49×10^8	3.56×10^8	1.52×10^8	7.03×10^6

Key optimization: min screening length, λ



Key performance dictated by λ

- bandgap
- gate dielectric (thickness, permittivity)
- silicon film thickness (UTB, NW)
- fringing fields

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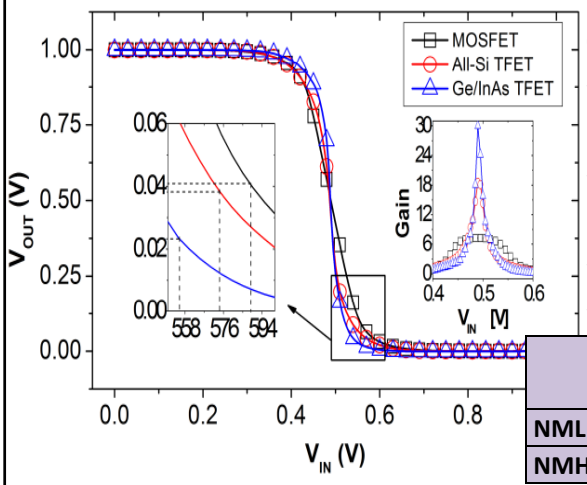
50nm C-TFET vs. 65nm C-MOS inverter



Differential gain dVout/dVin:
- highest for C-TFET inverters (Ge/InAs)
-peak ~ gm x rout

Noise margins:
- depend on S
- best for Ge/InAs C-TFET

	Si-TFET	He-TFET	CMOS
NML	387mV	410mV	394mV
NMH	426mV	445mV	411mV

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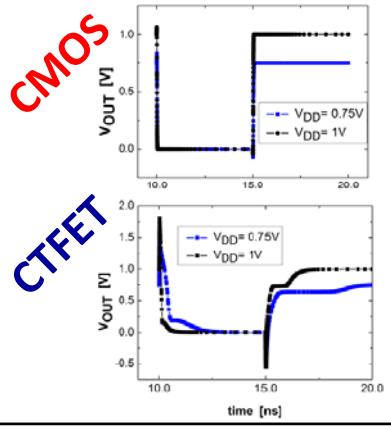
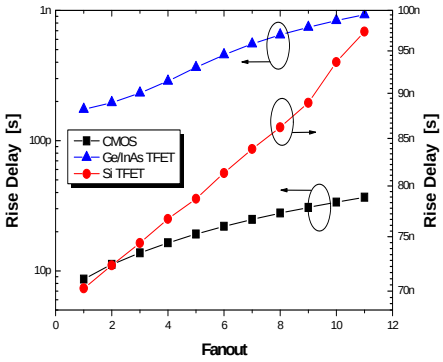
Delay

- 65nm CMOS much faster, as Ion is crucial for delay.
- Large capacitance in TFETs (Miller effect) is an issue: over/undershoots (needs adapted capacitance re-design).

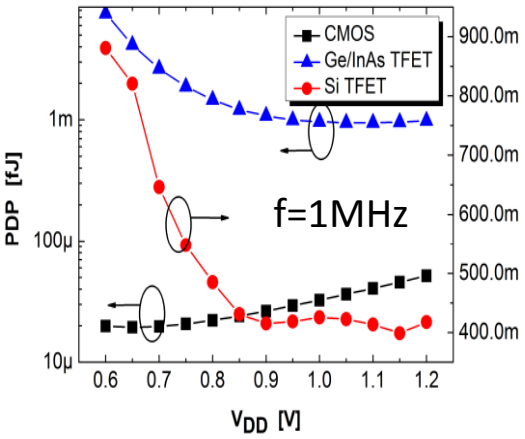




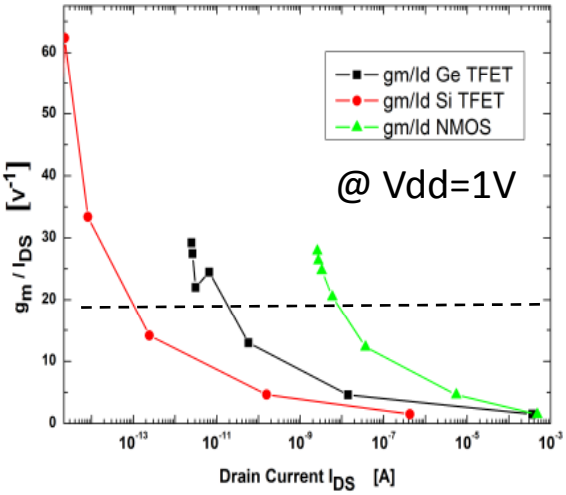
Static/dynamic power balance and PDP

-@VDD=1V, **the static power consumption of CMOS inverter** is 1.6nW which is **60% of the total power**.
-@VDD=1V, **the static power consumption of Si TFET** inverter is 1.3fW which is **0.02% of the total power**.
-@VDD=1V, **the static power consumption of Ge/InAs TFET inverter** is 600fW which is **11% of the total power**.

More TFET optimization needed



TFET for low power analog IC

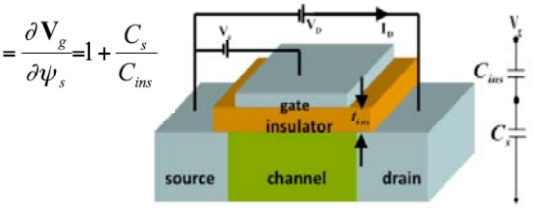


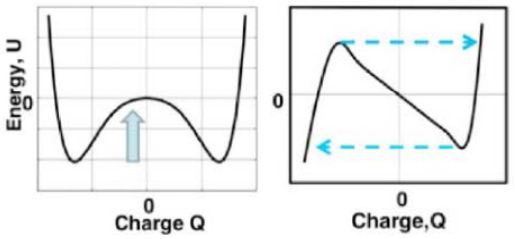
TFETs offer high gm/Id @ very little drain current (power) with very high temperature stability, which can trigger new low power analog IC design.

Negative capacitance FET

- step-up voltage transformer that could **amplify the gate voltage due to negative capacitance (m<1).**
- **S < 60mV/dec** in ferroelectric gate-stack FET: **lower Vdd**.
- **Hysteretic?**
- **Ion dictated by the FET channel, high!**

$$m = \frac{\partial V_g}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}}$$





S. Salahuddin, S, Data, NanoLett 2008.

Design of an active gate stack with m < 1

Design for stabilized negative capacitance effect

$$0 < m = \left[\frac{d\Psi_S}{dV_g}\right]^{-1} = \left[\frac{d\Psi_S}{dV_{\text{int}}}\frac{dV_{\text{int}}}{dV_g}\right]^{-1} = \frac{1}{G}\left[\frac{d\Psi_S}{dV_{\text{int}}}\right]^{-1} = 1 + \frac{C_d(V_g)}{\dfrac{C_{ox}C_{ferro}(V_{ferro})}{C_{ox}+C_{ferro}(V_{ferro})}} < 1$$

$$C_{MOS} = \frac{C_{ox}C_d(V_{\text{int}})}{C_{ox}+C_d(V_{\text{int}})} < -C_{ferro}(V_{ferro}) < C_{ox}$$

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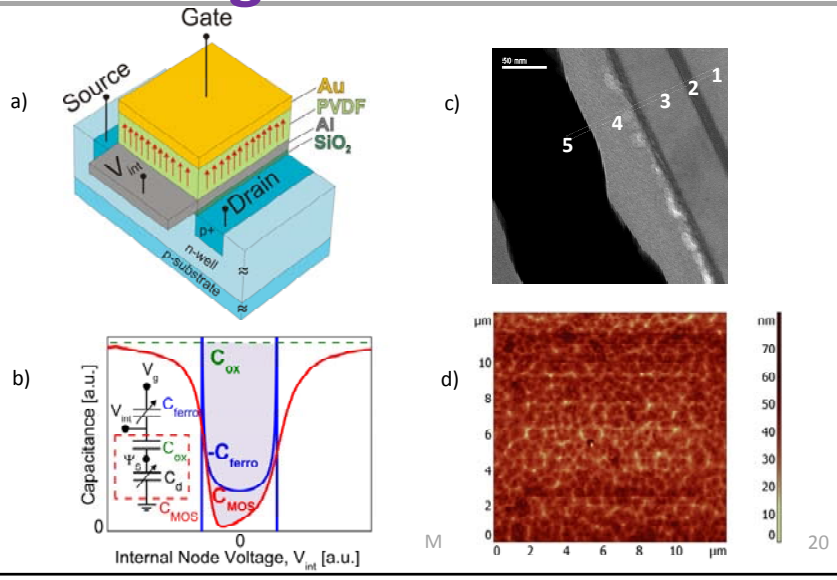
Metal/PVDF/metal/SiO2 gate stack

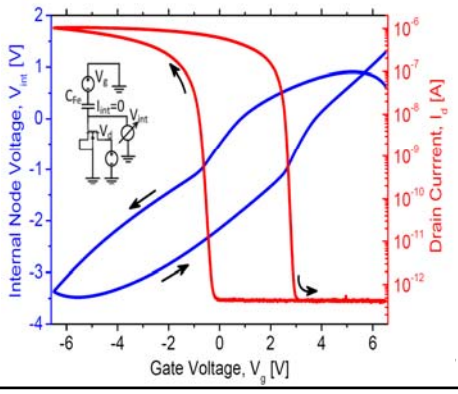


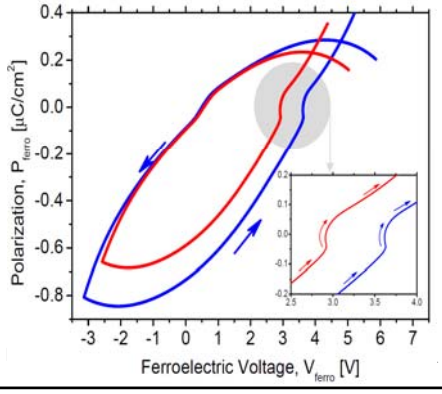
M 20

Neg Cap: S-shaped P-Vferro

- internal node voltage probed
- polarization extracted: S-shape P-Vferro where S is the lowest

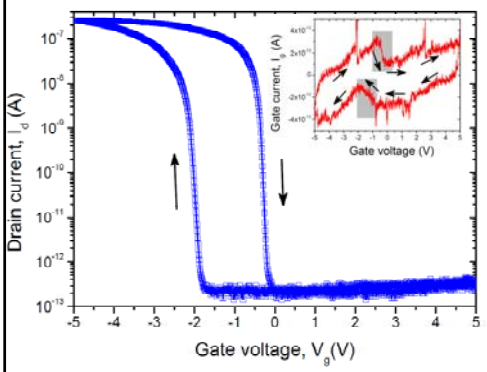
$$P = \left[\frac{(V_{\text{int}} - \Psi_S)k_{ox}}{t_{ox}} - \frac{V_g - V_{\text{int}}}{t_{Fe}} \right] \times \varepsilon_0$$

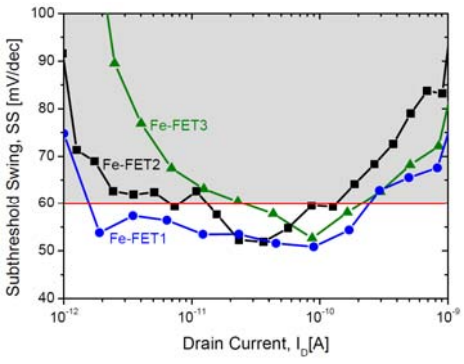




Subthermal Swing in Fe-FET

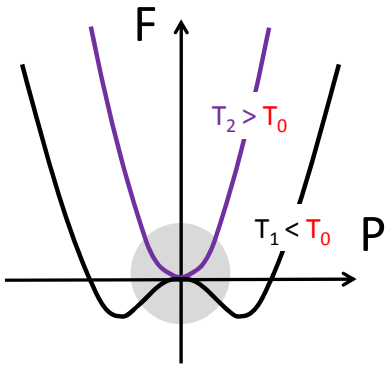
- S_{min} =46 mV/decade @ RT
- S_{avg}=51mV/decade over more than 2 decades of current



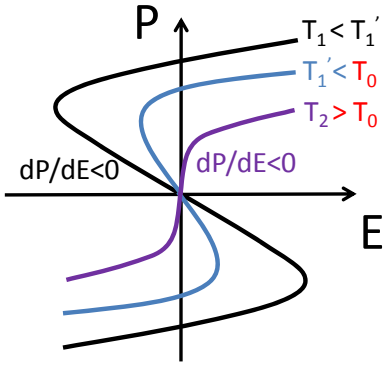


Temperature effect on NC

Effect of temperature on Helmholtz free energy, F.

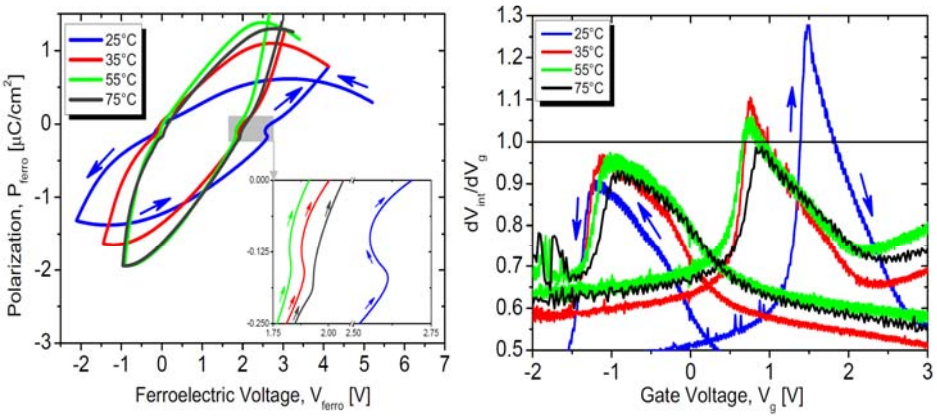


Effect of temperature on the S-shape P-E characteristics. $T<T_0$ material in the ferroelectric phase.

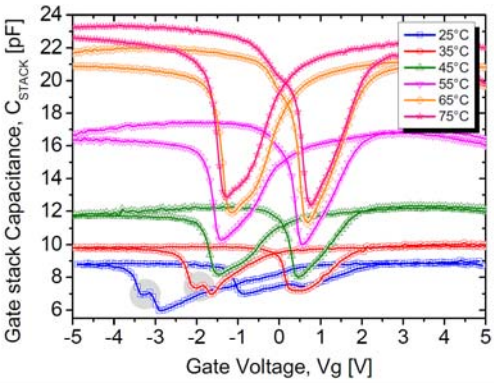


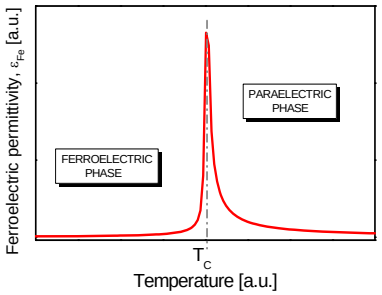
P(T), Internal gain (T)

Cancellation of negative capacitance effect near T0.



C_{stack} improved @ high T!





$$C_{Ferro} = \frac{\varepsilon_0}{d}\left(\lambda \frac{C_{CW}}{T - T_c}\right)$$

Interesting for circuit design:

- **Improved gate capacitance & lower swing @ high temperature.**
- **Integrated temperature sensor.**

$$C_{Fe-MOS}(T) = \frac{C_{OX} C_{CW} \lambda \varepsilon_0}{C_{CW} \lambda \varepsilon_0 + d C_{OX}(T - T_c)}$$

A.M. Ionescu, IEDM 2011

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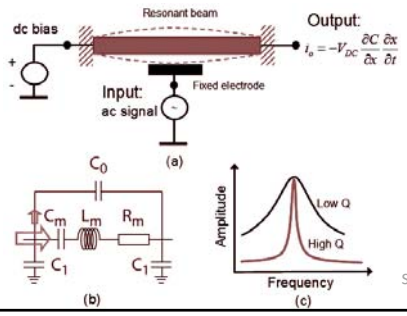
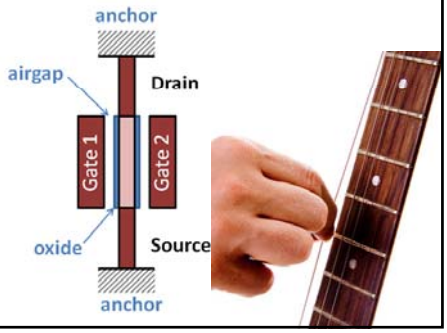
NEMS resonators: why?

- Probably the most promising family of RF M/NEMS.
- **Embedding full equivalent circuit functions (RLC) with very high-Q and voltage tuning** (possible replacement of quartz).
- Applications: **oscillators, mixing, filtering, sensing.**

Passive MEMS resonator

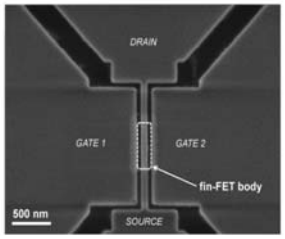


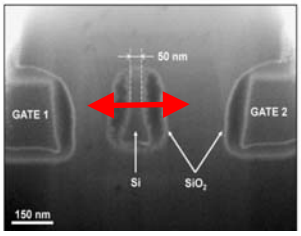
Resonant body transistor



scu, IE

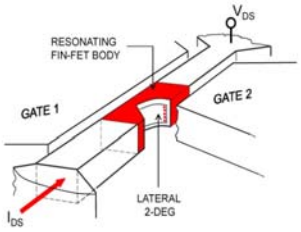
Vibrating body Fin-FET for nano-Watt oscillators

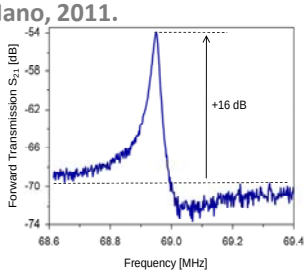


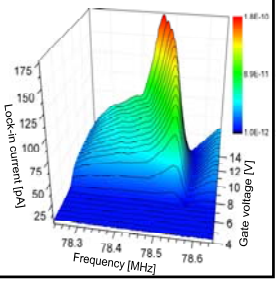


- fres:
  10 - 200MHz
- FD SOI film
- 100nm airgap
- Double gate control

S. Bartsch et al, To appear ACS-Nano, 2011.



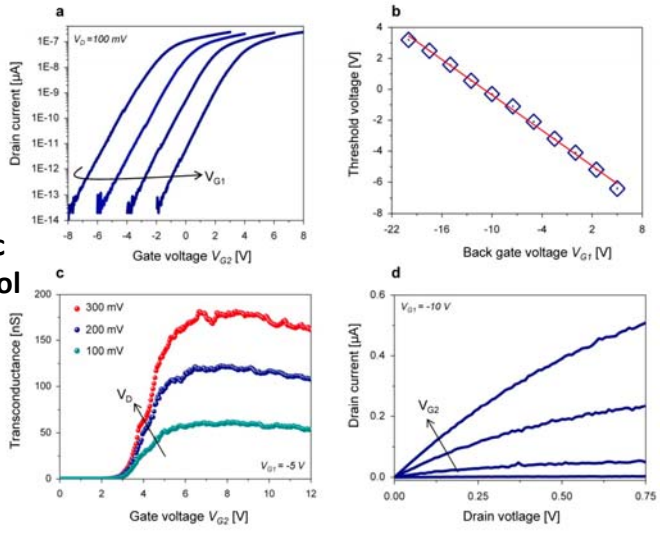




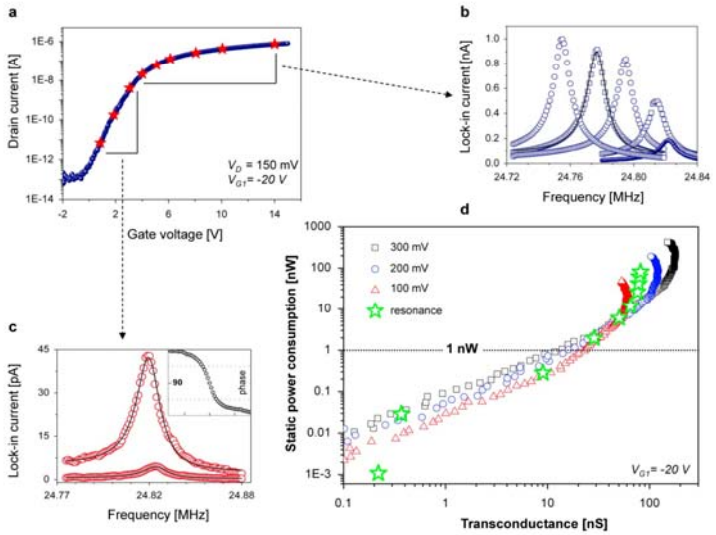
VB Fin-FET static characteristics

Excellent DG airgap FinFET:

- Ion/Ioff >10^7
- S ~300mV/dec
- DG gate control
- tunable VT
- saturated output



Vibrating body Fin-FET: power & gain trade-off



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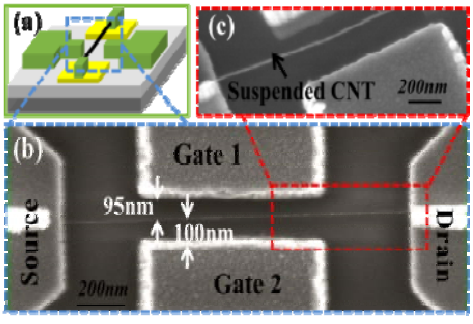
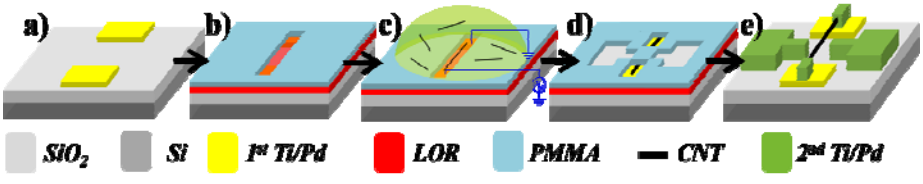
Suspended Body Double Gate CNT FET

Device concept:
- SW CNT instead of Si
- fres ~100MHz-1GHz
- strong piezores. Effect 2xf
- DG, 100nm airgap
- By resist-assisted DEP (>10^7 CNTs/cm^2)

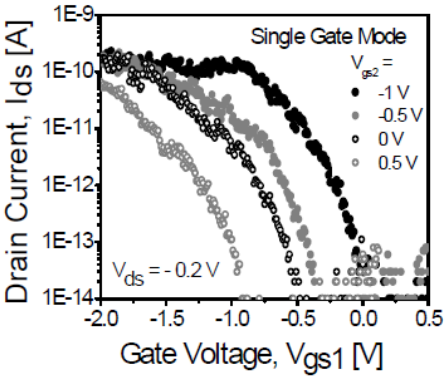


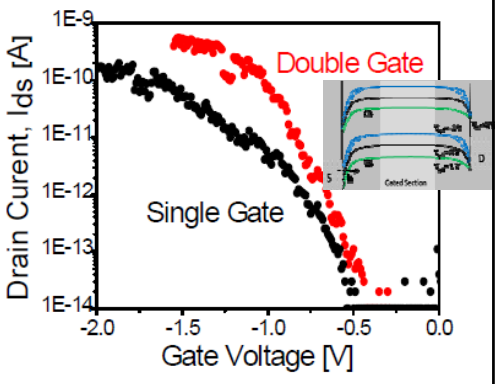


Electrical characteristics of airgap DG CNT FET

SG operation @ RT :
- S: 130 mV/decade
- Ion/Iof > 10^5

DG operation @ RT:
- improved S: 86 mV/decade
- 3x Ion and 4x gm (SB control)





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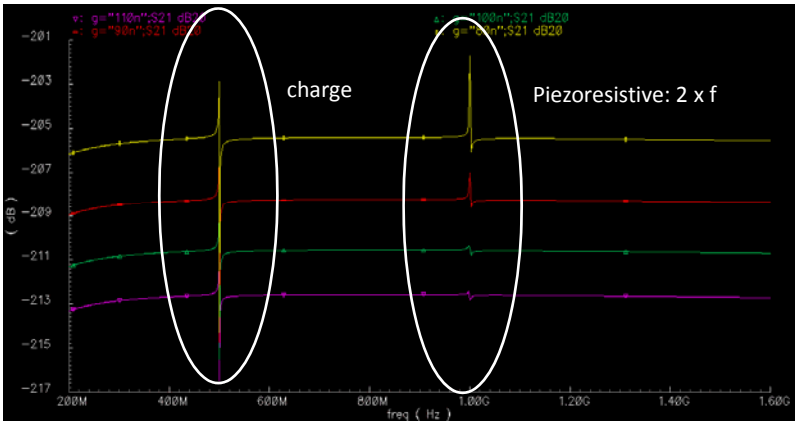
Low power GHZ resonant body DG CNT FET sensor

$$gm(\omega) = gm0 * \frac{F_{el}/\, m_{eff}}{\sqrt{(\omega^2 - \omega_0{}^2)^2 + \left(\frac{\omega\omega_0}{Q}\right)^2}}$$

Near GHz, nanoWatt integrated DG CNT FET resonant sensors



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Conclusions: benefits for low power IC design

- **Tunnel FET:**
  - logic IC's: sub-0.5V Vdd, steep inverter VTC, better noise margins, power dissipation reduction x100.
  - analog design: high gain @ 100x less power.
- **Negative capacitance FET:**
  - low voltage hysteretic switch (1T memory? analog?)
  - temperature sensor, high-temp analog IC design.
- **NEMS devices**
  - SOI VB Fin-FET: integrated sub-microWatt oscillators.
  - frequency: 100-200MHz & integrated sensor arrays
  - DG CNT FET: GHz oscillators and integrated atogram mass balances (sensor arrays)

Analytical models highly needed!

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