Compact Modeling of Ultra Deep Submicron CMOS Devices

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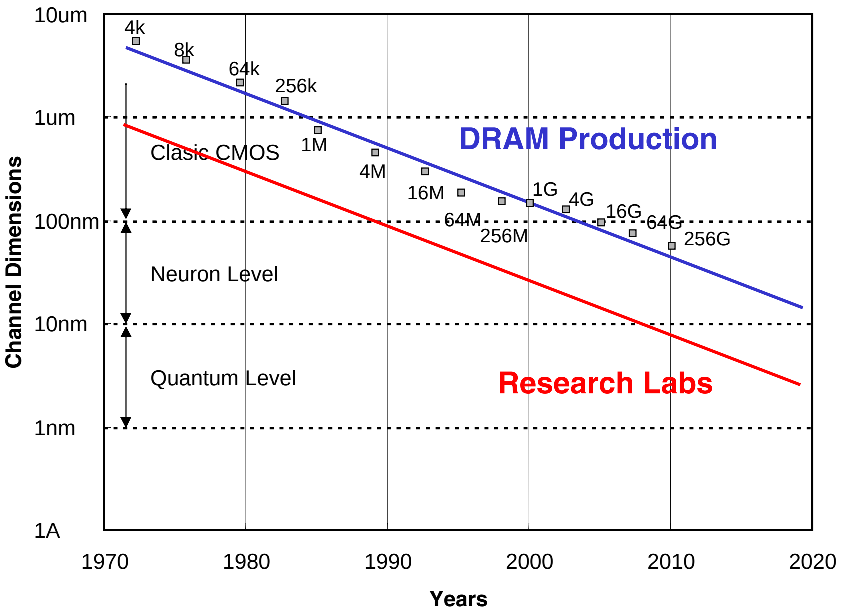
- Trends of the MOSFET Devices Scaling
- Challenges of the Compact Modeling
- The EPFL EKV v2.6 Model
  - *Model Formulation*
  - *Recent Developments*
  - *Analog and RF Application of the EKV v2.6 Model*

Trends of the MOSFET Devices Scaling



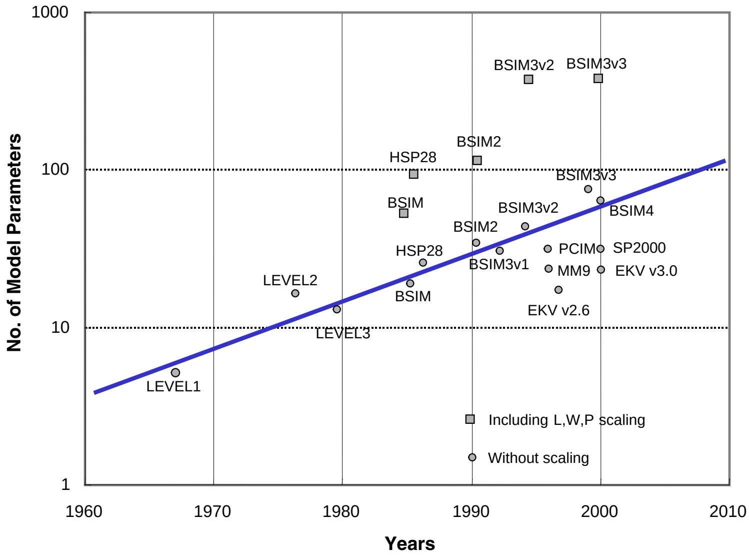
- Predictable Moor’s Law
  - *Technology Limitations*
  - *Physical Limitations*

State-of-art CMOS Technology

	CL015LV	**CL015H**	**CL015LP**
Core Voltage	1.2 V	1.5 V	1.5 V
Gate Dielectric - Core- IO, Analog Option	Dual 20 Å 70/50 Å	Dual 27 Å 70 Å	Dual 27 Å 70 Å
Physical Gate	0.12 m	0.14 m	0.13 m
Contacted Metal Pitch		M1: 0.39- m M2-6: 0.48- m M7: 0.90- m	
IOFF Spec. (worst case)	< 1 nA/ m	< 1 nA/ m	< 0.005 nA/ m
Well Formation		Super-steep retrograde	
Isolation		Shallow trench isolation	
Salicide		$CoSi_2$	
Metal		AlCu or Cu, up to 7 layers	
Intermetal Dielectric		Low-K	
Via Fill		Tungsten or copper, with CMP	
Lithography		Deep UV, with phase shifting mask	

- TSMC Delivers Foundry's First 0.15 um Technology

Development of the Compact Models



- Number of DC model parameters vs. the year of the introduction of the model
  - ❐ *Significant growth of the parameter number that includes geometry (W/L) scaling*
  - ❐ *Most recent versions of the BSIM, EKV, MM and PCIM models are included*

Compact Modeling Approaches

- Regional Approach:
  - ❐ *Easy to implement short-channel effects (but empirically),*
  - ❐ *Simple implementation into simulation tools = fast execution*
  - ❐ *Models are in* ***public domain***
  - ❐ *Discontinuous and ignores quantum effects*
  - ❐ *Introduce Binning to improve scaliability*
  - ❐ *Large number of parameters*
- Surface Potential Based Approach:
  - ❐ *Most accurate,*
  - ❐ *Needs iterative solution (no analytical solution),*
  - ❐ *Complex implementation and slow execution time*
- Hybrid Approach:
  - ❐ *Combines advantages of both presented approaches*
  - ❐ *Good fitting demonstrated for 0.1um CMOS devices*

Public-domain model evolution: EKV

- Introduction of EKV model versions:

1994: *v2.0, first fully* ***continuous*** *model (12 parameters):*
- ❐ *continuous: weak/strong inversion, conduction/saturation*
- ❐ *symmetric forward/reverse operation:* ***bulk reference***
- ❐ *drain current, capacitances, thermal noise, 1/f noise, NQS model*
- ❐ *mobility, velocity saturation, CLM, short-, narrow-channel effects*

1995: *v2.3 (16 parameters):*
- ❐ *improved short-channel effects and RSCE, added substrate current*

1996: *new QS charge-conservative model*

1997: *v2.6, applicable to deep sub-μm $(0.18\mu m)$ (18 parameters):*
- ❐ ***coherent*** *charge-based modeling of: static, QS, NQS and noise*
- ❐ *includes matching (statistical circuit simulation)*

1999: *v2.6, new analytical NQS and polydepletion models*

2000: *v3.0, has been announced*

EKV v2.6 MOSFET Model

- EKV v2.6 available in major commercial circuit simulators:
  - ❐ *Antrim-AMS, Aplac, Eldo-Accusim, PSpice, Saber, SmartSpice, Smash, Spectre-RF, Star-HSpice.*
  - ❐ *on-going implementations:*

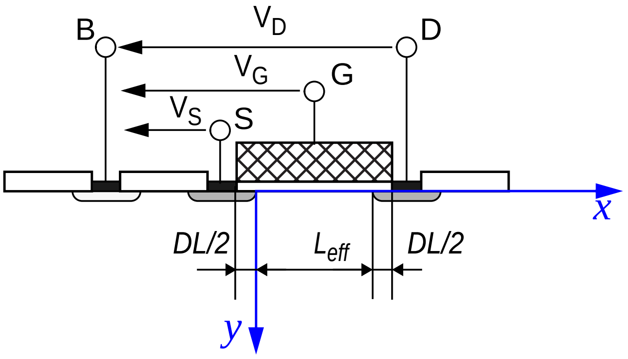
    ADS,

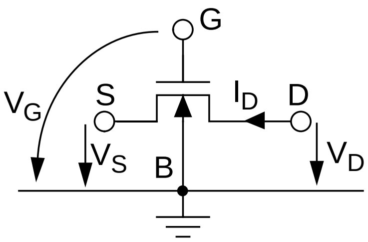
    MacSpice, Spice3, T-Spice,

    MINIMOS (TU Vienna),

    TRANZ-TRAN (TU Budapest)
- Visit: EKV model web site: <http://legwww.epfl.ch/ekv>

Charge-based Static Model





- Bulk-reference, symmetric model structure.
- Drain current expression including drift and diffusion:

$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch} = \beta \cdot \int_{V_S}^{\infty} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch} - \beta \cdot \int_{V_D}^{\infty} \left(\frac{-Q'_I}{C'_{ox}}\right) \cdot dV_{ch} = I_F - I_R \qquad (1)$$

where: $\beta = \mu \cdot C'_{ox} \cdot \frac{W_{eff}}{L_{eff}}$

Drain Current Normalization and Pinch-off Voltage

- Current normalization using the **Specific current** I_S:

$$I_D = I_F - I_R = I_S \cdot (i_f - i_r) = 2n\beta U_T^2 \cdot (i_f - i_r) \qquad (2)$$

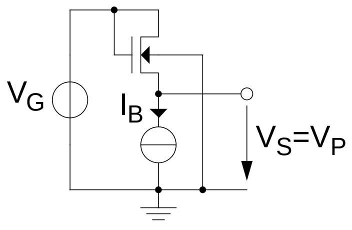
- **Pinch-off voltage** V_P accounts for...
  - ❒ ***threshold voltage*** V_{TO} *and* ***substrate effect*** $\gamma = (\sqrt{2q\varepsilon_s N_{sub}})/C'_{ox}$

$${}_P = V_G - V_{TO} - \gamma \cdot \left[\sqrt{V_G - V_{TO} + \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)^2} - \left(\sqrt{\Psi_0} + \frac{\gamma}{2}\right)\right. \qquad (3)$$

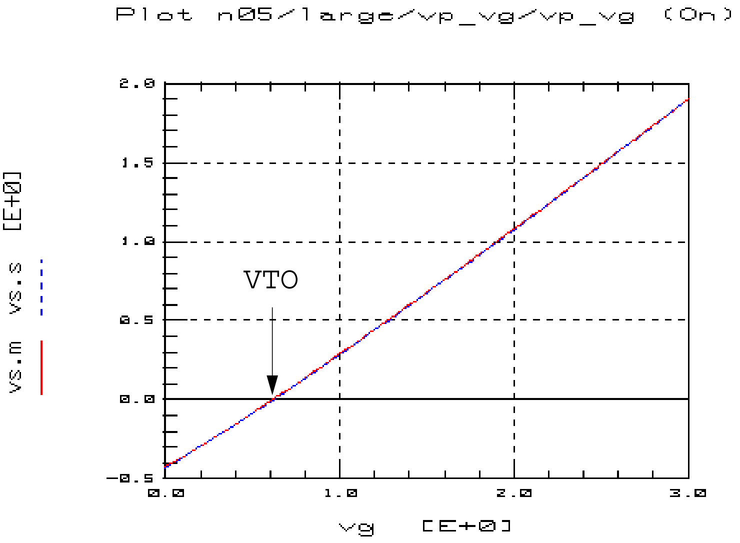
- **Slope factor** n:

$$n = \left[\frac{\partial V_P}{\partial V_G}\right]^{-1} = 1 + \frac{\gamma}{2\sqrt{\Psi_0 + V_P}} \qquad (4)$$

Pinch-off Voltage Characteristic



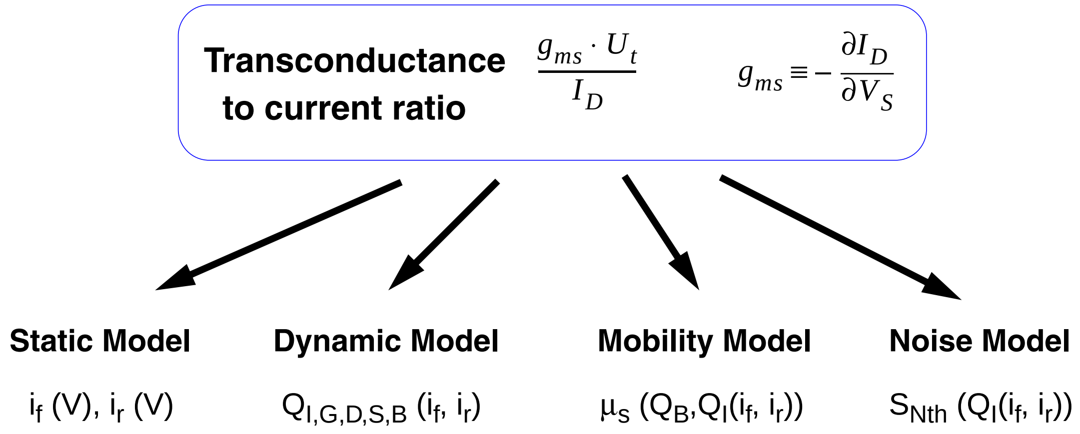
$$I_B \cong \frac{I_S}{2} = n \cdot \beta \cdot U_T^2$$



- Pinch-off voltage measurement at constant current (I_S/2)
  - ❒ *Gate voltage V_G is swept and V_P=V_S is measured at the source for a transistor biased in moderate inversion and saturation*

EKV v2.6 Model Structure

- Coherent model for static, dynamic and noise aspects.
  - ❒ *physical model basis leads to accurate description of transconductance-to-current ratio at all current levels*
  - ❒ *allows to derive all other model quantities in a coherent way*



Transconductance to current ratio $\frac{g_{ms} \cdot U_t}{I_D}$ $g_{ms} \equiv -\frac{\partial I_D}{\partial V_S}$

Static Model i_f (V), i_r (V)

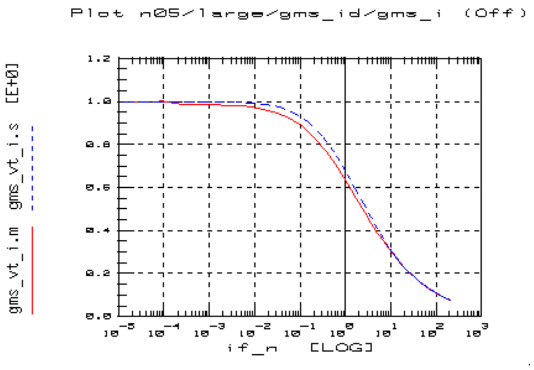
Dynamic Model $Q_{I,G,D,S,B}$ (i_f, i_r)

Mobility Model μ_S (Q_B,Q_I(i_f, i_r))

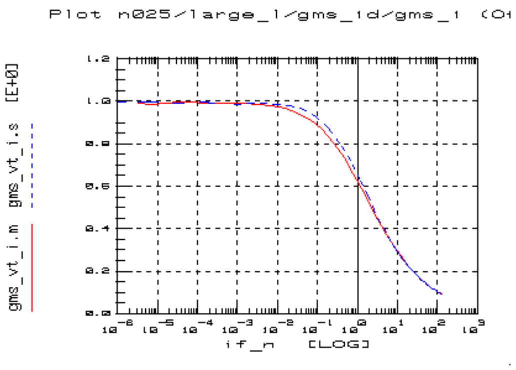
Noise Model S_{Nth} (Q_I(i_f, i_r))

  - ❒ *common variables to the entire model:* *normalized currents i_f and i_r (forward and reverse)*

Transconductance to Current Ratio



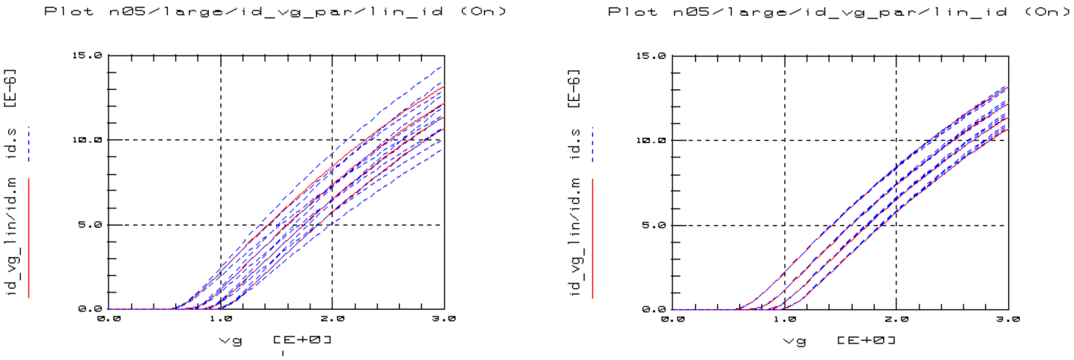
0.5um CMOS example



0.25um CMOS example

- Normalized transconductance-to-current ratio $g_{ms} \cdot U_T / I_D$ vs. normalized current $_D / I_S$ from weak thru moderate to strong inversion.
- Measurement and simulation comparisons show that g_{ms}/I_D ratio is technology independent.

Mobility Model



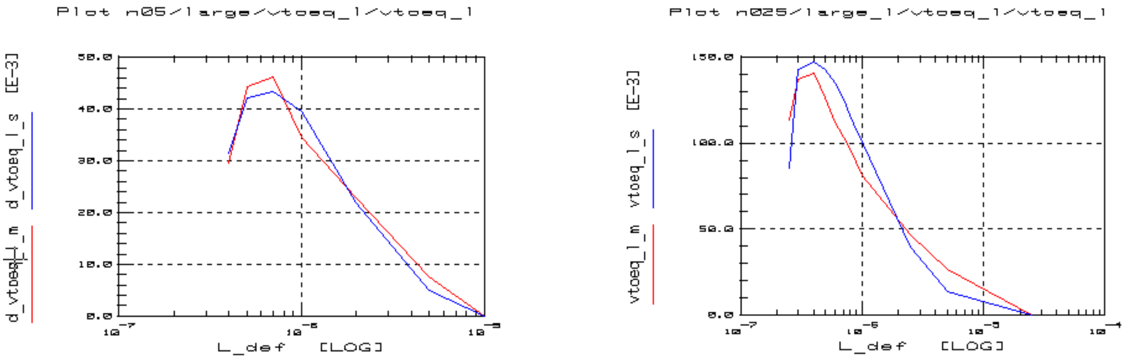
Influence of `KP` and `E0`, respectively, on the transfer characteristic (low V_{DS})

- Field- and position-dependent mobility:

$$\mu(x) = \frac{\mu_0'}{1 + \frac{E_{eff}(x)}{\mathrm{E0}}} \qquad \text{where:} \quad E_{eff}(x) = \frac{Q'_B(x) + \eta \cdot Q'_{inv}(x)}{\varepsilon_0 \varepsilon_{si}} \tag{5}$$

- One parameter: `E0` vertical critical field in the oxide
  - ❐ *No back-bias dependence needed due to inclusion of bulk charge*

Reverse Short Channel Effect (RSCE)

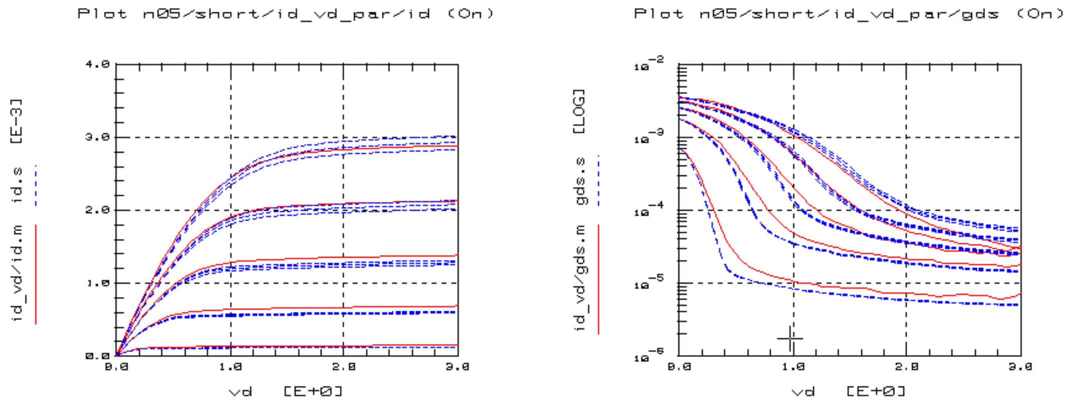


0.5um CMOS example

0.25um CMOS example

- Defect enhanced diffusion during fabrication leads to RSCE
- RSCE is modeled as a change in the threshold voltage depending on L_{eff}
- Two model parameters `Q0` and `LK`

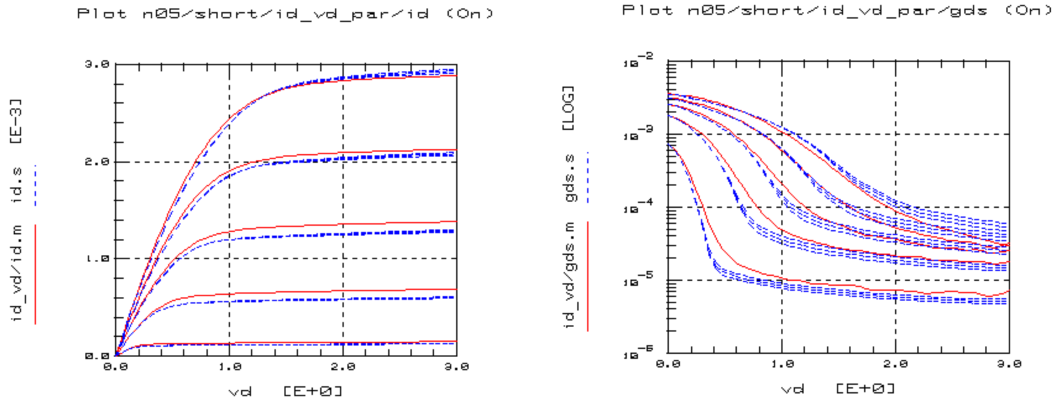
Velocity Saturation



Influence of `UCRIT` on the output characteristics

- A high lateral electric field in the channel causes the carrier velocity to saturate and limits the drain current.
- Parameter `UCRIT` accounts for this effect.

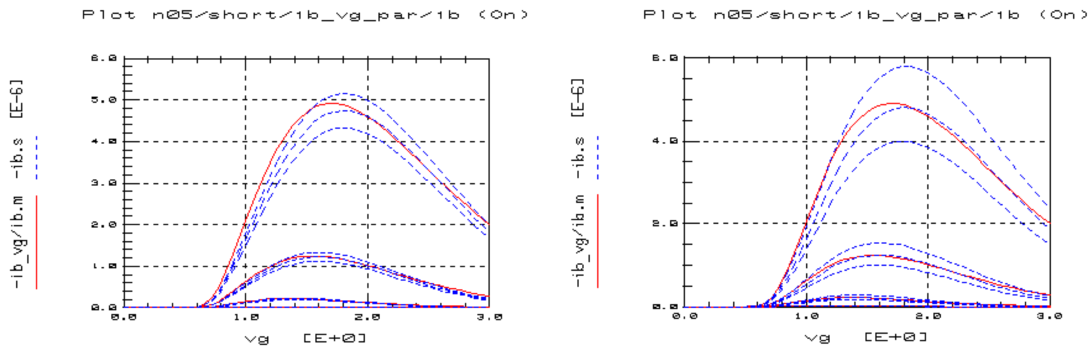
Channel-Length Modulation (CLM)



Influence of `LAMBDA` on the output characteristics

- The relative channel length reduction depends on
  the pinch-off point in the MOSFET channel near drain end.
- Depletion length coefficient (`LAMBDA`) models CLM effect.

Impact Ionization Current



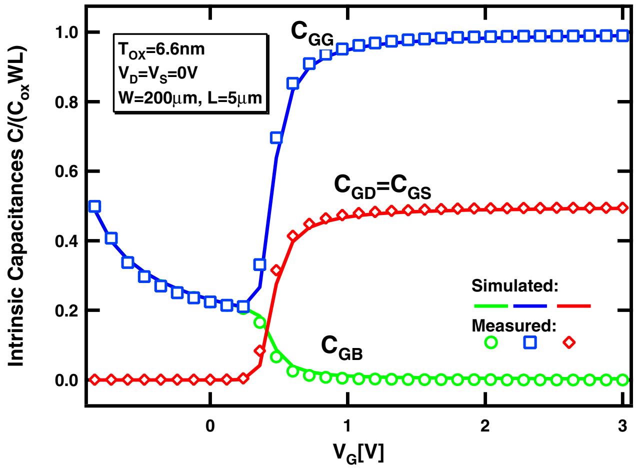
Influence of `IBA` and `IBB`, respectively, on the substrate current

- The substrate current is treated as a component of the total extrinsic current:

$$I_D = I_{DS} + I_{DB}$$

- Substrate current affects the total extrinsic conductances, in particular drain conductance (g_{DS}).

(Trans-)Capacitances Model

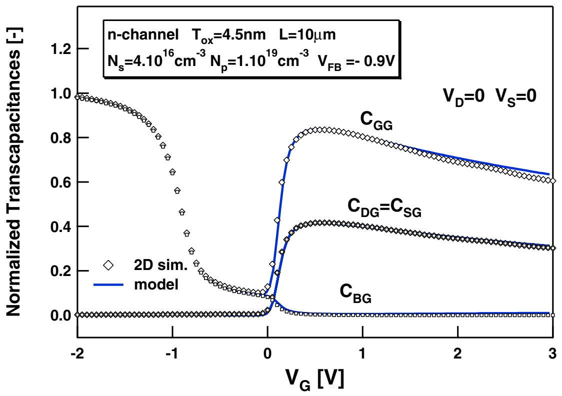


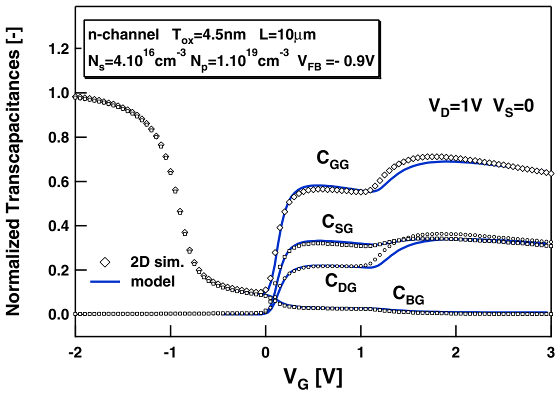
- Transcapacitances: derivation with respect to the terminal voltage:

$$C_{MN} = \pm\frac{\partial}{\partial V_N}(Q_M) \qquad M, N = G, D, S, B \tag{6}$$

  - *Accurate capacitances through all inversion levels.*
  - *Symmetric C_{GS} and C_{GD} at V_D=V_S=0.*

Polydepletion modeling





- Strengths of new polydepletion model:
  - *consistent effect from weak to strong inversion, conduction/saturation*
  - *one single extra parameter:* N_{POLY}
  - *polydepletion only affects threshold voltage* V_{TO}*, pinch-off voltage* V_P *and slope factor* n

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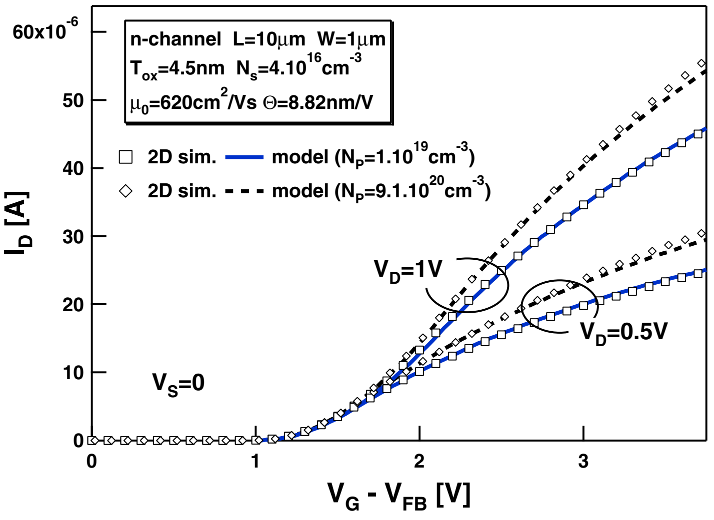
Polydepletion modeling

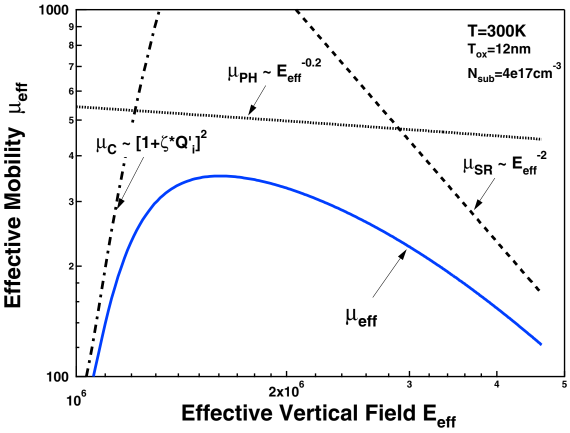


- *comparison with 2D simulation with and without polydepletion*
- *no fitting parameters: same parameters used as for CV*
- *coherent with all other aspects of charge based model (IV, CV, thermal noise)*

Vertical field dependent mobility modeling

- Deep sub-μm CMOS uses higher $N_{sub} \rightarrow$ *lower* $\mu_{\perp}$
- Mobility $\mu_{\perp}$ depends on Q_B', Q_i' (bias), N_{sub}, T
- The scattering-limited mobility depends on,
  - ❒ *Coulomb-scattering (low field) [significant in* $\sim 0.15\mu m$ *CMOS even at* ***room T****]*
  - ❒ *phonon-scattering (intermediate field)*
  - ❒ *surface-roughness scattering (high field)*
- Problem:
  - ❒ *difficult to address all dependencies together with few parameters*
  - ❒ *mobility effects are position-dependent!*
- Idea: use the charges model for modeling mobility
  - ❒ *model should have built-in temperature behaviour*

Vertical field dependent mobility modeling



$$\frac{1}{\mu_{\perp}} = \frac{1}{\mu_C} + \frac{1}{\mu_{PH}} + \frac{1}{\mu_{SR}}$$

$$\mu_C \propto N_{sub} \cdot [1 + \zeta \cdot Q'_i]^2$$

$$\mu_{PH} \propto E_{eff}{}^{-0.2}$$

$$\mu_{SR} \propto E_{eff}{}^{-2}$$

$$E_{eff} = |Q'_B + \eta \cdot Q'_i| / \varepsilon_{si}$$

- Strengths of new mobility model:
  - ❒ *directly linked to charges model*
  - ❒ *position- (and bias-) dependence accounted for by integration along channel*
  - ❒ *few parameters (5, none required for bias-dependence)*

Velocity saturation modeling

- Velocity saturation is the main cause of I_D reduction in short-channel MOS transistors
- NMOS and PMOS transistors have different $\mu(E_{\parallel})$ relationships
    - *NMOS is much more strongly affected by velocity saturation than PMOS*

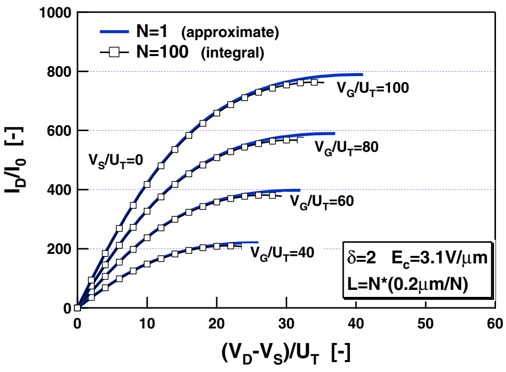
$$\mu = \frac{\mu_{\perp}}{\sqrt{1+(E_{\parallel}/E_c)^2}} \text{ (NMOS); } \mu = \frac{\mu_{\perp}}{1+E_{\parallel}/E_c} \text{ (PMOS)}$$

- Velocity saturation modeling has many implications:
    - *bias-dependence*
    - *scaling*
    - *asymptotic behaviour:*

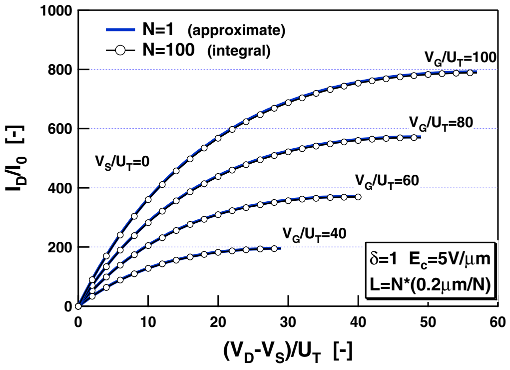
        series connection of multiple devices

        asymptotic behaviour at $V_{DS} \rightarrow 0$

Velocity saturation modeling



NMOS



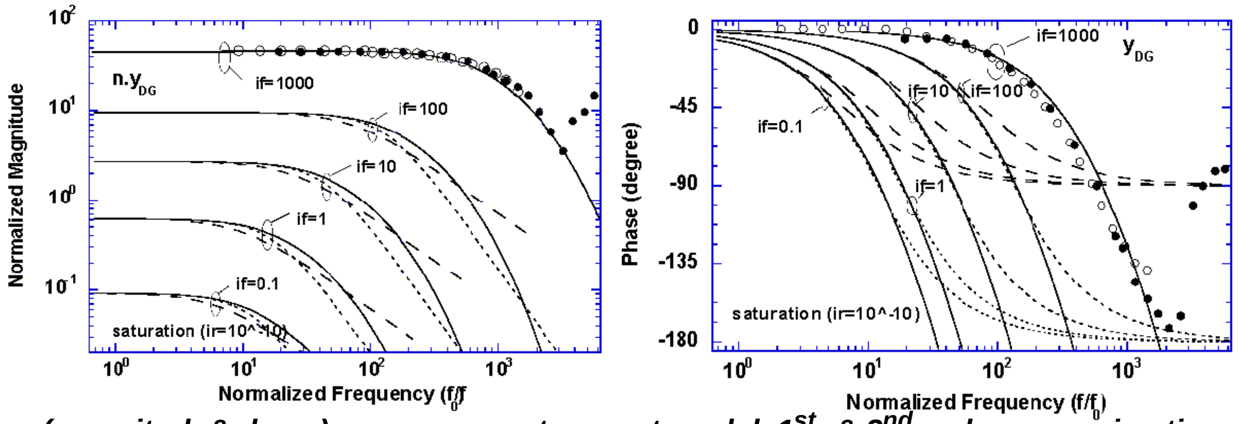
PMOS

- Strengths of new velocity saturation model:
    - *charge-based, from strong to weak inversion*
    - *correct multiple series devices behaviour*
    - *improved scaling*
    - *correct asymptotic behaviour at* $V_{DS} \rightarrow 0$

Non-quasistatic (NQS) AC modeling

- New physics-based NQS model
- Exact analytical solutions for complex transadmittances
    - *1st and 2nd-order approximations*
    - *«0-order» approximation: coincides with QS model!*
- No additional parameters
- Normalization of different quantities:
    - *normalized Currents, Potentials, Charges*
    - *normalized Coordinates, Time, Frequency*

Non-quasistatic (NQS) AC modeling



y_{DG} (magnitude&phase), measurements, exact model, 1^{st}- & 2^{nd}-order approximations

- Strengths of new NQS model:
    - *valid from strong through moderate to weak inversion*
    - *simple analytical expressions for (complex) transadmittances*
    - *entirely consistent with polydepletion, mobility model, etc.*
    - *easy to implement in circuit simulators (access to complex admittances matrix)*

EKV v2.6 Parameter Set

■ 18 Intrinsic Model Parameters

Purpose	NAME	DESCRIPTION	UNITS	EXAMPLE
Process parameters	COX	gate oxide capacitance per unit area	F / m^2	3.45E-3
	XJ	junction depth	m	0.15E-6
	DW	channel width correction	m	-0.05E-6
	DL	channel length correction	m	-0.1E-6
Doping & Mobility related parameters	VTO	long-channel threshold voltage	V	0.55
	GAMMA	body effect parameter	$\sqrt{V}$	0.7
	PHI	bulk Fermi potential (*2)	V	0.8
	KP	transconductance parameter	A / V^2	160E-6
	E0	vertical characteristic field for mobility reduction	V / m	80E6
	UCRIT	longitudinal critical field	V / m	4.0E6
Short- & narrow-channel effect parameters	LAMBDA	depletion length coefficient (channel length modulation)	-	0.3
	WETA	narrow-channel effect coefficient	-	0.1
	LETA	short-channel effect coefficient	-	0.3
	Q0	reverse short-channel effect peak charge density	$A \cdot s / m^2$	500E-6
	LK	reverse short-channel effect characteristic length	m	0.34E-6
Substrate current related parameters	IBA	first impact ionization coefficient	$1 / m$	260E6
	IBB	second impact ionization coefficient	V / m	350E6
	IBN	saturation voltage factor for impact ionization	-	1.0

EKV v2.6 Parameter Set (cont.)

■ Completed with 3 matching parameters

NAME	DESCRIPTION	UNITS	Example
AVTO	area related threshold voltage mismatch parameter	Vm	- DEV=15E-9
AKP	area related gain mismatch parameter	m	- DEV=25E-9
AGAMMA	area related body effect mismatch parameter	$\sqrt{V}m$	- DEV=10E-9

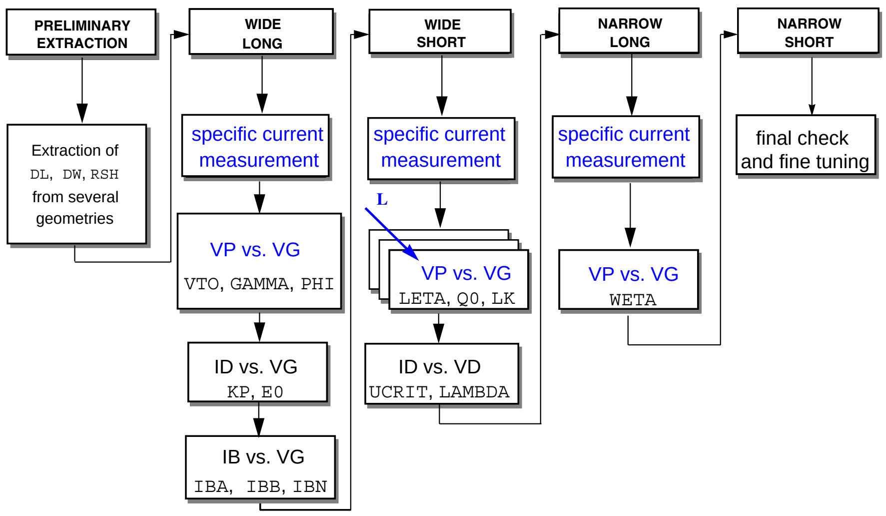
■ 4 temperature parameters

NAME	DESCRIPTION	UNITS	Example
TCV	threshold voltage temperature coefficient	V/K	1.0E-3
BEX	mobility temperature exponent	-	-1.5
UCEX	longitudinal critical field temperature exponent	-	0.8
IBBT	temperature coefficient for IBB	1/K	9.0E-4

■ 2 noise parameters

NAME	DESCRIPTION	UNITS	Example
KF	flicker noise coefficient	-	0
AF	flicker noise exponent	-	1

EKV v2.6 Parameter Extraction Methodology



PRELIMINARY EXTRACTION

Extraction of `DL, DW, RSH` from several geometries

WIDE LONG

specific current measurement

VP vs. VG
`VTO, GAMMA, PHI`

ID vs. VG
`KP, E0`

IB vs. VG
`IBA, IBB, IBN`

WIDE SHORT

specific current measurement

L

VP vs. VG
`LETA, Q0, LK`

ID vs. VD
`UCRIT, LAMBDA`

NARROW LONG

specific current measurement

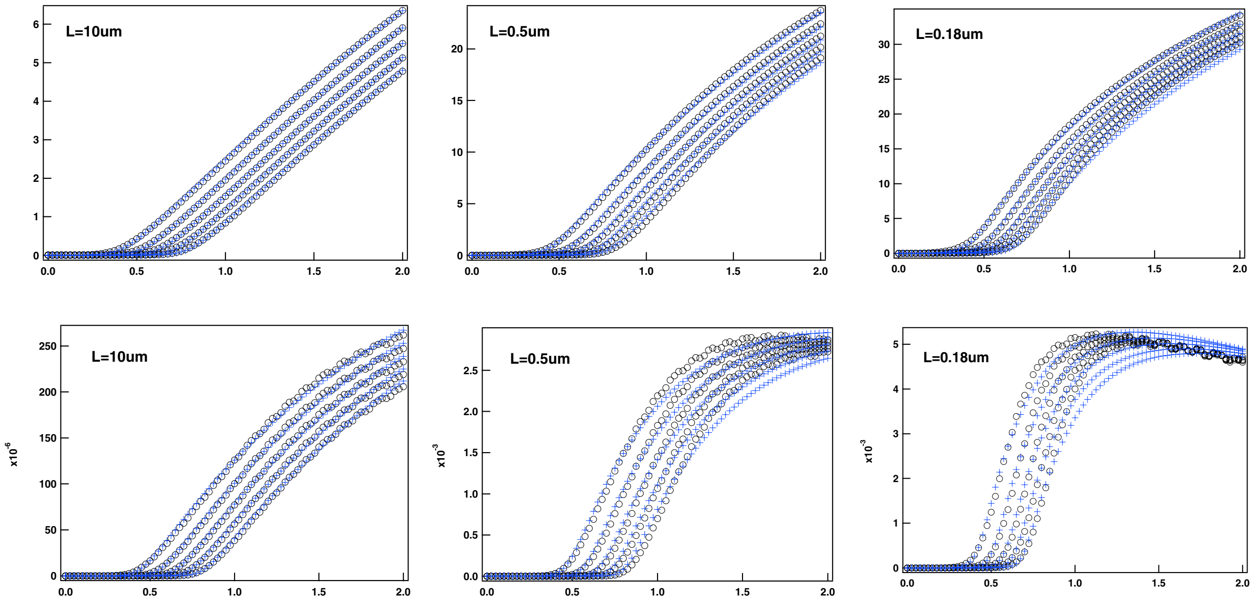
VP vs. VG
`WETA`

NARROW SHORT

final check and fine tuning

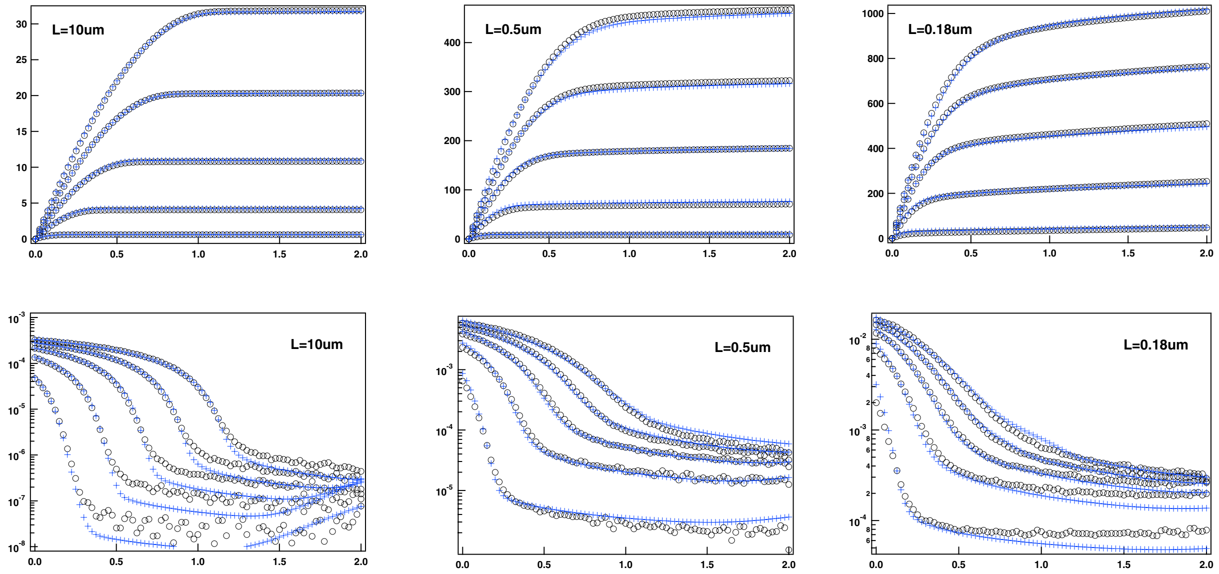
- Sequential task: parameter extraction methodology established for EKV v2.6
  - *performed using an array of transistors in the W/L plane.*

EKV v2.6 - 0.18um CMOS



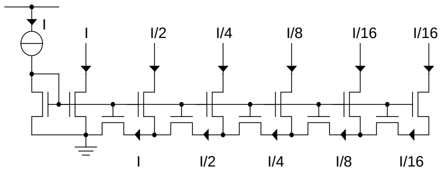
- Transfer characteristics IdVg and gmgVg (low drain voltage Vd)

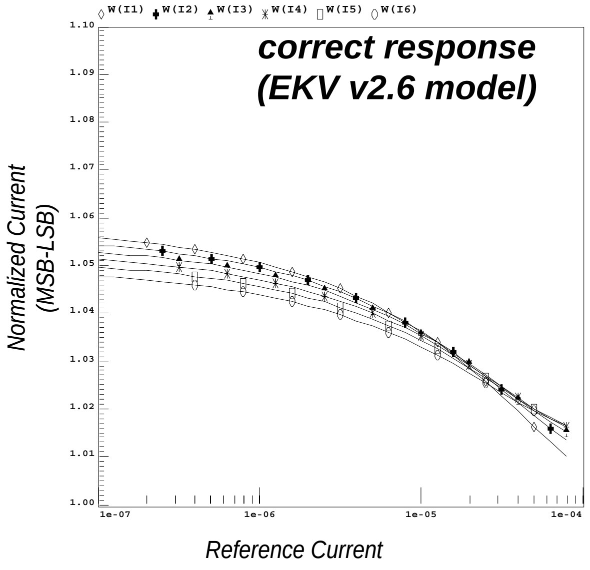
EKV v2.6 - 0.18um CMOS

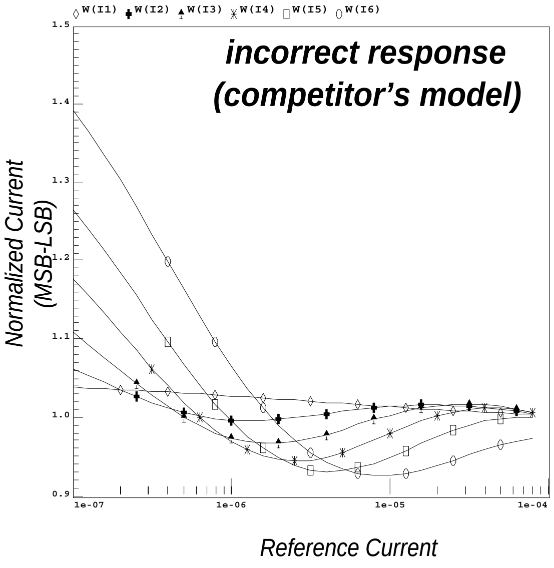


- Output characteristics IdVd and gdsVd.

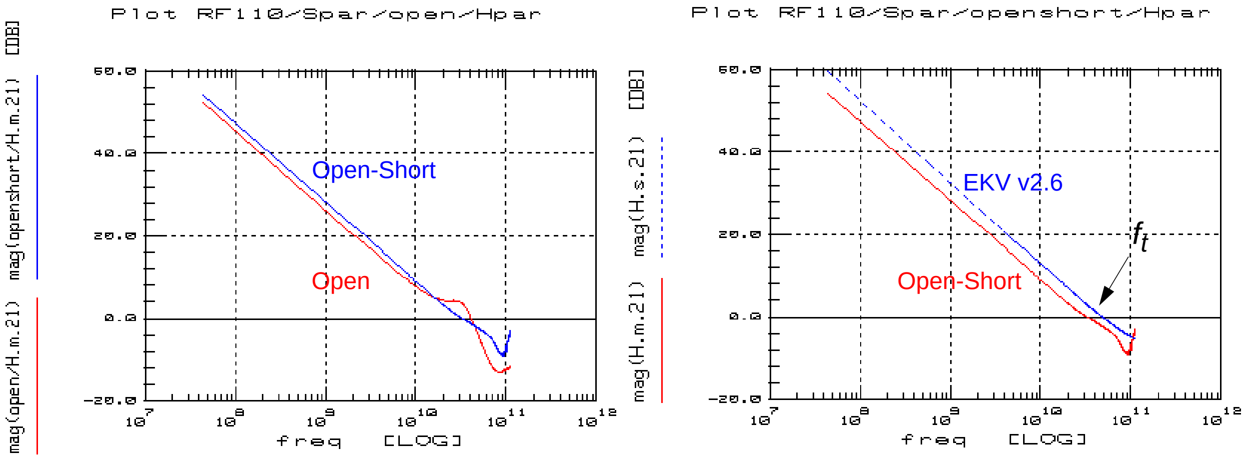
D/A Converter Circuit





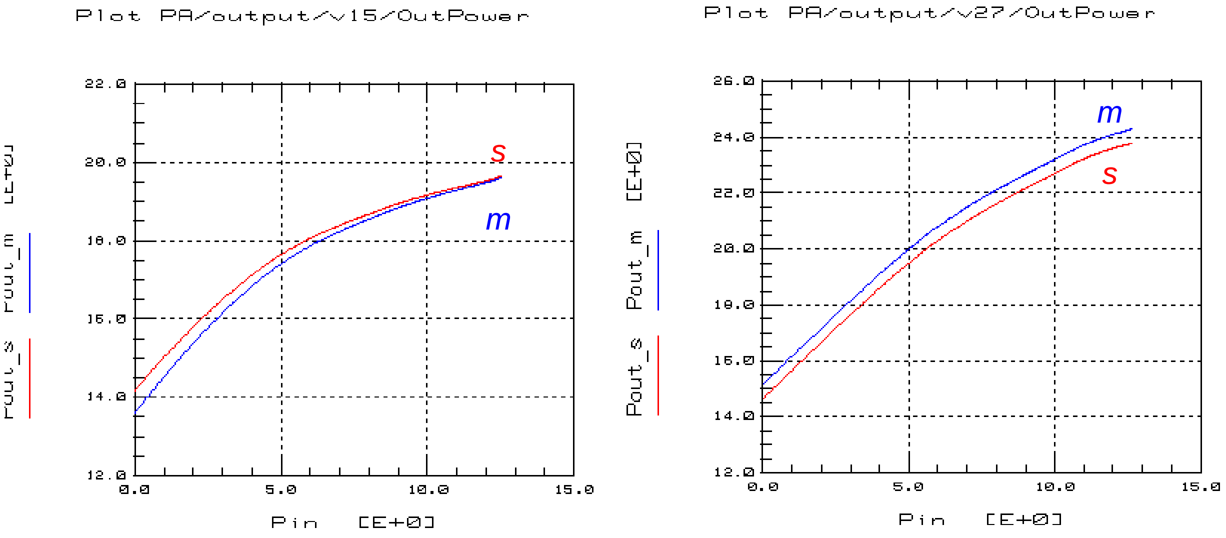


RF Characterization: De-embedding



- Open, Open-Short deembedding and simulation data up to 110GHz
    - *nMOSFET Device: 30 x 20um/0.35um*
    - *Bias condition: V_g=1.0V, V_d=1.0V*

RF Power Amplifier

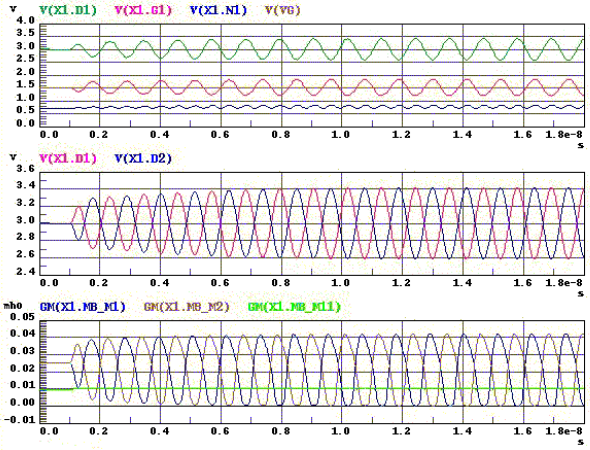


a) V_{supply}=1.5V *b) V_{supply}=2.7V*

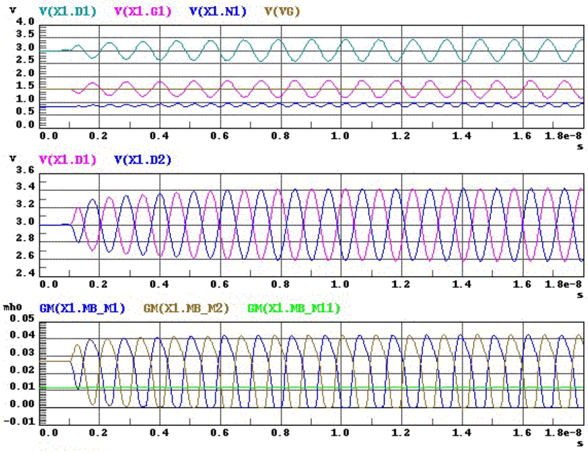
- Output power vs. input power characteristics (in dBm)
    - *a) supply voltage V_{supply}= 1.5V*
    - *b) supply voltage V_{supply}= 2.7V*

Harmonic Oscillator

MM9



EKV v2.6



- Simulation results: MM9 vs. EKV v2.6

Summary

- EPFL EKV v2.6 MOST model is a charge-based compact model
  - *Continuous, physics-based model valid for all bias conditions.*
  - *Includes charge-based static and dynamic models, and noise.*
  - *Uses a low number of parameters*
- EPFL-EKV model enables the simulation of ultra deep submicron CMOS integrated systems, from DC to RF
  - *Experimental validation down to 0.18um CMOS*
  - *Circuit applications have been presented*
- The model and related parameter extraction methodology have been developed at Electronics Labs of EPFL
  - *Web resource: <http://legwww.epfl.ch/ekv>*
- Parameter extraction services and design support are available through Smart Silicon Systems, Lausanne
  - *Contact: modeling@smartsilicon.ch*