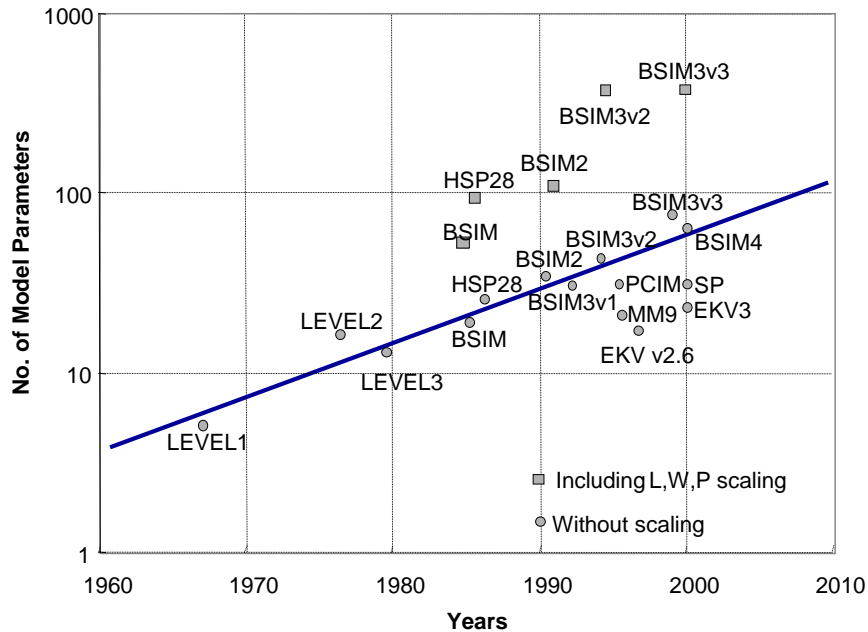

EKV v2.6 Parameter Extraction Tutorial

Wladyslaw Grabinski
GMC

Tutorial Outline

- Developments of the Compact Models
- EKV v2.6 MOSFET Model
 - Modeled Effects
 - Model Structure
 - Parameter set
- Parameter Extraction Methodology
 - Specific Current Extraction
 - Pinch-off Voltage Characteristic
 - Reverse Short Channel Effect (RSCE)
 - Mobility Model
 - Velocity Saturation
 - Channel-Length Modulation (CLM)
 - Impact Ionization Current
- Extraction Example: 0.18um CMOS
- EKV3: Extended Deep Submicron Model
- Summary
- Appendix
- References

Developments of the Compact Models



- Number of DC model parameters vs. the year of the introduction of the model
 - Significant growth of the parameter number that includes geometry (W/L) scaling
- Most recent versions of the EKV, PCIM and SP models are included

EKV Model Versions

1994: v2.0, first fully continuous model (12 parameters):

- *continuous: weak/strong inversion, conduction/saturation*
- *symmetric forward/reverse operation: bulk reference*
- *drain current, capacitances, thermal noise, 1/f noise, NQS model*
- *mobility, velocity saturation, CLM, short-, narrow-channel effects*

1995: v2.3 (16 parameters):

- *improved short-channel effects, added substrate current*

1996: new QS charge-conservative model (MOS-AK meeting, Nov. 96, Bremen)

1997: v2.6, applicable to deep submicron (0.25 μ m) (18 parameters):

- **coherent** charge-based modeling of: *static, QS, NQS effects and thermal noise*
- *reverse short-channel effect (RSCE)*
- *includes matching (statistical circuit simulation)*

1999: v2.6, analytical NQS and polydepletion models

2000: EKV3 introduction (MOS-AK meeting, May 2000, Lausanne)

EKV v2.6 MOSFET Model

EKV v2.6 in summary:

- a **physics based** MOSFET model in the **public domain**.
- Design driven modeling concept dedicated to **analog circuit simulation** of submicron CMOS circuits.
- has < 20 intrinsic model parameters.
- used in industrial and academic design groups

EKV v2.6 available in major commercial circuit simulators:

AMI-spice, Antrim-AMS, Aplac, Eldo-Accusim, Intosoft, Hsim, LTspice, MacSpice, Microsim-CapV, PSpice, NanoSpice, NG-spice, Saber, SmartSpice, Smash, Spice-Opus, Spectre, Star-HSpice, Synopsis, Spice3, WinSpice.

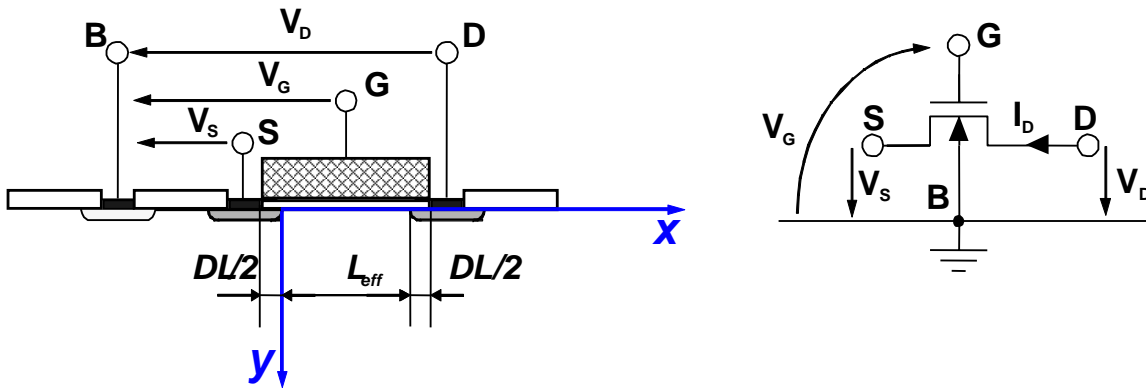
on-going implementations:

ADS & ICCAP, T-Spice, MINIMOS (TU Vienna), TRANZ-TRAN (TU Budapest)

EKV v2.6 Modeled Effects

- Physics-based modeling of weak, moderate and strong inversion.
- Effects of substrate doping level, substrate effect.
- Vertical field dependent mobility.
- Common short-channel effects:
 - *velocity saturation*
 - *channel length modulation (CLM)*
 - *two-dimensional bulk charge-sharing for short-and narrow-channel effects*
 - *reverse short-channel effect (RSCE)*
 - *substrate current effects on drain conductance*
- Short-distance matching for statistical circuit simulation.

EKV v2.6 Model Structure



Bulk-reference, symmetric model structure.

Drain current expression including drift and diffusion:

$$I_D = \beta \int_{V_S}^{V_D} \left(\frac{-Q'_I}{C'_{OX}} \right) \cdot dV_{CH} = \beta \int_{V_S}^{\infty} \left(\frac{-Q'_I}{C'_{OX}} \right) \cdot dV_{CH} - \beta \int_{V_D}^{\infty} \left(\frac{-Q'_I}{C'_{OX}} \right) \cdot dV_{CH} = I_F - I_R$$

where:

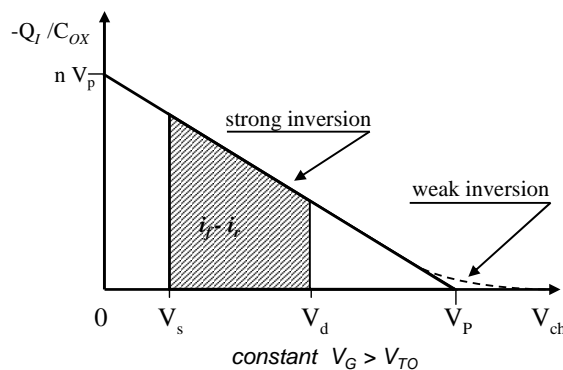
$$\beta = \mu \cdot C_{OX} \frac{W_{eff}}{L_{eff}}$$

EKV v2.6 Model Structure

A simple and useful relation can then be obtained between the inversion charge density and the surface potential in a differential form:

$$dQ'_I / C'_{OX} = n \cdot d\psi_S$$

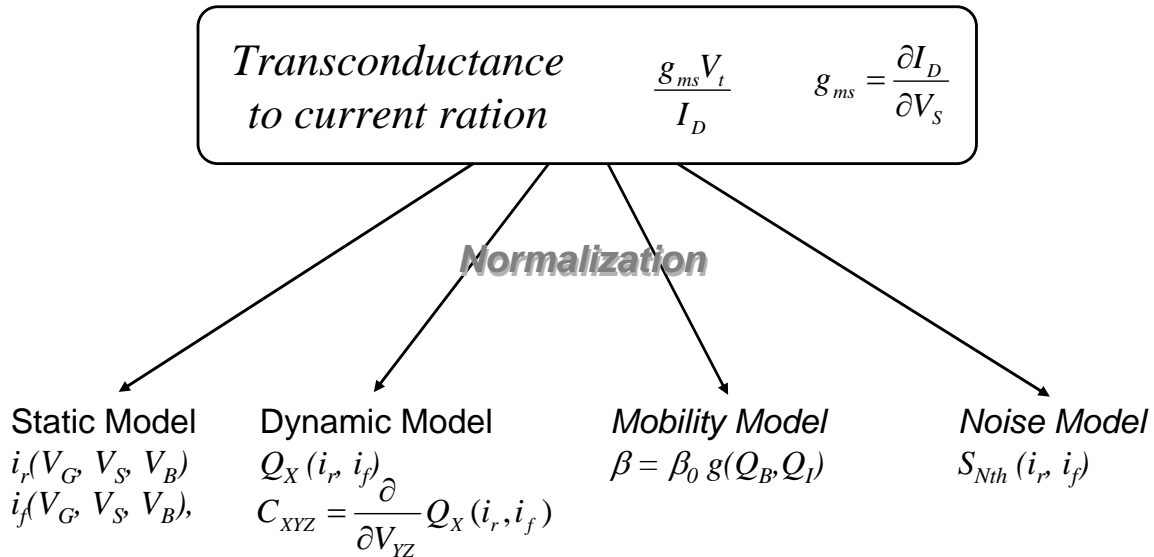
Consequently, the EKV model can also be considered as a surface potential based model



- Schematic representation of the normalized inversion charge density as a function of the channel voltage.
- Pinch-off voltage V_P used in calculation of currents and charges

EKV v2.6 Model Structure (cont.)

Physical model basis leads to accurate description of transconductance-to-current ratio at all current levels allows coherent derivation of all model quantities including static, dynamic and noise modeling aspects.



EKV v2.6 Parameter set

18 Intrinsic Model Parameters:

Purpose	Name	Description	Units	Example
Process parameters	COX	gate oxide capacitance per unit area	F/m ²	3.45E-3
	XJ	junction depth	m	0.15E-6
	DW	channel width correction	M	-0.05E-6
	DL	channel length correction	M	-0.1E-6
Doping & Mobility related parameters	VTO	long-channel threshold voltage	V	0.55
	GAMMA	body effect parameter	V ^{1/2}	0.7
	PHI	bulk Fermi potential (*2)	V	0.8
	KP	transconductance parameter	A/V ²	160E-6
	E0	vertical characteristic field for mobility reduction	V/m	80E6
	UCRIT	longitudinal critical field	V/m	4.0E6
Short- & narrow-channel effect parameters	LAMBDA	depletion length coefficient (channel length modulation)	-	0.3
	WETA	narrow-channel effect coefficient	-	0.1
	LETA	short-channel effect coefficient	-	0.3
	Q0	reverse short-channel effect peak charge density	A s/m ²	500E-6
	LK	reverse short-channel effect characteristic length	m	0.34E-6
Substrate current related parameters	IBA	first impact ionization coefficient	1/m	260E6
	IBB	second impact ionization coefficient	V/m	350E6
	IBN	saturation voltage factor for impact ionization	-	1.0

EKV v2.6 Parameter Set (cont.)

4 temperature parameters:

Name	Description	Units	Example
TCV	threshold voltage temperature coefficient	V/K	1.0E-3
BEX	mobility temperature exponent	-	-1.5
UCEX	longitudinal critical field temperature exponent	-	0.8
IBBT	temperature coefficient for IBB	1/K	9.0E-4

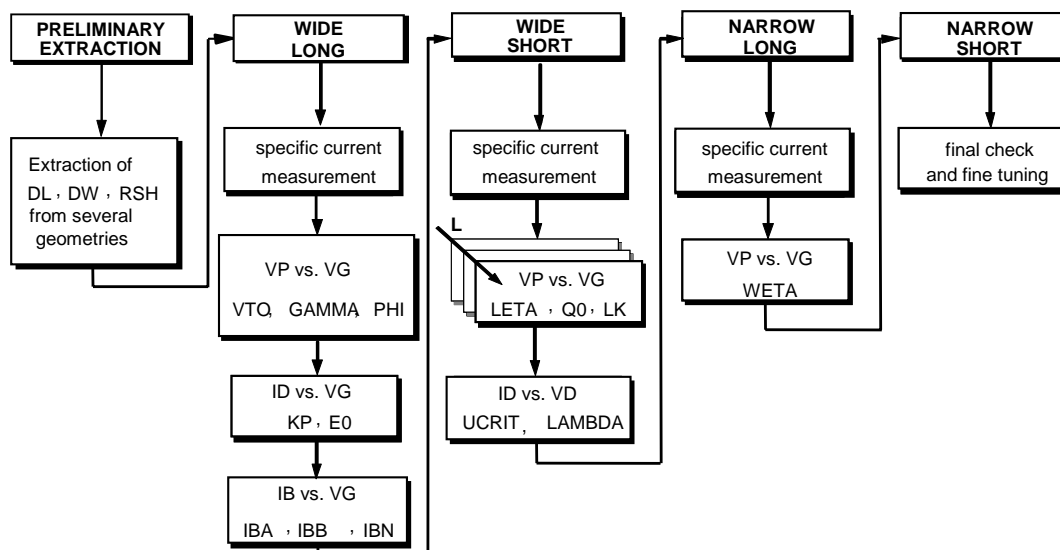
2 noise parameters:

Name	Description	Units	Example
KF	flicker noise coefficient	-	0
AF	flicker noise exponent	-	1

Completed with 3 matching parameters:

Name	Description	Units	Example
AVTO	area related threshold voltage mismatch parameter	V _m	- DEV=15E-9
AKP	area related gain mismatch parameter	m	- DEV=25E-9
AGAMMA	area related body effect mismatch parameter	V _m) ^{1/2}	- DEV=10E-9

EKV v2.6 DC Parameter Extraction Methodology



- Parameter extraction methodology established for EKV v2.6
- Sequential task performed from an array of transistors in the W/L plane.

Specific Current Extraction

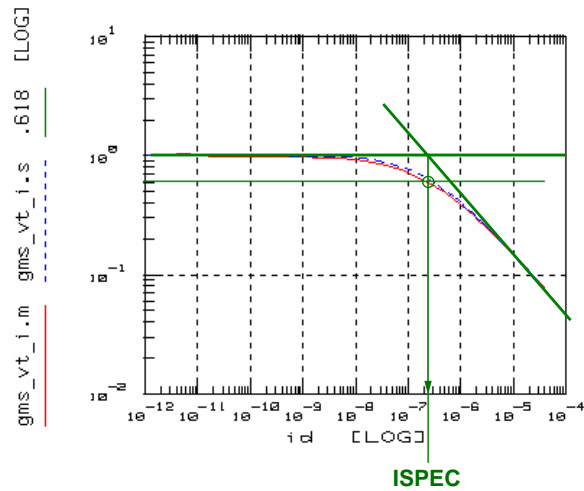
Transconductance to current ratio in saturation:

$$\frac{g_{ms} \times U_t}{I_D} = \frac{1}{\sqrt{\frac{1}{4} + \frac{I_D}{I_s} + \frac{1}{2}}}$$

Setting I_D/I_S to 1:

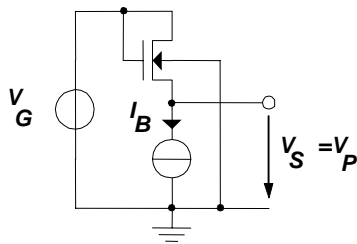
$$\frac{1}{\sqrt{\frac{1}{4} + 1 + \frac{1}{2}}} \cong 0.618$$

Plot n05/large/gms_id/gms_i (Off)



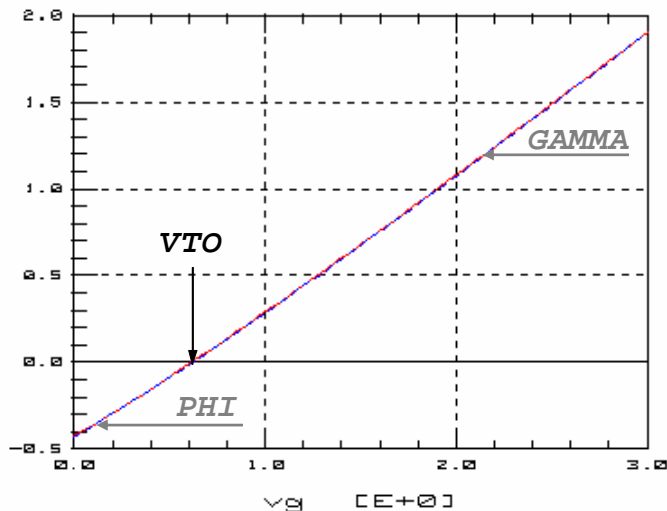
- Specific current I_{SPEC} corresponds to intersection of strong and weak inversion asymptotes
- Not affected by:
 - CLM, high field mobility reduction, S/D extrinsic resistances

Pinch-off Voltage Characteristic



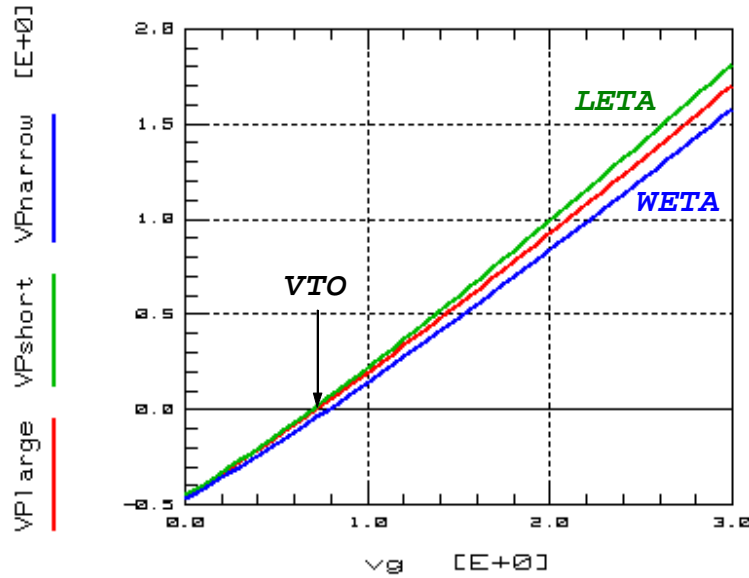
$$I_B = \frac{I_S}{2} = n \cdot \beta \cdot U_T^2$$

Plot n05/large/vp_vg/vp_vg (On)



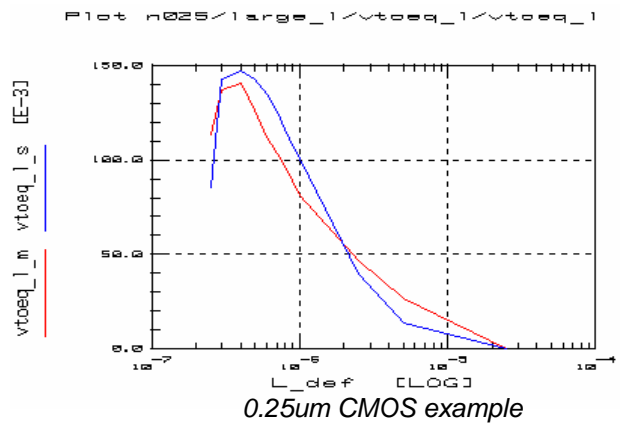
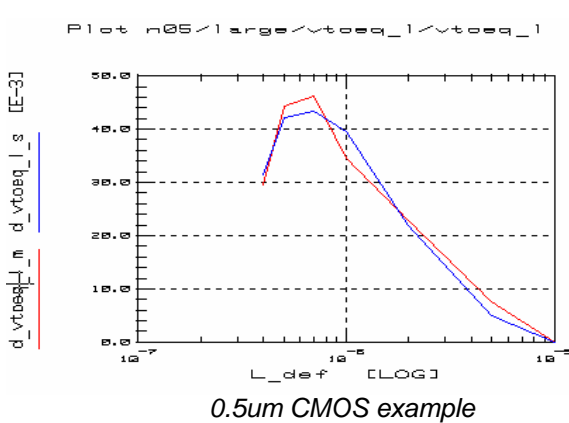
- Pinch-off voltage measurement at constant current ($I_S/2$)
- Gate voltage V_G is swept and $V_P=V_S$ is measured at the source for a transistor biased in moderate inversion and saturation

Short- and Narrow-Channel Effects on $V_p - V_g$



- Effects of short- and narrow-channels are analysed using the charge-sharing approach.
- Corresponding parameters: $LETA$ and $WETA$.

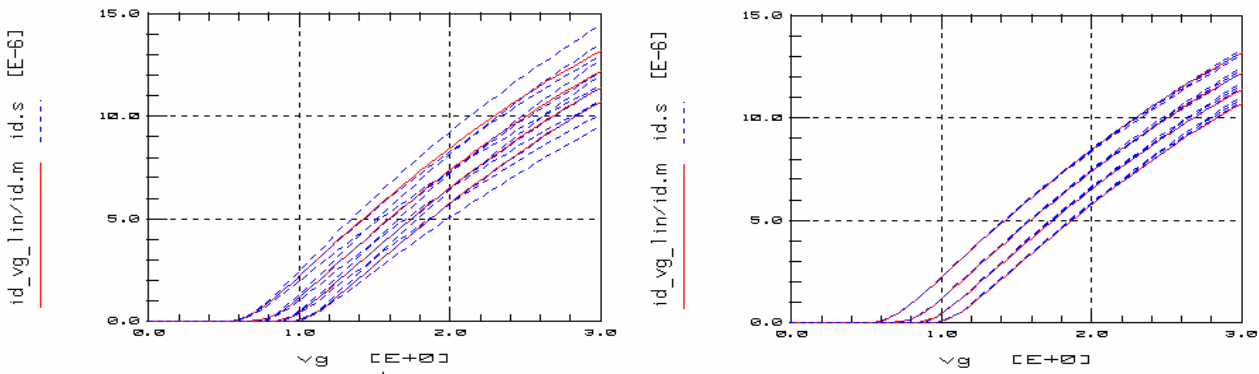
Reverse Short Channel Effect (RSCE)



- Defect enhanced diffusion during fabrication leads to RSCE.
- RSCE is modeled as a change in the threshold voltage depending on L_{eff}
- Only two model parameters $Q0$ and LK .

Mobility Model

Plot n05/large/id_vg_par/lin_id (C) Plot n05/large/id_vg_par/lin_id (On)

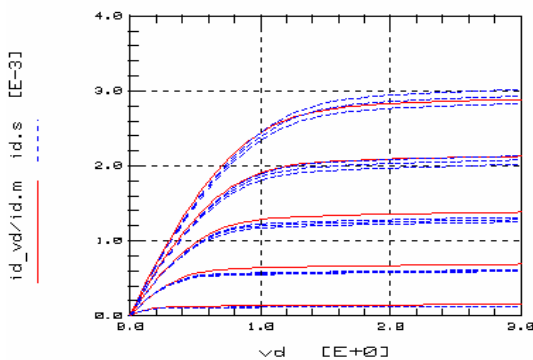


Influence of KP and $E0$ on the transfer characteristics, respectively

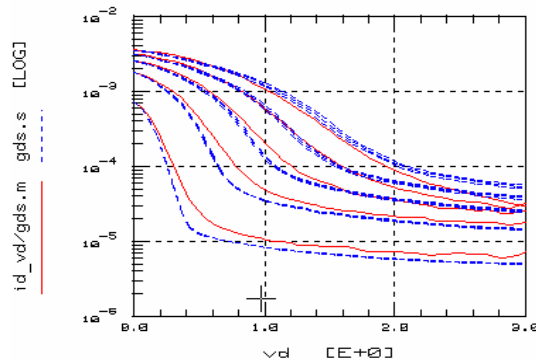
- Good behaviour for mobility reduction for both channel types.
- Substrate effect is correctly accounted for.
- No back-bias dependence required.

Velocity Saturation

Plot n05/short/id_vd_par/id (On)



Plot n05/short/id_vd_par/gds (On)

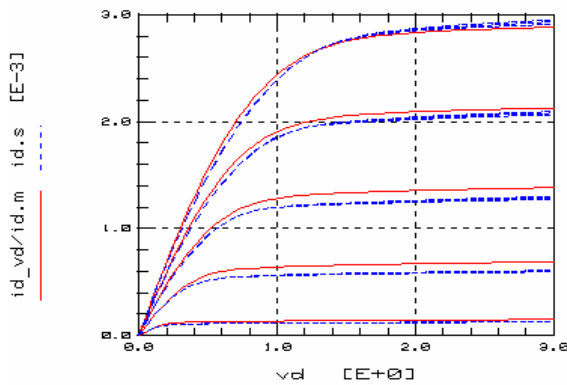


Influence of $UCRT$ on the output characteristics

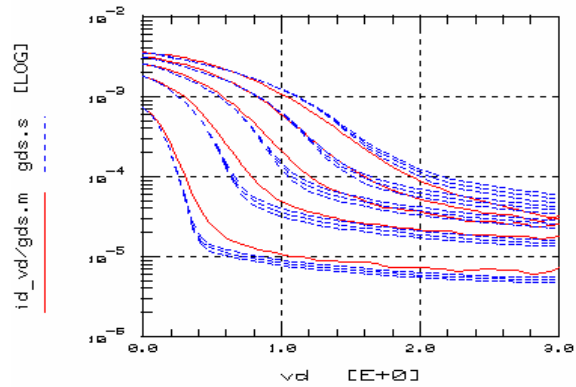
- A high lateral electric field in the channel causes the carrier velocity to saturate and limits the drain current.
- Parameter $UCRIT$ accounts for this effect.

Channel-Length Modulation (CLM)

Plot n05/short/id_vd_par/id (On)



Plot n05/short/id_vd_par/gds (On)

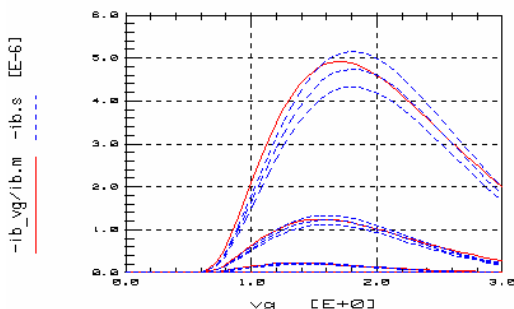


Influence of $LAMBDA$ on the output characteristics

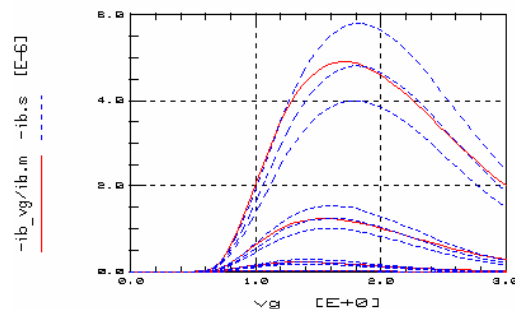
- The relative channel length reduction depends on the pinch-off point in the MOSFET channel near drain end.
- Depletion length coefficient ($LAMBDA$) models CLM effect.

Impact Ionization Current

Plot n05/short/ib_vg_par/ib (On)



Plot n05/short/ib_vg_par/ib (On)



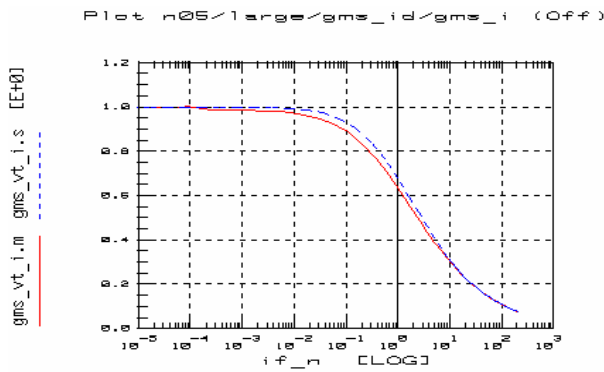
Influence of IBA and IBB on the substrate current, respectively

- The substrate current is treated as a component of the total extrinsic current:

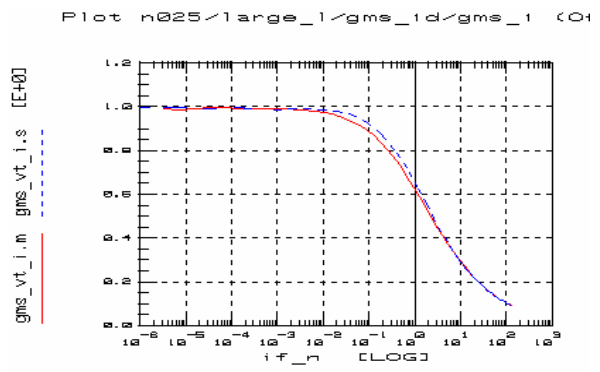
$$I_D = I_{DS} + I_{DB}$$

- Substrate current affects the total extrinsic conductances, in particular drain conductance (g_{DS}).

Transconductance to Current Ratio



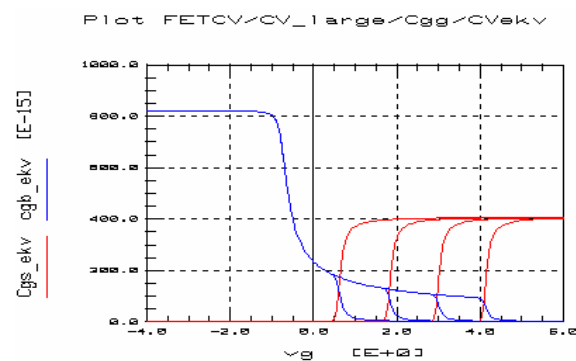
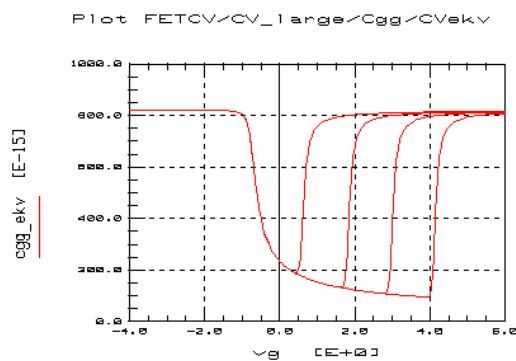
0.5um CMOS example



0.25um CMOS example

- Excellent match from weak through moderate to strong inversion regions.
- Measurement and simulation comparisons show that g_{ms}/I_D ratio is technology independent.

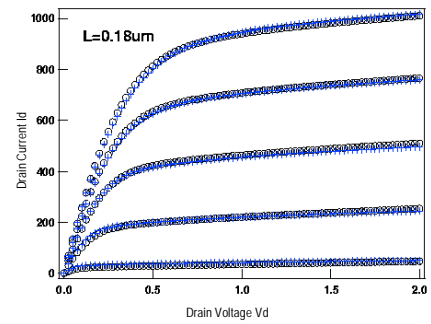
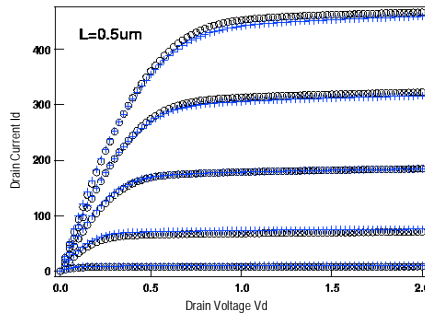
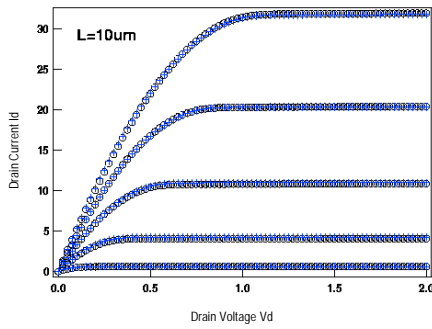
CV Modeling Example



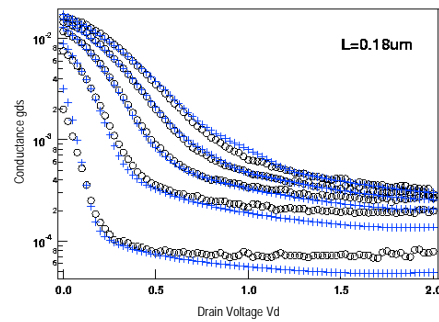
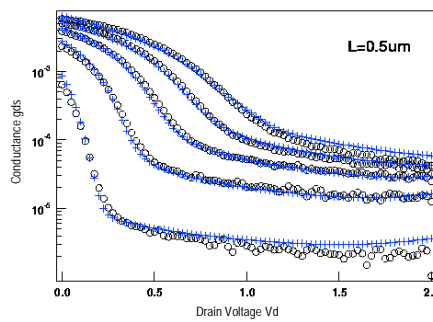
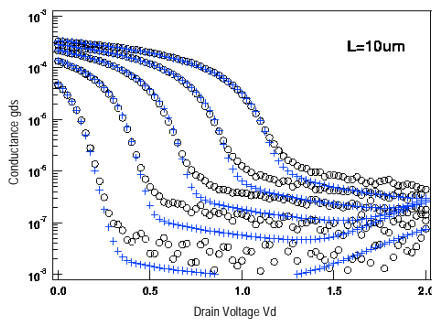
CV characteristics (C_{gg} , C_{gd} , C_{gs} , G_{gb}) of a large MOSFET as function the the gate to bulk bias ($V_D=V_S=0$)

- Consistent model for all charges and capacitances (G, D, S, B).
- Capacitances are valid in all operating regions, continuous, and symmetrical at $V_{DS}=0$

Extraction Example: 0.18um CMOS



Output current: I_d vs. V_d characteristics



Output conductance: g_{ds} vs. V_d characteristics

EKV3: Extended Deep Submicron Model

Advances in EKV3 compact modeling include:

- polydepletion effect
- quantum-mechanics QM effects
- extended charge-based mobility model
- enhanced velocity saturation/CLM model (charge-based)
- improved short-channel effects: DIBL, weak inversion slope
- extended reverse short channel effect (RSCE) model
- second order short/narrow channel effects
- gate current model
- gate induced drain leakage (GIDL)
- NQS effects
- short-channel thermal noise

Summary

- ❑ The EKV v2.6 model and related parameter extraction methodology have been developed at Electronics Lab of EPFL
- ❑ Design driven MOSFET modeling concept is dedicated to analog circuit simulation of the advanced CMOS circuits.
- ❑ The model is well suited for direct and optimization based extraction as well as for statistical modeling tasks
- ❑ On-line model documentation at: <http://legwww.epfl.ch/ekv>
- ❑ Complete DC and CV EKV v2.6 model code is available as generic c-code, and also in spice3 and Verilog-A formats
- ❑ The EKV3 developments are carried out by international modeling team: EPFL Switzerland, NTUA Greece, ENSPS France

Acknowledgements

C. Enz, F. Krummenacher, E. Vittoz
Authors of the initial EKV paper

M. Bucher, J-M. Sallese, C. Lallement, F. Theodoloz
EKV Development Team

F. Krummenacher, M. Bucher,
Smart Silicon Systems (S3)

C. McAndrew, L. Lemaitre, O. Pilloud, J. Victory
GMC, Motorola

M. Mierzwinski, F. Sischka
Agilent

All developers implementing the EKV model into
public domain and commercial simulation tools

Appendix

The EKV intrinsic model parameters can roughly be estimated from Spice level 2/3 parameters as indicated in the table below, if no parameter extraction facility is available. Attention has to be paid to units of the parameters. This estimation method can be helpful and generally gives reasonable results. Nevertheless be aware that the underlying modeling in Spice level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore it is preferred if parameter extraction is made directly from measurements.

NAME	UNITS	DEFAULT	EXAMPLE	'LOWER'	'UPPER'	ESTIMATION
COX	F/m ²	0.7E-3	3.45E-3	-	-	ϵ_{si} / TOX
XJ	m	0.1E-6	0.15E-6	0.01E-6	1E-6	XJ
DL	m	0	-0.15*L _{min}	-0.5*L _{min}	0.5*L _{min}	$XL - 2 LD$
DW	m	0	-0.1*W _{min}	-0.5*W _{min}	0.5*W _{min}	$XL - 2 WD$
VTO	V	0.5	0.7	0	2	VTO
GAMMA	V ^{1/2}	1.0	0.7	0	2	$(2q\epsilon_{si} NSUB)^{1/2} COX$
PHI	V	0.7	0.5	0.3	2	$2V_i \ln(NSUB/n_i)$
KP	A/V ²	50E-6	150E-6	10E-6	-	$U0 COX$
E0	V/m	1.0E12	200E6	0.1/(0.4 TOX)	-	$0.2/(THETA TOX)$
UCRIT	V/m	2.0E6	2.3E6	1.0E6	25E6	$VMAX/U0$
LAMBDA	-	0.5	0.8	0	3	-
LETA	-	0.1	0.3	0	2	-
WETA	-	0.25	0.2	0	2	-
Q0	As/m ²	0.0	230E-6	0	-	-
LK	m	0.29E-6	0.4E-6	0.05E-6	2E-6	-
IBA	1/m	0.0	2.0E8	0.0	5.0E8	$ALPHA VCR / L_C$
IBB	V/m	3.0E8	2.0E8	1.8E8	4.0E8	VCR/L_C
IBN	-	1.0	0.6	0.4	1.0	-

$$\epsilon_{ox} = 0.0345E-9 \text{ F/m}, q = 1.609E-19 \text{ C}, k = 1.381E-23 \text{ J/K} \quad L_c = \sqrt{\epsilon_{si} XJ / COX}$$

$$\epsilon_{si} = 0.104E-9 \text{ F/m} \quad n_i = 1.45E16 \text{ m}^{-3} \quad V_i = kT/q = 0.0259 \text{ V (at room temperature)}$$

NOTE: Parameters in this table suppose m (meter) has been chosen as length unit. L_{min} and W_{min} are the minimum drawn length and width of the transistors. Example values are indicated for enhancement N-channel devices.

References

- 1.C. Enz, F. Krummenacher, E. Vittoz, 'An analytical MOS transistor model valid in all regions of Operation and dedicated to low-voltage and low-current applications', Journal on Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers, pp. 83-114, July 1995
- 2.C. Lallement, F. Pêcheux, Y. Hervé, 'VHDL-AMS Design of a MOST Model Including Deep Submicron and Thermal-Electronic Effects', 2001 IEEE International Workshop on Behavioral Modeling and Simulation BMAS 2001 October 10-12, 2001 FountainGrove Inn Santa Rosa, California, USA
- 3.M. Bucher, J.-M. Sallese, C. Lallement, "Accounting for Quantum Effects and Polysilicon Depletion in an Analytical Design-Oriented MOSFET Model", Simulation of Semiconductor Processes and Devices 2001, pp. 296-299, Eds.D. Tsoukalas, C. Tsamis, Springer Vienna, NewYork, ISBN 3-211-83708-6
- 4.J.-M. Sallese, "Advancements in DC and RF MOSFET Modeling with the EPFL-EKV Charge Based Model", Special session: MOS Transistor: Compact Modeling and Standardization Aspects, 8th International Conference MIXDES 2001, Zakopane, Poland, June 21-23, 20001.
- 5.W. Grabinski "Compact Modeling of Low-power and RF Analogue MOSFET Devices", Special session: MOS Transistor: Compact Modeling and Standardization Aspects, 8th International Conference MIXDES 2001, Zakopane, Poland, June 21-23, 20001.
- 6.D. Binkley, M. Bucher, D. Foty, 'Design-Oriented Characterization of CMOS over the Continuum of Inversion Level and Channel Length', Proc. 7th IEEE Int. Conf. on Electronics, Circuits & Systems ICECS'2k, pp. 161-164, Kaslik, Lebanon, Dec. 17-20, 2000.
- 7.W. Grabinski, M. Bucher, J.-M. Sallese, F. Krummenacher, 'Compact Modeling of Ultra Deep Submicron CMOS Devices', ICSES'2000, October 17-20, 2000, Ustron, Poland.
- 8.W. Grabinski, M. Bucher, J.-M. Sallese, F. Krummenacher, 'Advanced Compact Modeling of the Deep Submicron Technologies', Diagnostic and Yield, D&Y'2000, June 28-30, 2000, Warsaw, Poland.
- 9.F. Krummenacher, W. Grabinski, M. Bucher, 'Advances in RF CMOS Modeling Based on the EPFL-EKV Model', Workshop on RF CMOS Transceivers, Pavia, June 20-21, 2000
- 10.J.-M. Sallese, A.-S. Porret, 'A novel approach to charge-based non-quasi-static model of the MOS transistor valid in all modes of operation', Solid State Electronics, Volume 44, No 6, pp. 887-894, June 2000.
- 11.J.-M. Sallese, M. Bucher, C. Lallement, 'Improved Analytical Modelling of Polysilicon Depletion for CMOS CircuitSimulation', Solid State Electronics, Volume 44, No 6, pp. 905-912, June 2000.
- 12.W. Grabinski, M. Bucher, F. Krummenacher, 'Harmonic Distortion Analysis Based on the EPFL-EKV Model', Silicon RF-IC: Modeling and Simulation Workshop 24-25 February 2000, EPFL, Lausanne, Switzerland
- 13.J.-M. Sallese, M. Bucher, C. Lallement, W. Grabinski, 'Advances in AC Modeling of MOSFET Using EKV Formalism', Silicon RF-IC: Modeling and Simulation Workshop 24-25 February 2000, EPFL, Lausanne.
- 14.M. Bucher, 'Analytical MOS Transistor Modelling for Analog Circuit Simulation', Ph.D. Thesis No. 2114 (1999), Swiss Federal Institute of Technology, Lausanne

References

- 15.M. Bucher, J.-M. Sallese, C. Lallement, W. Grabinski, C. C. Enz, F. Krummenacher, 'Extended Charges Modeling for Deep Submicron CMOS', Int. Semicond. Device Research Symp. (ISDRS'99), Charlottesville, Virginia, December 1-3, 1999.
- 16.F. Krummenacher, W. Grabinski, M. Bucher, 'RF MOSFET modeling approach based on the EPFL-EKV model', International workshop on low power RF integrated circuits, Lausanne, 19-20 October 1999
- 17.W. Grabinski, M. Bucher, F. Krummenacher, 'The EKV Compact MOSFET Model and its Low-Power Analog and RF Applications', Proc. XXIIInd Nat. Conf. on Circuit Theory and Electronic Networks, KKTOIUE'99, pp. 265-270, Stare Jablonki, Poland, October 20-23, 1999.
- 18.W. Grabinski, M. Bucher, F. Krummenacher, 'The EKV Model Parameter Extraction Based on its IC-CAP USERC Implementation', HP-IC-CAP Users Meeting, Marseille, France, June 17, 1999.
- 19.C. Enz, Y. Cheng, 'MOS Transistor Modeling Issues for RF Circuit Design', Workshop on Advances in Analogue Circuit Designs, Nice, March 1999.
- 20.M. Bucher, W. Grabinski, 'EKV MOS Transistor Modelling & RF Application', HP-RF MOS Modelling Workshop, Munich, February 15-16, 1999
- 21.L. Portmann, C. Lallement, F. Krummenacher, 'A High Density Integrated Test Matrix of MOS transistors for Matching Study', ICMTS 1998. 1998 IEEE International Conference on Microelectronic Test Structures, Proceedings IEEE, pp.19-24, 1998;
- 22.M. Bucher, C. Lallement, C. Enz, F. Théodoloz, F. Krummenacher, 'Scalable GM/I Based MOSFET Model' Proc. 1997 Int. Semiconductor Device Research Symposium (ISDRS'97), pp. 615-618, Charlottesville, VA, USA, December 10-13, 1997.
- 23.C. Lallement, M. Bucher, C. Enz, 'Modelling and characterization of non-uniform substrate doping', Solid-State-Electronics. vol. 41: (12), pp. 1857-1861 Dec. 1997,
- 24.C. Enz, E.A. Vittoz, 'MOS transistor modeling for low-voltage and low-power analog IC design' Microelectronic Engineering 39: (1-4) 59-76, Sp. Iss. SI Dec. 1997
- 25.M. Bucher, C. Lallement, C. Enz, F. Krummenacher, 'Accurate MOS modelling for analog circuit simulation using the EKV model' 1996 IEEE International Symposium on Circuits and Systems Circuits and Systems Connecting the World, ISCAS 96, pp. 703-6 vol.4, 1996.
- 26.C. Lallement, C. Enz, M. Bucher, 'Simple solutions for modelling the non-uniform substrate doping', 1996 IEEE International Symposium on Circuits and Systems. Circuits and Systems Connecting the World, ISCAS 96, pp. 436-9 vol.4, 1996;
- 27.M. Bucher, C. Lallement, C. Enz 'An efficient parameter extraction methodology for the EKV MOST model', ICMTS 1996. 1996 IEEE International Conference on Microelectronic Test Structures, Proceedings IEEE, pp.145-50, 1996;
- 28.G.A.S. Machado, C. Enz, M. Bucher, 'Estimating key parameters in the EKV MOST model for analogue design and simulation' , 1995 IEEE Symposium on Circuits and Systems IEEE, New York, NY, USA; 3 vol. 1+2346 pp. p.1588-91 vol.3. 1995;