NanoTera Workshop on Next-Generation MOSFET Compact Models

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Analog performance of advanced CMOS and EKV3 model

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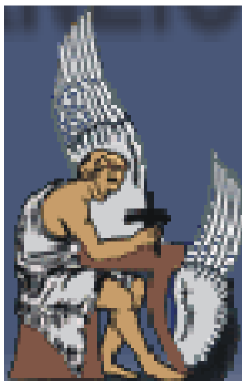
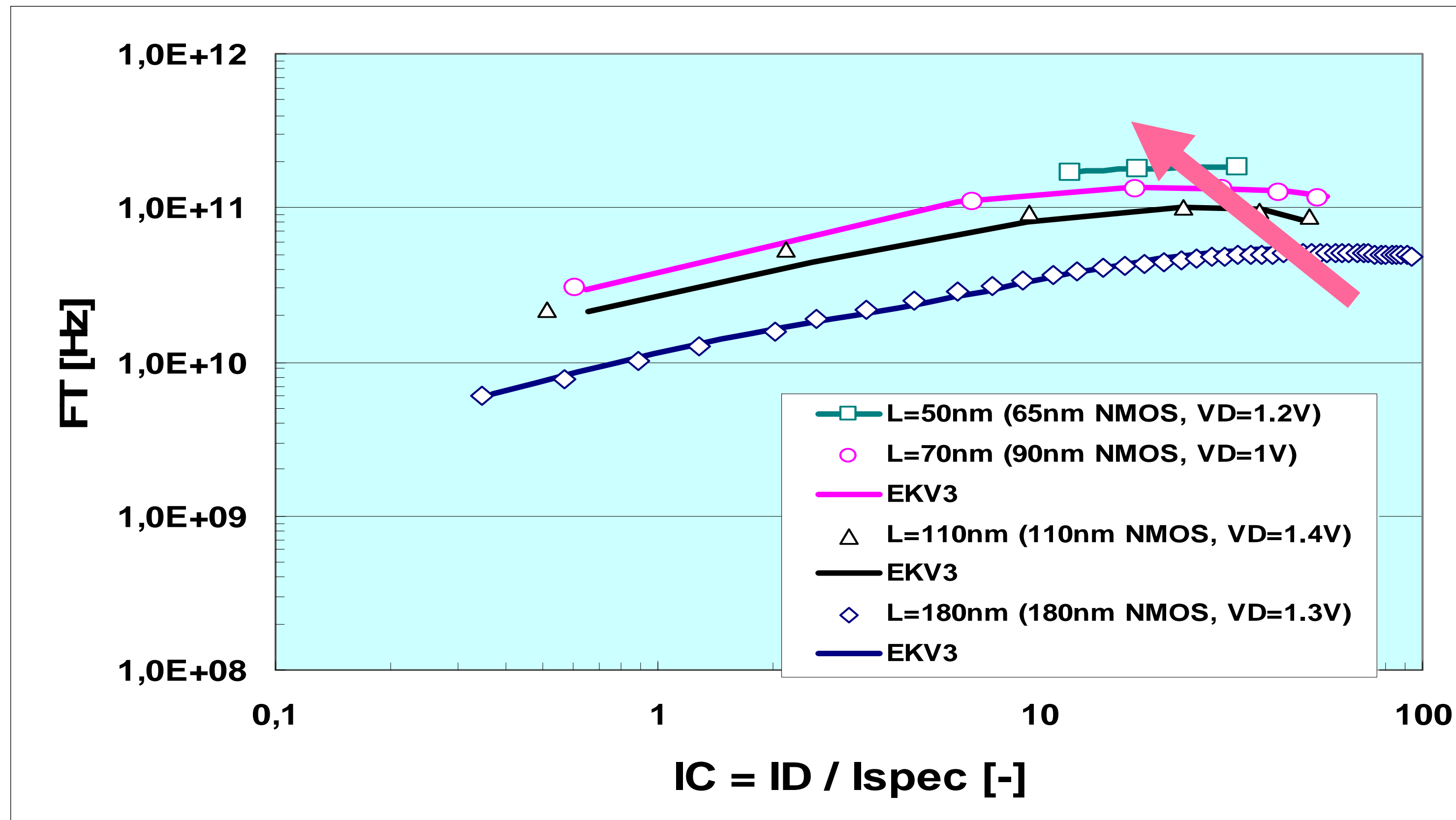


Outline

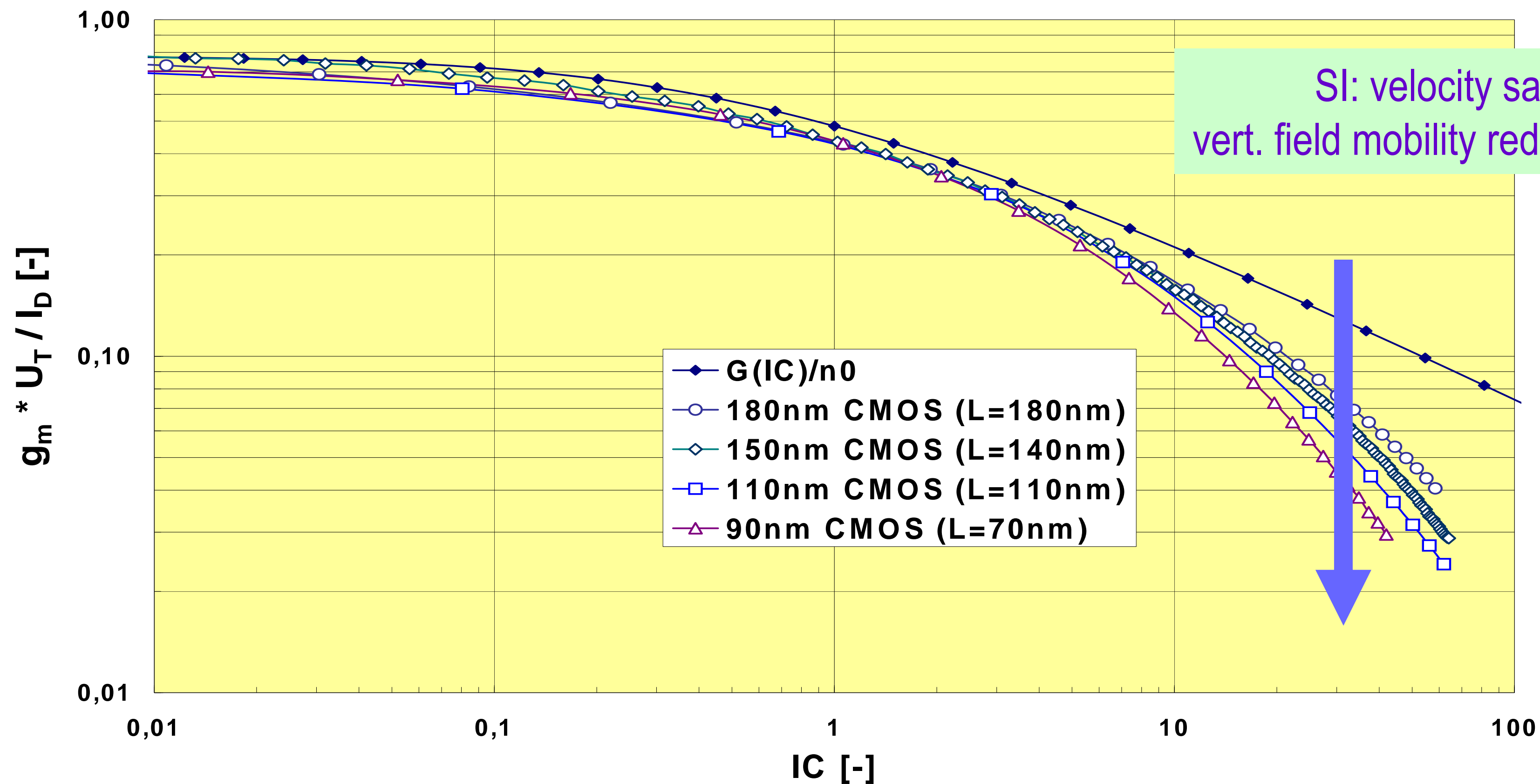
- Motivation – the need for moderate inversion design
- Evolution of CMOS device performance – from planar bulk to double-gate and FinFET
- EKV3 charge-based compact model
- EKV3 high-frequency model
- Conclusions

Scaling of F_T for 180nm –> 65nm CMOS



- NMOS transistors, high V_D bias (variable)
- F_T reaches 187, 134, 101, 52 GHz, respectively
- A plateau (max. F_T) is reached
  - ✓ slightly above Moderate Inversion (MI, 0.1 < IC < 10)
  - ✓ IC ~= 20 … 50, depends on V_D

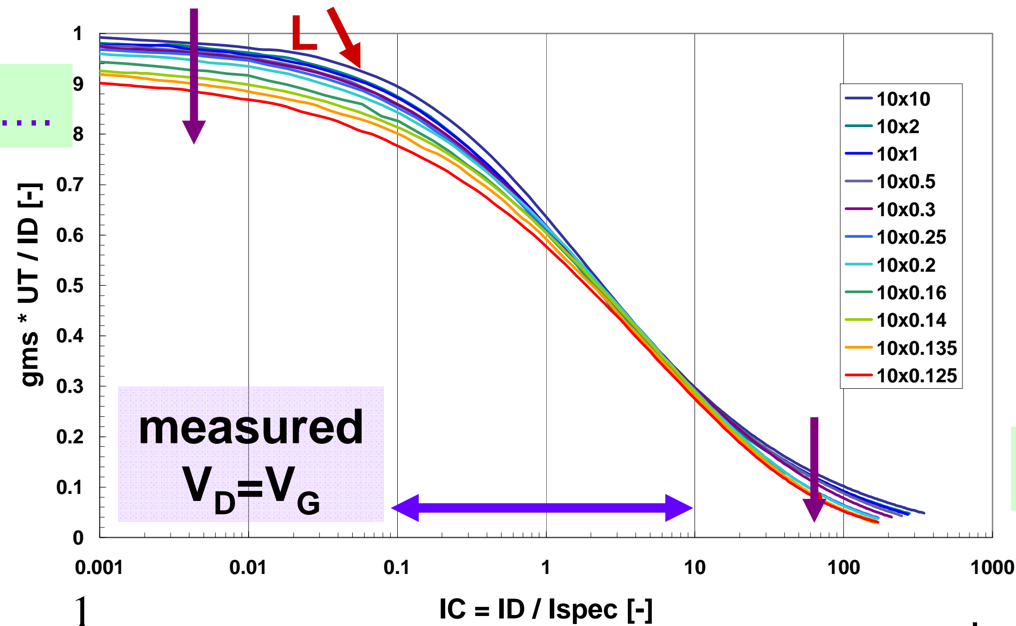
Scaling of normalized transconductance



- Weak Inversion (WI, IC<0.1): highest transconductance per given current
- Strong Inversion (SI, IC>10): stronger degradation due to higher fields in more advanced technology

Normalized transconductance

WI: (DIBL, CS) STI….



SI: VS, CLM….

$$\frac{g_{ms} \cdot U_T}{I_D} = G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

Moderate Inversion

L = 10 um → 125nm

Inversion Coefficient:

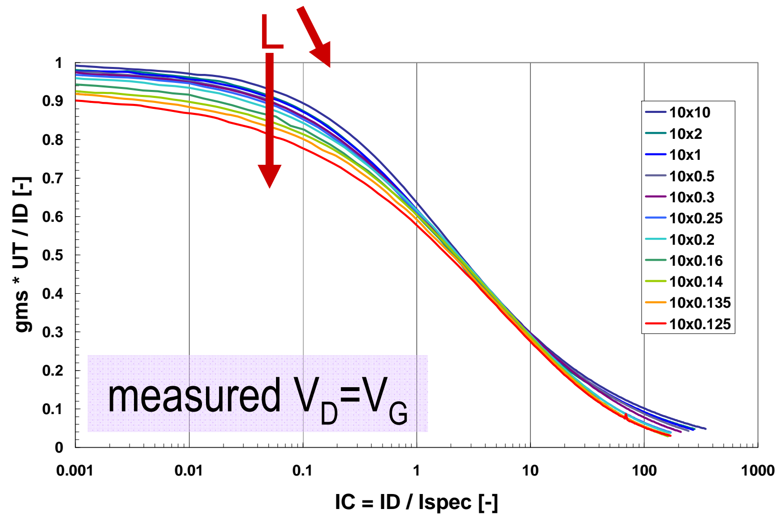
$$IC = \frac{I_D}{I_{SPEC}}$$

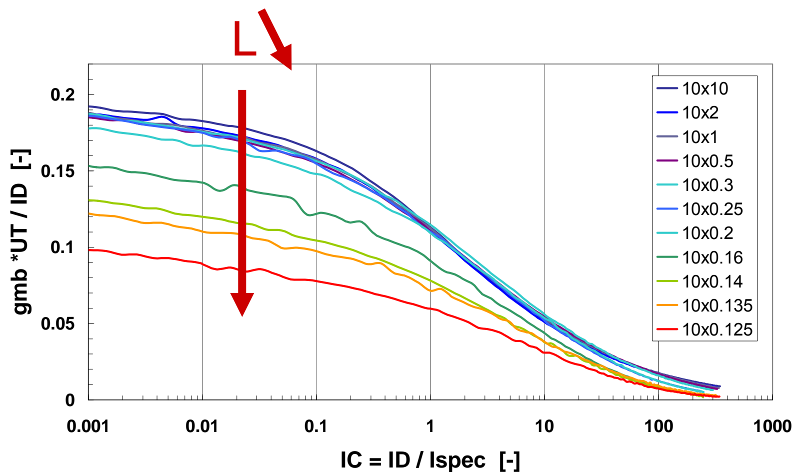
Specific Current:

$$I_{Spec} = 2nU_T^2 \mu C'_{ox} \frac{W}{L}$$

- Normalization factor for drain current: $\mathbf{I}_{spec}$
- Normalized g_m and g_{ds} vs. IC and L
- Anomalous scaling of output conductance in WI

g_{ms}/I_D, g_{mb}/I_D vs. IC, L





Moderate Inversion

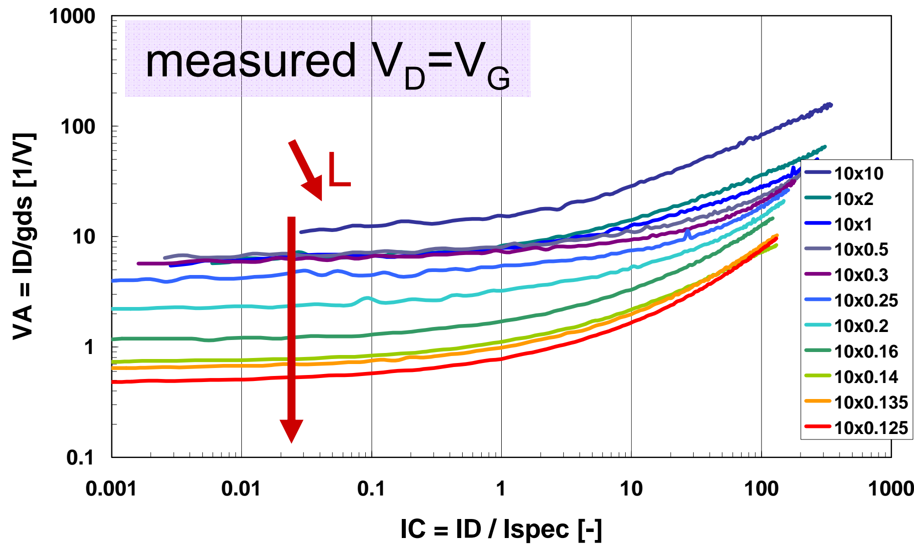
$$\frac{g_{ms} \cdot U_T}{I_D} = G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}}$$

$$\frac{g_m \cdot U_T}{I_D} = \frac{1}{n} \cdot G(IC)$$

$$\frac{g_{mb} \cdot U_T}{I_D} = \frac{n-1}{n} \cdot G(IC)$$

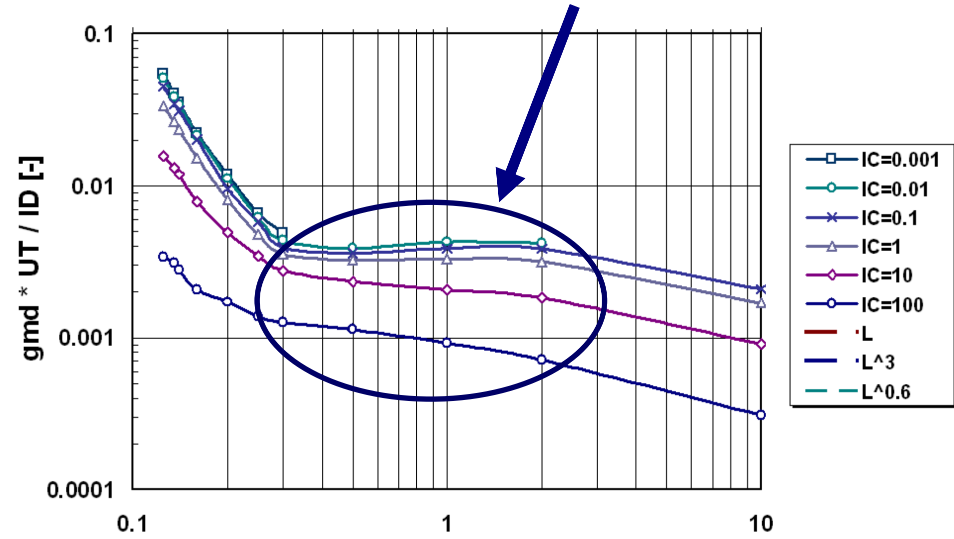
- EKV model offers convenient estimation of large- and small-signal quantities for ideal charge-based MOSFET – not available from other modelling approaches

Early voltage vs. IC, L



Moderate Inversion

Anomalous VA scaling

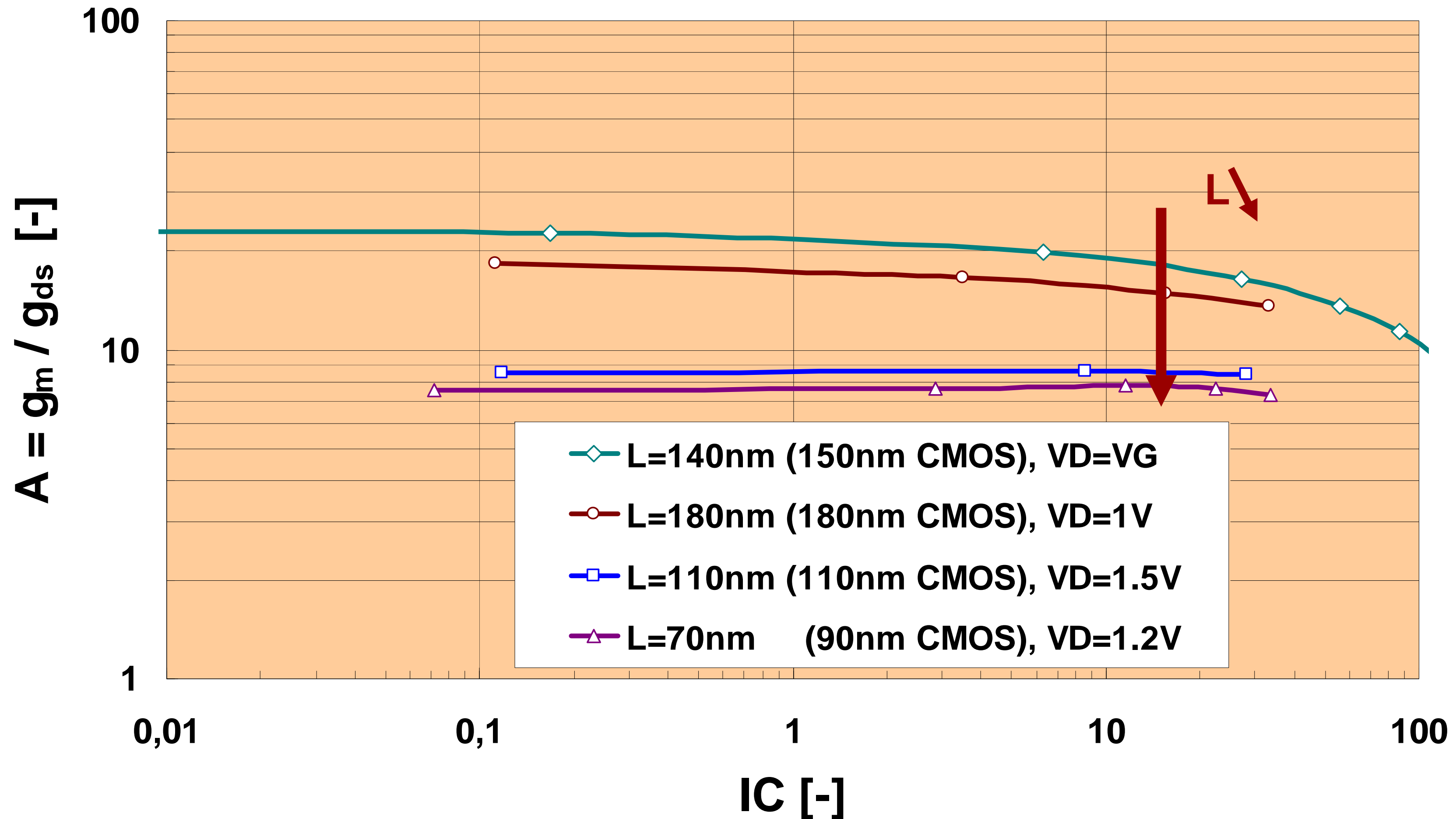


$$\frac{U_T}{V_A} = \frac{g_{ds} \cdot U_T}{I_D} \cong -\frac{\partial V_{TO}}{\partial V_D} \cdot \frac{1}{n} \cdot G(IC)$$

DIBL effect dominates gds in WI-MI

- Early Voltage V_A scaling is dominated by DIBL effect ($\delta V_{TO}/\delta V_D$)
  - ✓ V_A scaling related to transconductance function G(IC)
- In strong inversion, velocity saturation & CLM dominate
- Anomalous scaling of output conductance in WI

Scaling of DC gain – planar bulk CMOS



- DC gain is strongly degraded (@minimum length!) for scaled CMOS → problem for analog/RF design!

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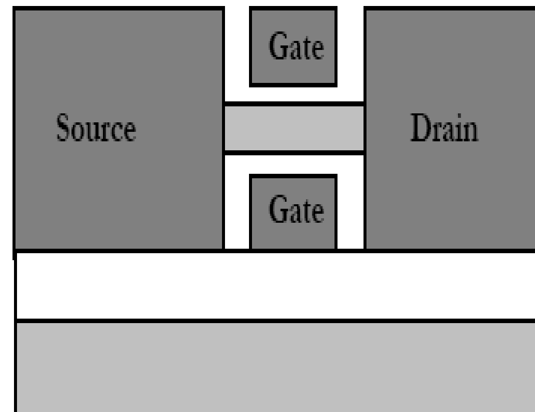
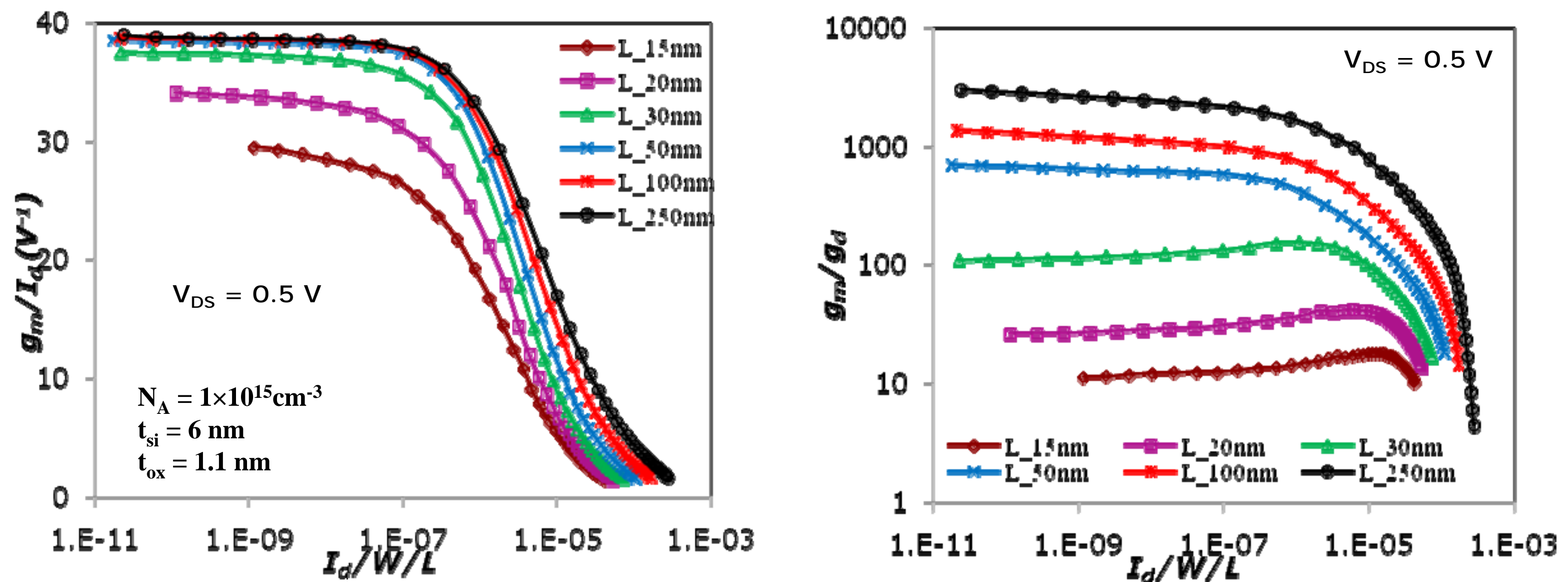
Double gate MOSFETs



- DG MOSFET is (one of !?!) the most promising device, because it has less geometry effects such as corner and narrow width effects
- The two gates are easy to be biased separately as they are formed in different process steps
  - symmetric or asymmetric operation possible
- Effective control of short channel effects
- Higher current drive capability and transconductance
- Ideal weak inversion slope

Double gate FET – transconductance and gain scaling

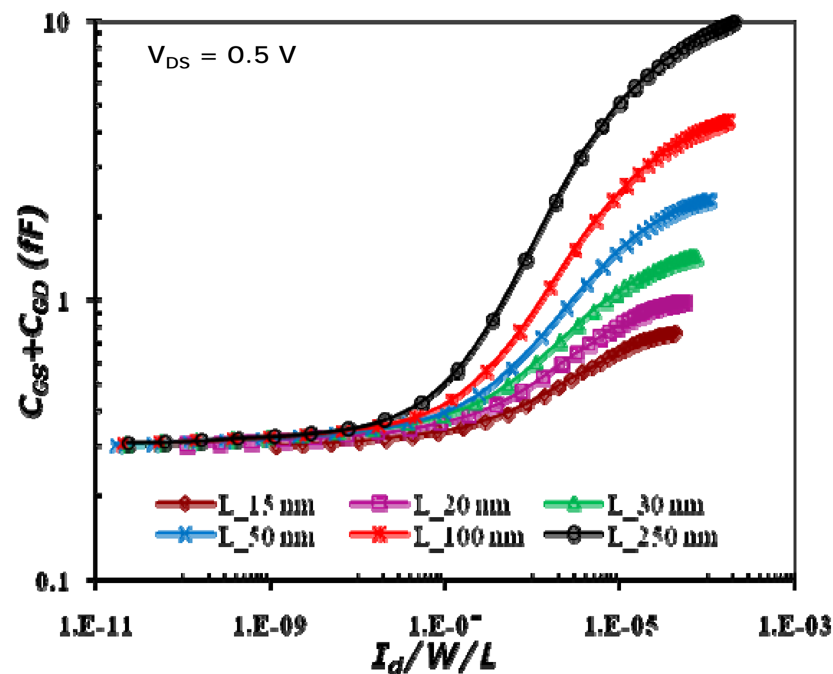
Transconductance efficiency (g_m/I_D) and intrinsic gain (g_m/g_{ds})

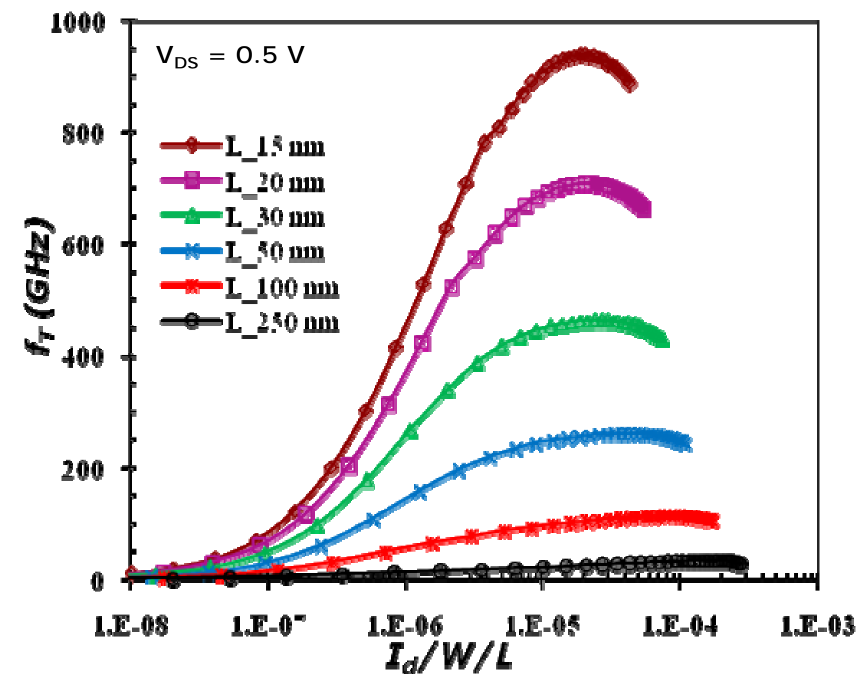


- For gate lengths below 50 nm, important decrease in device efficiency and voltage gain → drain/gate engineered DG MOSFETs required
- TCAD simulation

Double gate FET – capacitance and F_T scaling

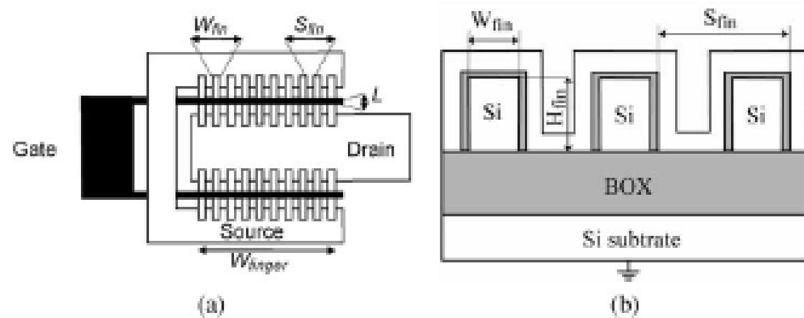
Capacitance $C_{GS}+C_{GD}$ and cut-off frequency F_T

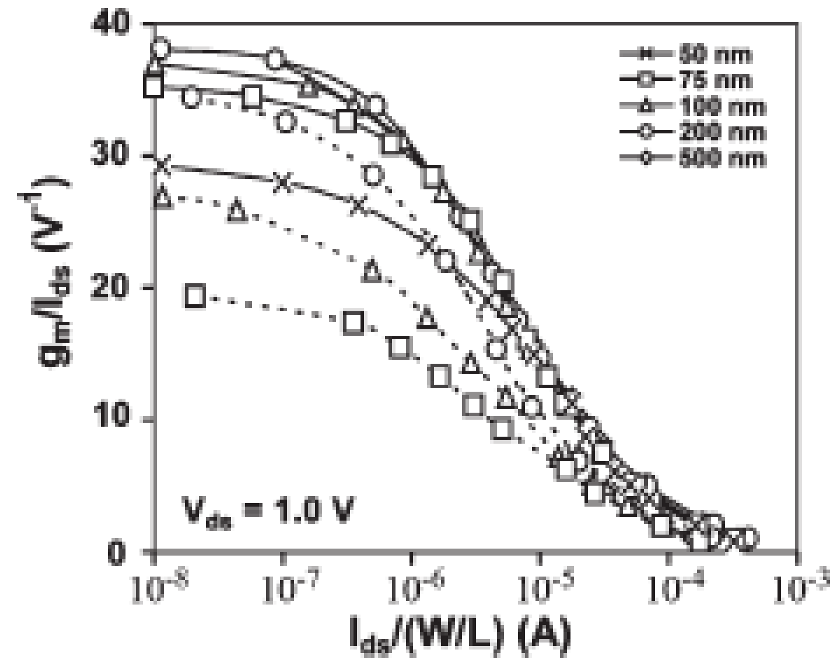


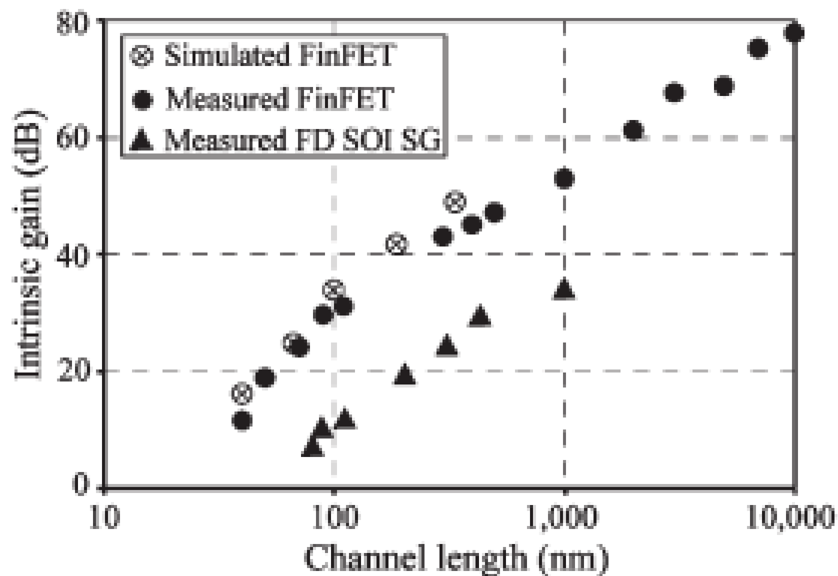


- Extremely high speed of intrinsic devices
- Parasitics need to be considered

FinFET transconductance & gain



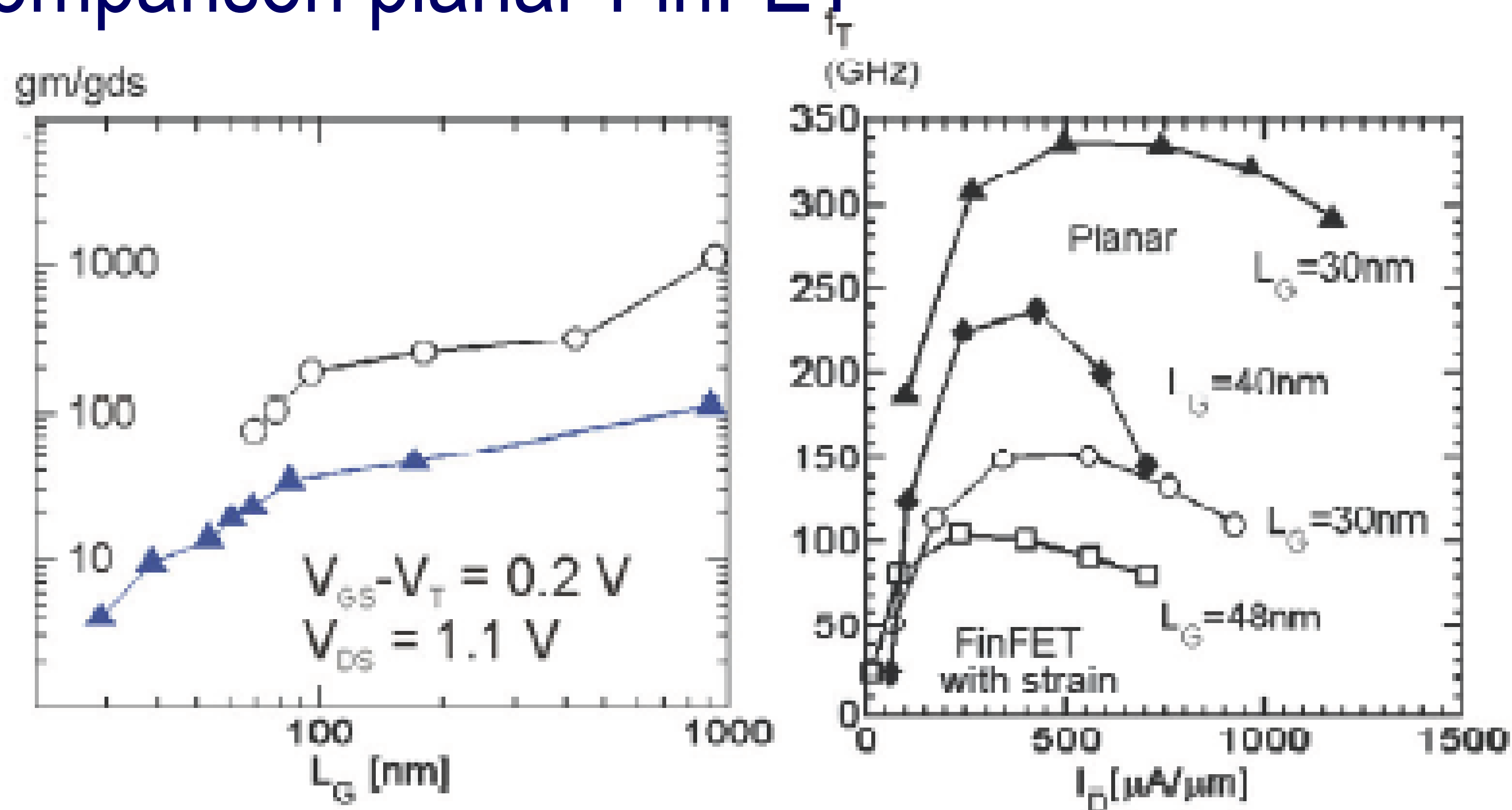




Raskin e.a., TED(53), 2006

- FinFET: short-channel effects on gm/ID

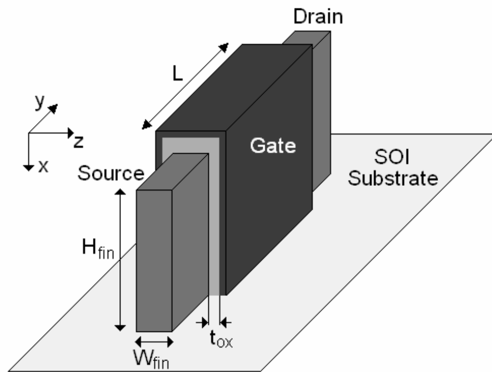
Comparison planar-FinFET

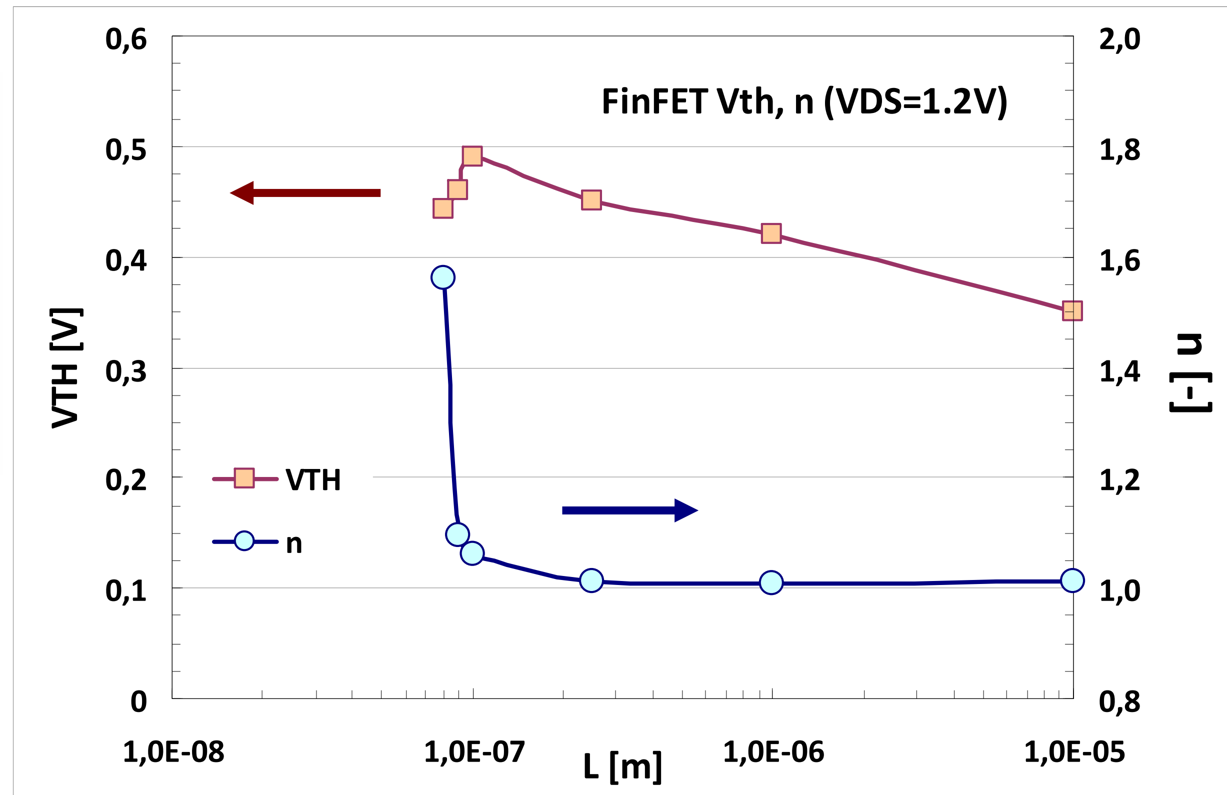


Wambacq e.a., ISSCC 2008

- Better gm/gds in FinFETs compared to planar
- Higher speed in planar bulk CMOS (strained silicon)
- Higher parasitic capacitances – series resistance in FinFETs

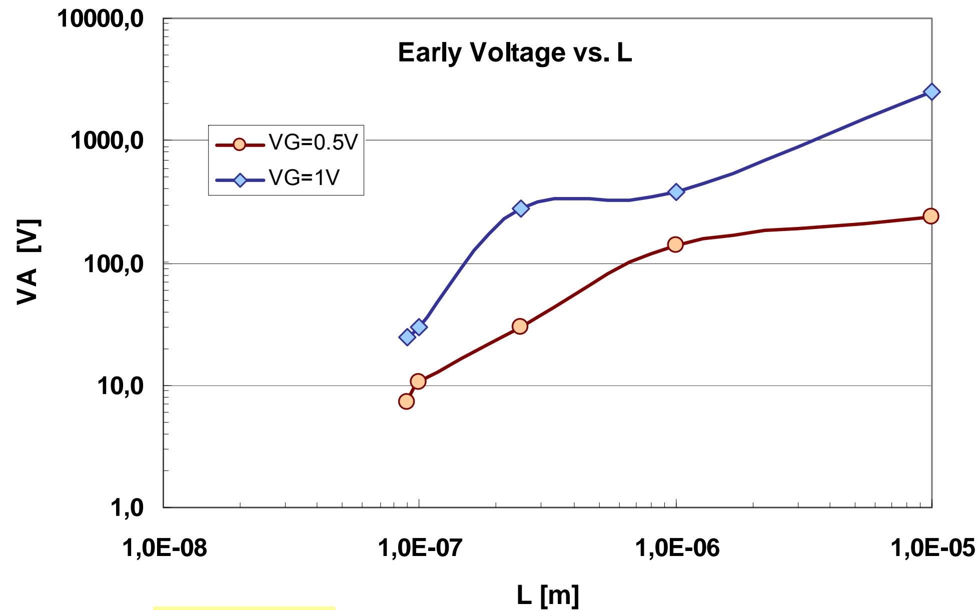
FinFET V_T & n scaling



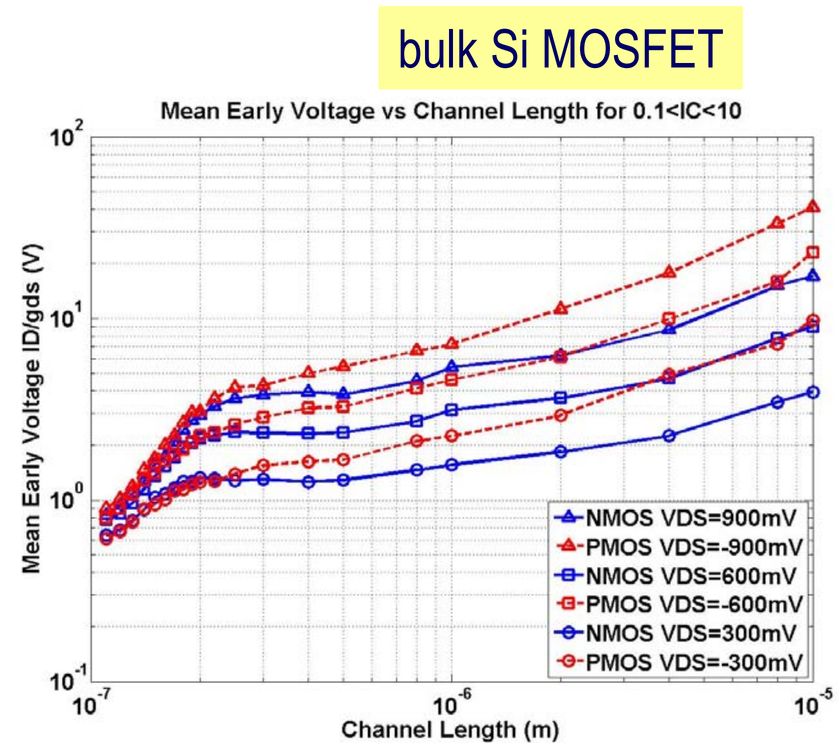


- 80nm, n-FinFETs, measured characteristics.
- Scaling versus channel length – RSCE appears
- Show severe subthreshold slope degradation @ L=80nm

FinFET Early voltage scaling

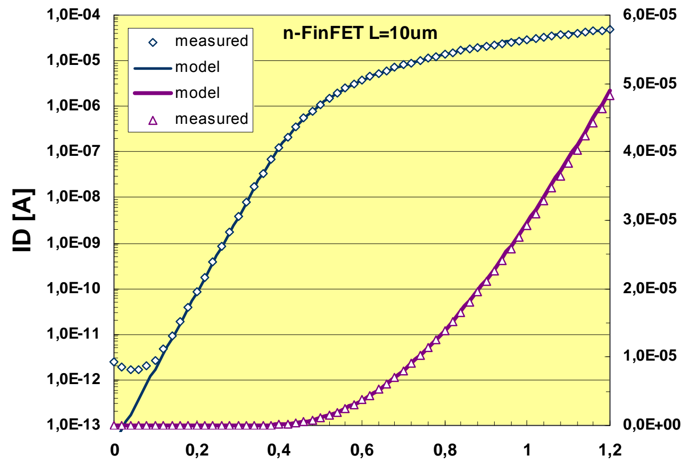


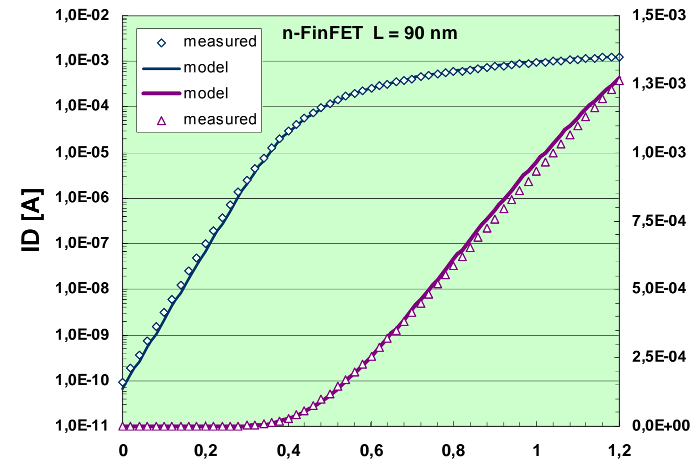
FinFET

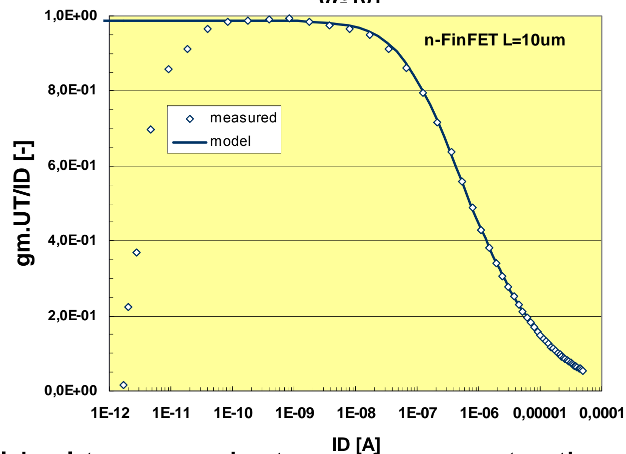


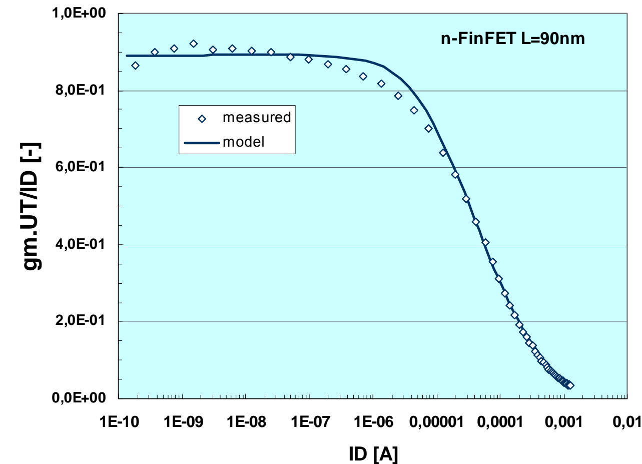
- 80nm n-FinFETs
- V_A scaling versus channel length
- FinFET Early voltage is very high $V_{A,FinFET}$ >= 10$V_{A,planar\ bulk}$ @same L
- entails high intrinsic gain vs. planar

FinFET IV modelling with EKV3



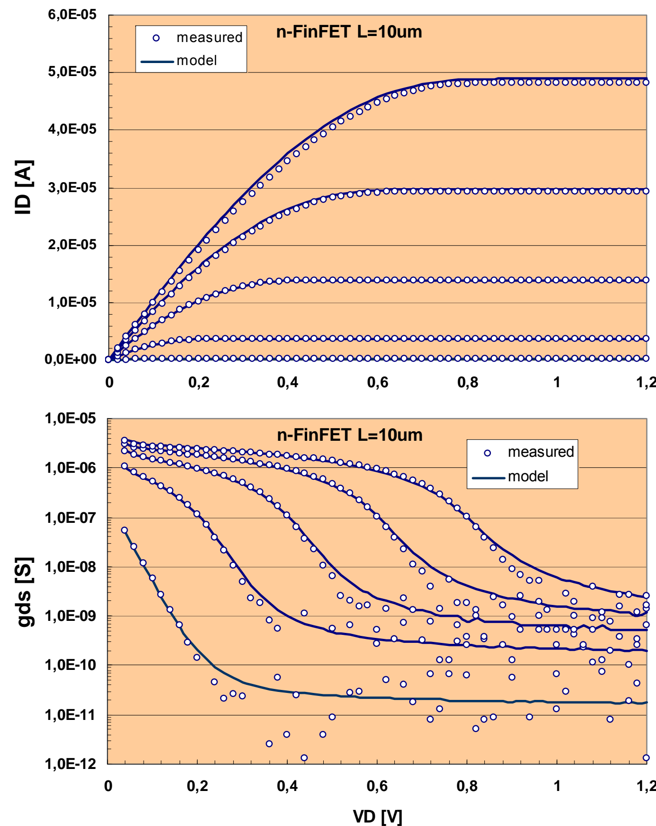


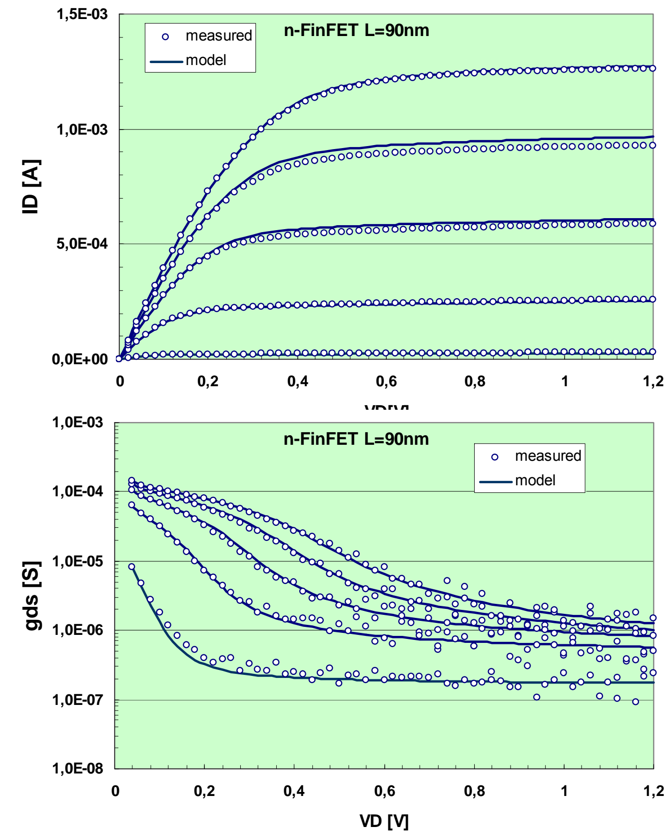




- Ideal transconductance to current ratio
- “planar-like” (very low substrate doping)
- Short channel weak inversion slope remains good (L=90nm)
- similar observations as in planar bulk Si MOSFETs – moderate inversion degradation of gm/ID

FinFET IV modelling with EKV3





- Short-channel output characteristics
- Velocity saturation effects, CLM, DIBL, … needed
  - ✓ many similarities with bulk Si MOSFETs

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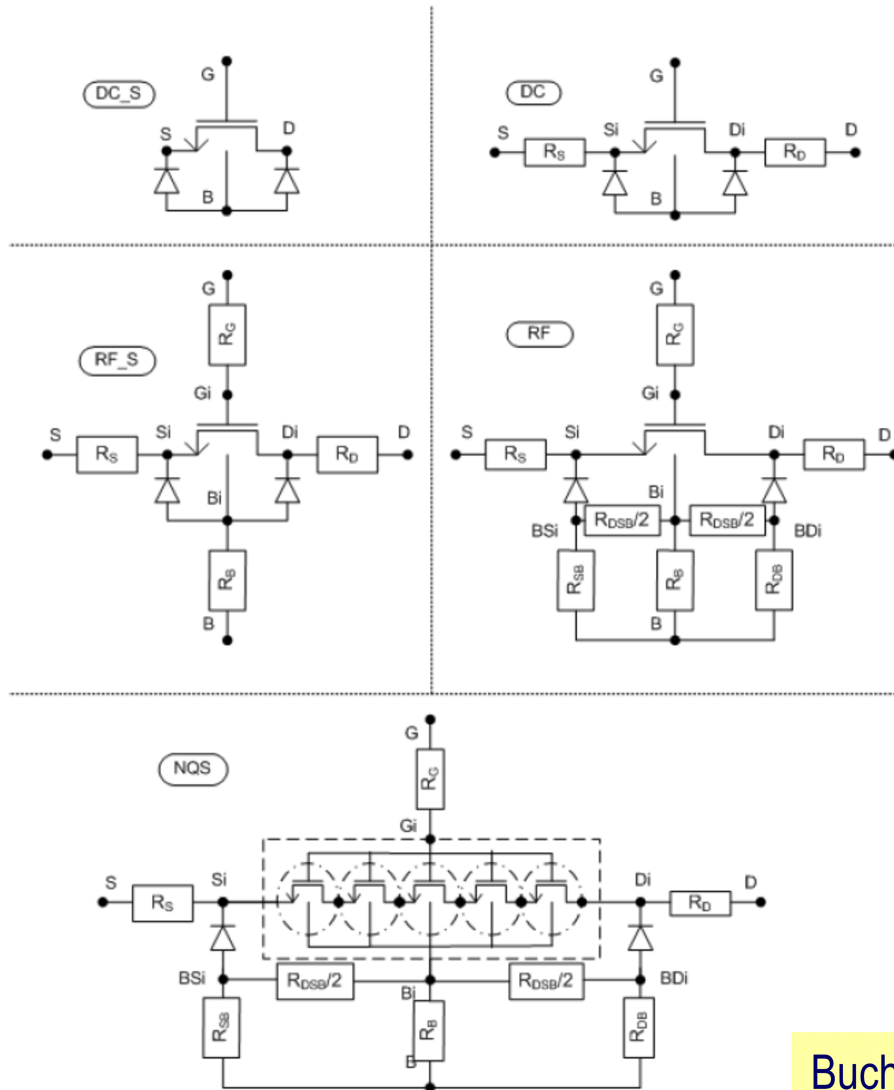
EKV3 model overview

- Due to CMOS scaling, ICs operate more and more in moderate and weak inversion
- Design methods and models are required
  – 'classical' methods don't cover moderate inversion
- EKV3 is a Compact MOS Transistor Model dedicated to Analog/RF IC design
  - ✓ Developed as a successor of EKV2.6
  - ✓ Full charge-based modelling approach – close to physics and design
  - ✓ Special attention to analog/RF IC design requirements
  - ✓ Covers essential effects down to 45nm CMOS
  - ✓ Scaling over Technology – Width – Length – T – Bias
  - ✓ EKV3 available for implementation to CAD vendors.

Configurations of EKV3

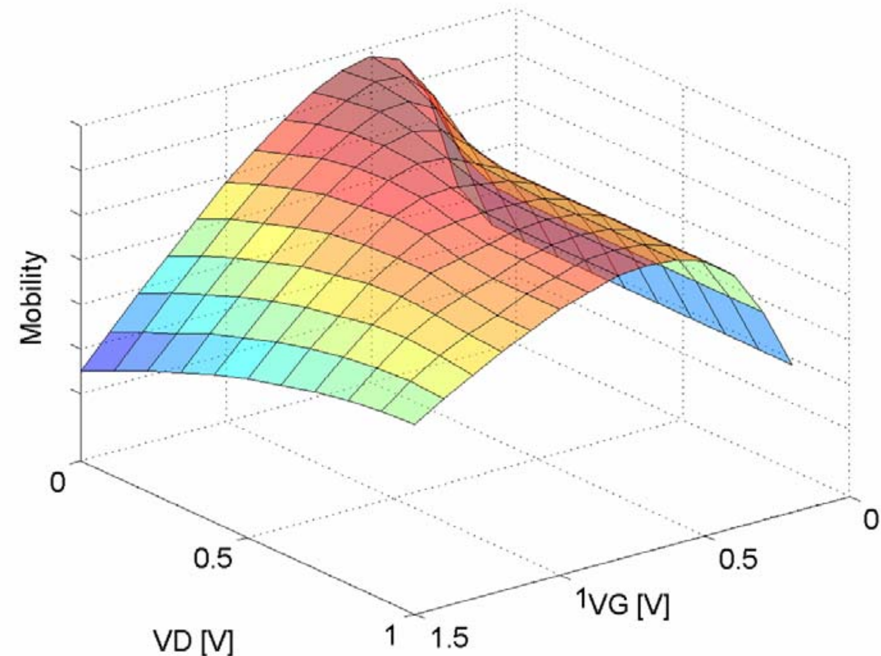


- Simple model – only internal accounting for (S,D) series resistance
- Simple model with external series resistance
- Simple RF model with gate and substrate resistance
- Full RF model with substrate resistivity network
- Full RF & NQS (channel segmentation) model.

Bucher e.a., SSE(52), 2008

EKV3 – charge based model & extensions

- Basis of charge model development is surface potential equation & inversion charge linearization
  - ✓ Same parameters as surface potential model
  - ✓ Preserves the essence of a surface potential model.
- Extensions for CV:
  - ✓ Vertical non-uniform doping
  - ✓ Polydepletion
  - ✓ Quantum effects
- Extensions of IV:
  - ✓ Charge-based vertical field mobility
  - ✓ Charge-based velocity saturation
  - ✓ Charge-based CLM
  - ✓ Gate tunnelling



EKV3 model scaling effects

- RSCE, INWE, combined short&narrow-channel effects
- DIBL, charge-sharing
- Halo/pocket implant effects
  - ✓ including @long channel
- Bias-dependent overlap & inner fringing capacitances
- Bias-dependent series resistance
- Geometry & temperature scaling
- Parasitic effects modelling
  - ✓ Layout dependent stress
  - ✓ Edge conduction
  - ✓ Gate tunneling
  - ✓ ….

EKV3 model basic parameters

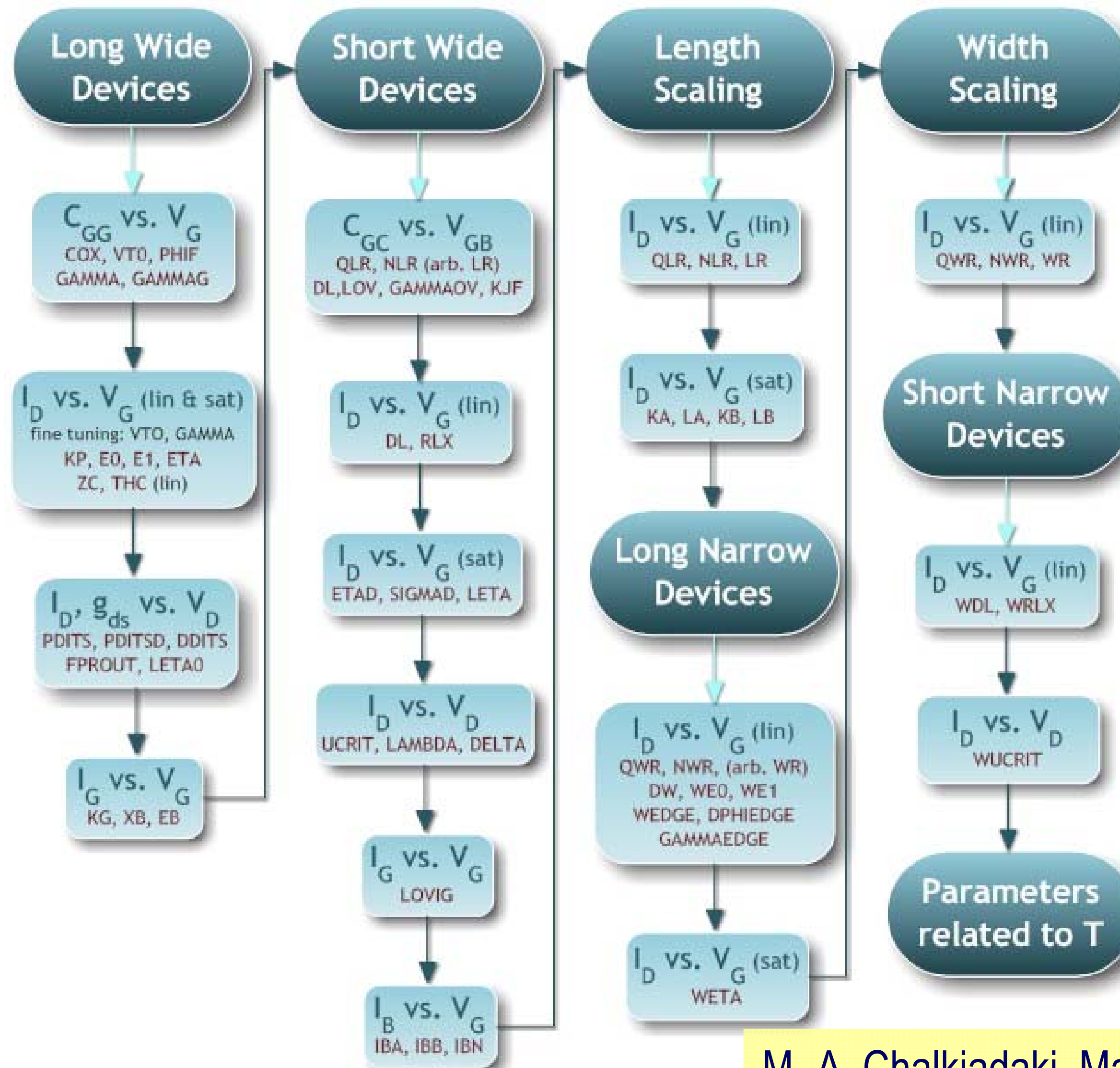
Parameter	Nmos	Pmos
Flags & Setup Parameters		
SIGN	1.0	-1.0
TNOM	27.0	27.0
TG	-1.0	-1.0
QOFF	0.0	0.0
XL	0.0	0.0
XW	0.0	0.0
SCALE	1.0	1.0
Oxide, Substrate & Gate Doping		
VTO	91m	-132m
COX	13.5m	13.1m
XJ	22n	11.4n
PHIF	458m	434m
GAMMA	149m	23.9m
GAMMAG	14.7	5.9
N0	1.018	1.023
Quantum Effects		
AQMA	18	570m
AQMI	480m	372m
ETAQM	738m	742m
Vertical Field Mobility		
KP	1.050m	290.0u
E0	130MEG	92MEG
E1	9.7G	8.1G
ETA	1.0	1.21
ZC	0.9u	0.95u
THC	0.0	0.0
Velocity Saturation & CLM		
UCRIT	3.9MEG	16.9MEG
LAMBDA	430m	1.454
DELTA	2.01	1.02
ACLM	838m	827m
Charge Sharing Effect		
NCS	1.6	21
LETA0	1.2MEG	2.78MEG
LETA	1.054	1.54
LETA2	-24n	0.0
WETA	0.0	0.0
Reverse Short Channel Effect		
LR	67.8n	38.9n
QLR	3.4m	8.2m
NLR	78m	7.6
FLR	1.1	0.0

Parameter	Nmos	Pmos
Inverse Narrow Width Effect		
WR	103n	43n
QWR	5.5u	306u
NWR	5.1m	-32m
Drain Induced Barrier Lowering		
ETAD	1.19	1.65
SIGMAD	306m	1.1
Geometrical Parameters		
DL	25.23n	82n
DW	-9n	0.0
DLC	0.0	0.0
DWC	13.9n	117n
LL	0.0	0.0
LLN	1.1	1.1
WDL	6f	0.0
LDW	2.8f	0.0
Drain Induced Threshold Shift		
FPROUT	2.9MEG	9.75MEG
PDITS	57u	14u
PDITSL	0.0	0.0
PDITSD	190m	780m
DDITS	9.0	9.0
Mobility Scaling Parameters		
KA	380m	0.0
LA	270n	2.7u
KB	465m	0.0
LB	19n	165n
WKP1	249n	307n
WKP2	605m	-272m
WKP3	509m	1.51
WKP3	509m	1.51
Long & Wide VTO & GAMMA		
LVT	1.089	1.076
WVT	104u	104u
AVT	36m	158m
LGAM	1.098	1.45u
WGAM	110u	1.3
AGAM	25.8m	-211m
Matching Parameters		
AVTO	0.0	0.0
AGAMMA	0.0	0.0
AKP	0.0	0.0

Parameter	Nmos	Pmos
Gate Current		
KG	13.9u	24.4u
XB	5.0	4.98
EB	42.0G	29.42G
LOVIG	24n	29.06n
Impact Ionization Current		
IBA	0.0	0.0
IBB	987MEG	445MEG
IBN	110m	109m
Edge Device		
DGAMMAEDGE	0.0	0.0
DPHIEDGE	0.0	0.0
WEDGE	0.0	0.0
Overlap Capacitances		
LOV	23n	26n
GAMMAOV	4.1	3.4
VFBOV	0.0	0.0
VOV	1.0	1.0
Fringing Capacitance		
KJF	0.0	0.0
CJF	0.0	0.0
Temperature Parameters		
TCV	310u	-530u
BEX	-1.3	-1.2
TETA	0.0	0.0
UCEX	1.4	3.7
TLAMBDA	223m	1.32
TE0EX	0.0	490m
TE1EX	0.0	1.1
IBBT	950u	730u
Temperature & Geometry Scaling		
TCVL	0.0	-37p
TCVW	82p	31p
TCVWL	0.0	0.0
Resistance Temperature Scaling		
TR	0.0	-4.6m
TR2	0.0	0.0
Flicker Noise Parameters		
AF	1.0	1.0
KF	0.0	0.0
EF	2.0	2.0
KGNF	0.0	0.0

Parameter	Nmos	Pmos
STI Stress Effect		
SAREF	1.423u	1.423u
SBREF	1.423u	1.423u
KVTO	0.0	6.0n
KKP	-38n	32n
KGAMMA	0.0	0.0
KETAD	33n	0.0
KUCRIT	-8.8	0.0
Width Scaling Parameters		
WE0	45n	157n
WE1	0.0	0.0
WRLX	45n	0.0
WUCRIT	-44n	138n
WLAMBDA	0.0	24n
WETAD	0.0	-48n
WUCEX	0.0	0.0
WLR	0.0	0.0
WQLR	0.0	-22n
WNLR	139n	-176n
WDPHIEDGE	0.0	0.0
Length Scaling Parameters		
LWR	0.0	0.0
LQWR	1.4u	0.0
LNWR	0.0	-55n
LDPHIEDGE	0.0	0.0
Combined Scaling Parameters		
WLDPHIEDGE	0.0	0.0
WLDGAMMAEDGE	0.0	0.0
Source-Drain Series Resistance		
RLX	73u	51u
RSH	0.0	0.0
LDIF	0.0	0.0
HDIF	234n	234n
Gate Resistance		
GC	1.3	1.3
RGSH	52	51
Substrate Resistance		
RDSBSH	1.467K	10.9K
RBWSH	1.2K	1.2K
RSBWSH	35	56
RDBWSH	35	56

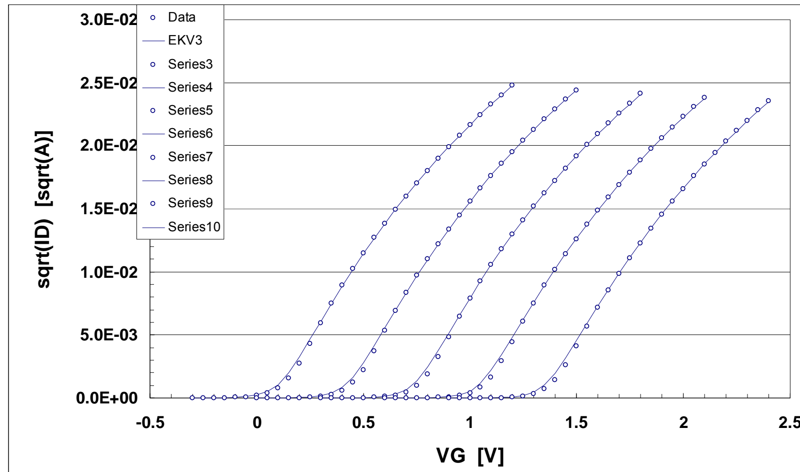
EKV3 model IV-CV-T parameter extraction

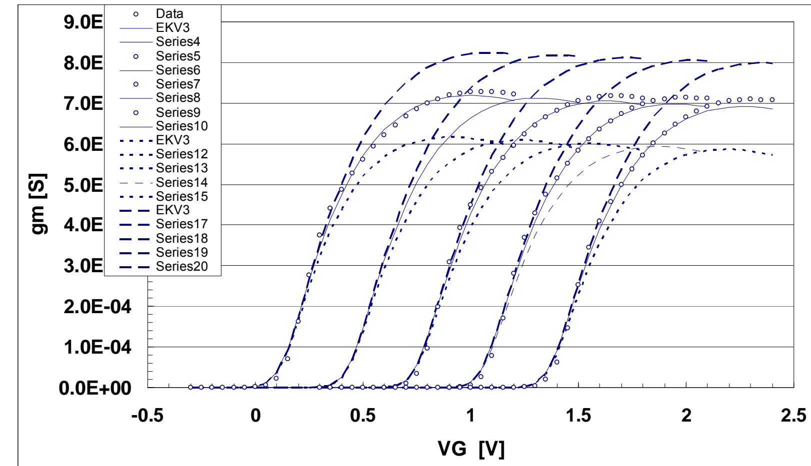


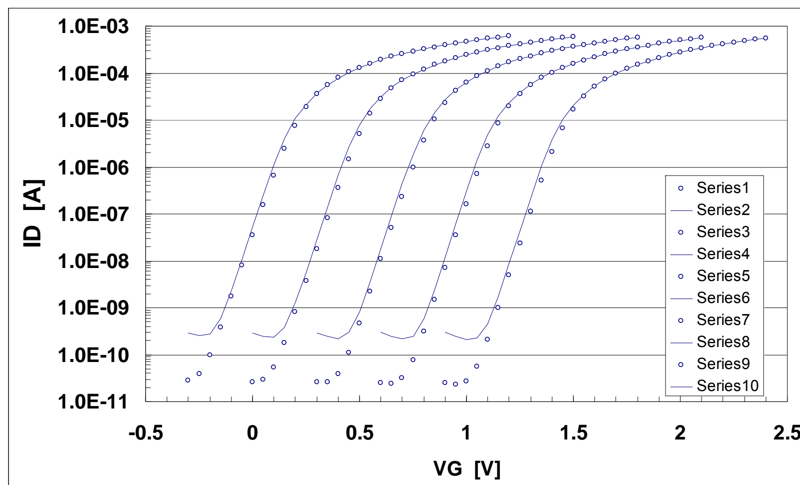
M.-A. Chalkiadaki, Master Thesis, TUC 2011

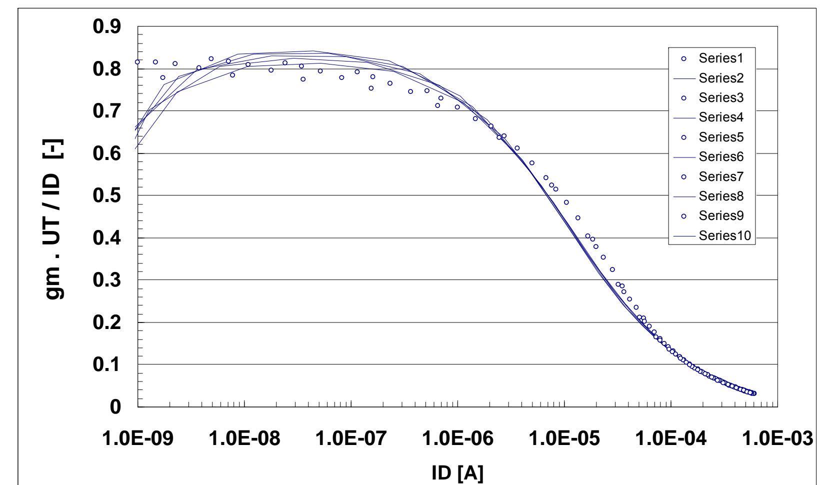
EKV3 – long channel

W = 2um, L = 0.5um



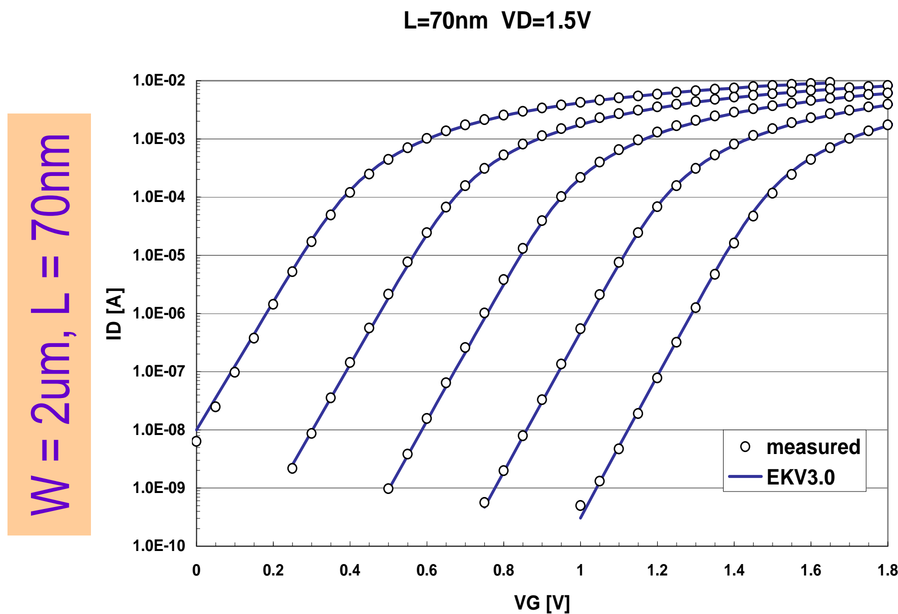


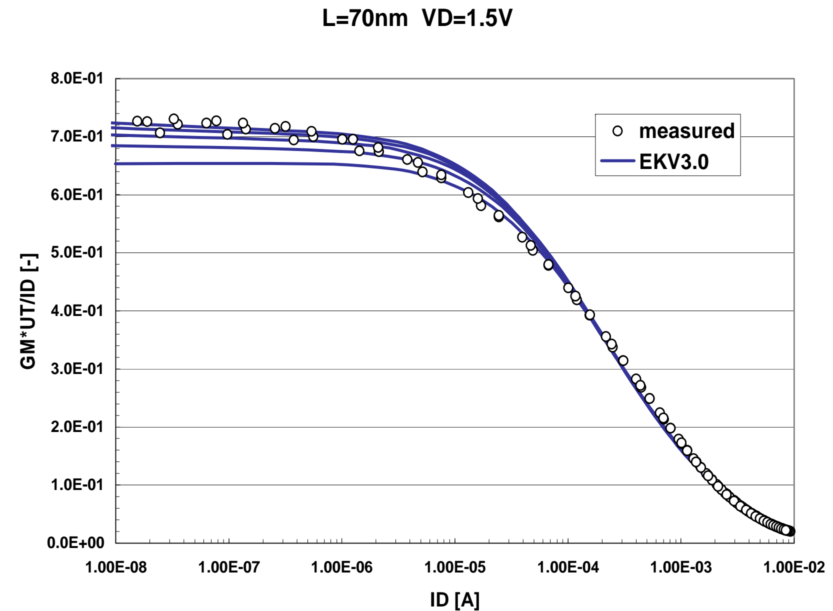




EKV3 – short-channel

W = 2um, L = 70nm

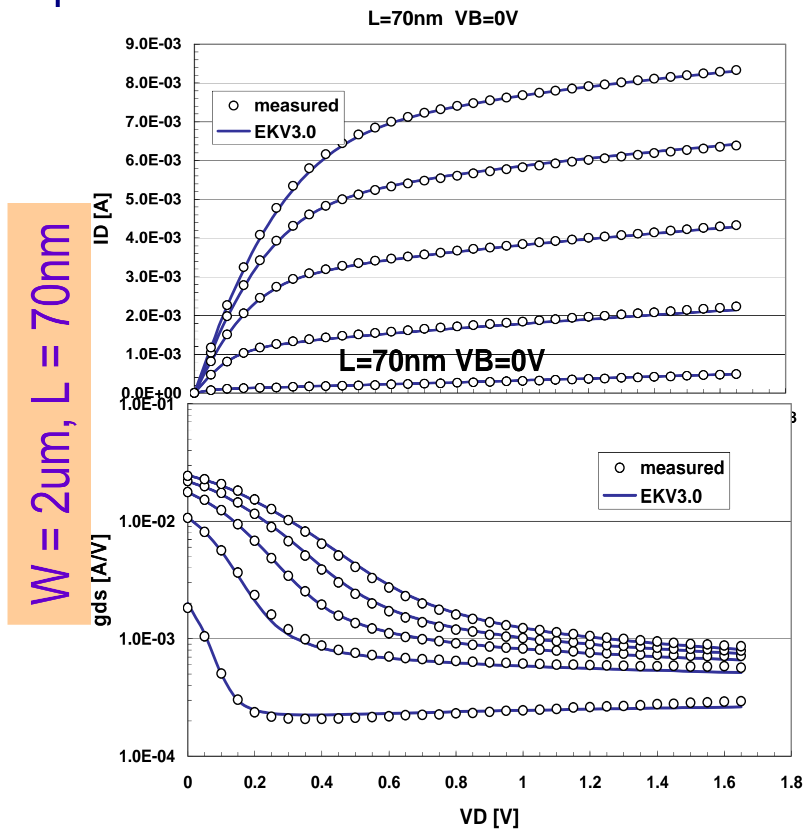


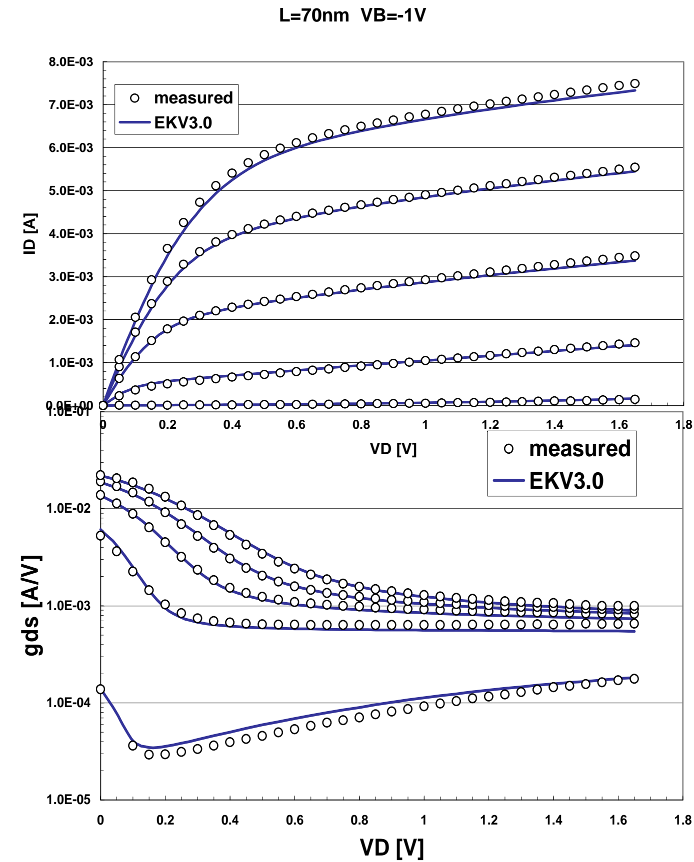


- Correct weak & moderate inversion behavior
  - ✓ Smoothness and correct asymptotic behavior
  - ✓ Correct weak inversion slope and DIBL modelling
- Transconductance-to-current ratio vs. drain current (log. axis)

EKV3 – short-channel

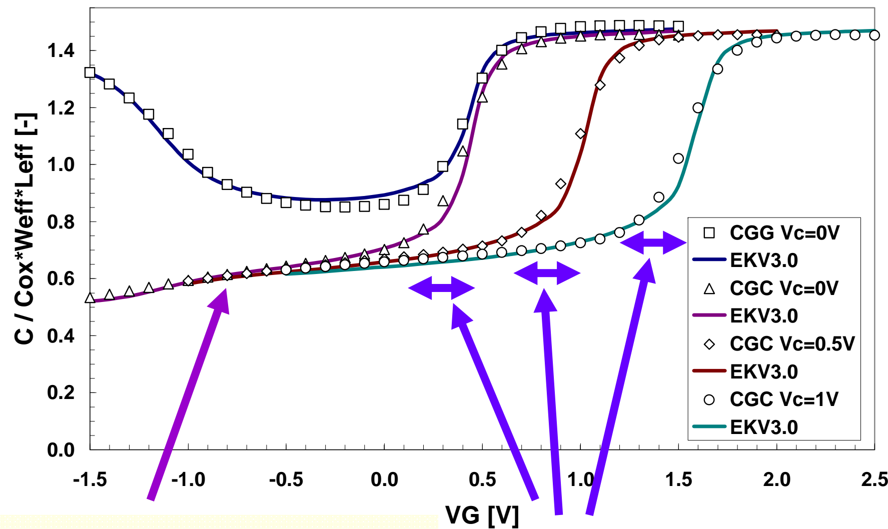
W = 2um, L = 70nm





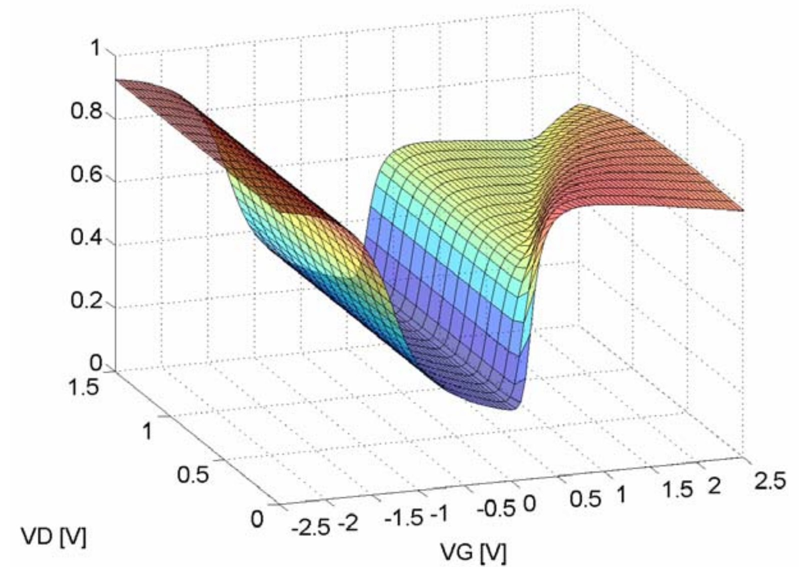
- Illustrates combination of: DIBL, CS, velocity saturation, CLM modelling @ Lgate = 70nm

EKV3 – CV characteristics of MOSFETs



Overlap & fringing caps.
(do NOT scale with L)

Moderate Inversion



- Moderate inversion in MOSFETs – highly important for analog/RF IC design
- Good trade-off among gain, speed, linearity, noise, matching
- Low-medium saturation voltage, series resistance effect negligible
- Reduced impact of mobility effects (vertical field) and velocity saturation

Outline

- Motivation – the need for moderate inversion design
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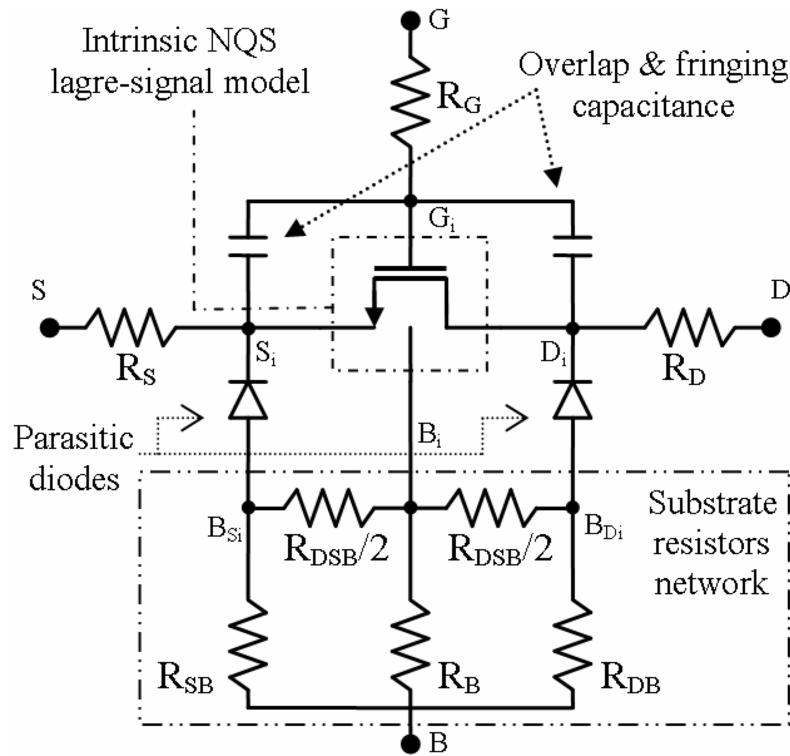
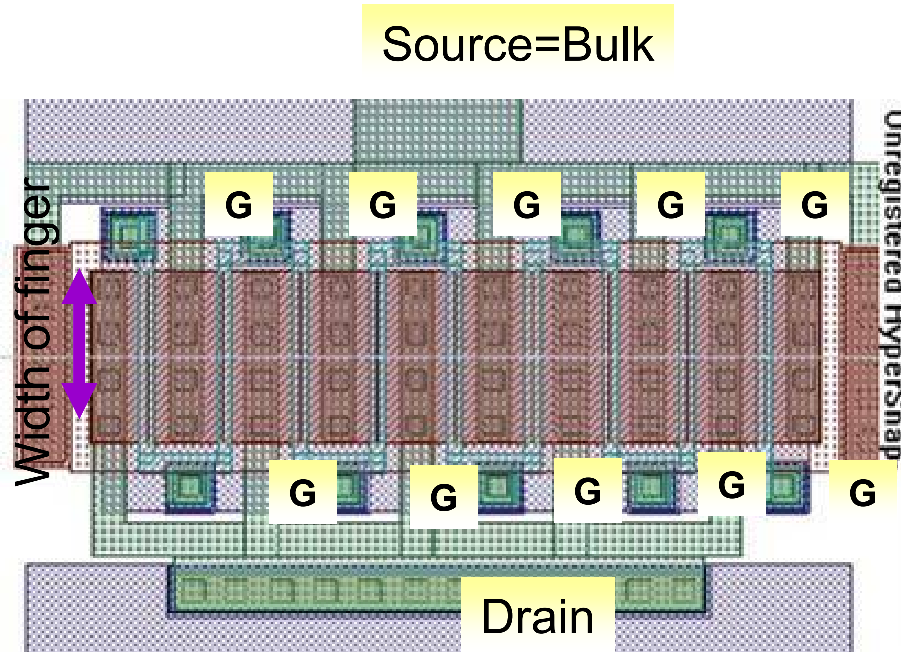
EKV3 scalable model for high frequency

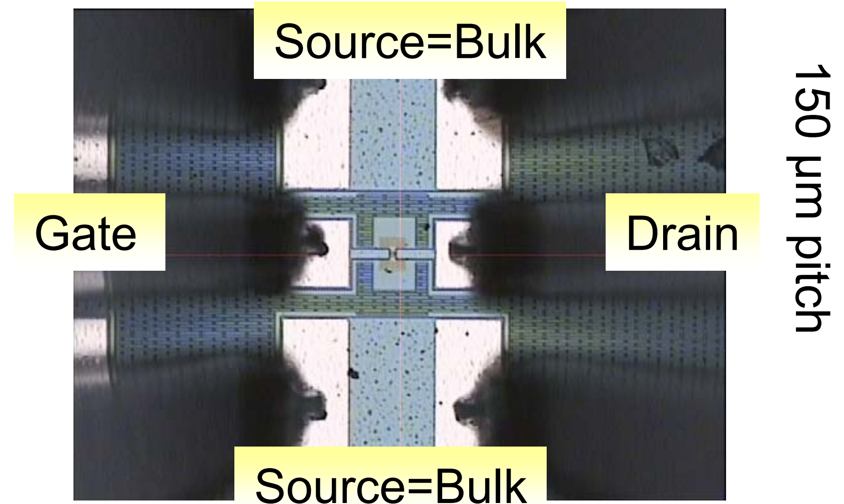


- Non quasi-static model (NQS)
  - ✓ channel segmentation
  - ✓ consistent AC/transient
- Gate- and substrate- parasitics scale with multi-finger layout

R_G	$\sim W_f/(L*N_F)$
R_{SB}, R_{DB}	$\sim 1/W_f$
R_B	$\sim 1/W_f$
R_{DSB}	$\sim L/(W_f*N_F)$

Multi-finger RF MOSFETs

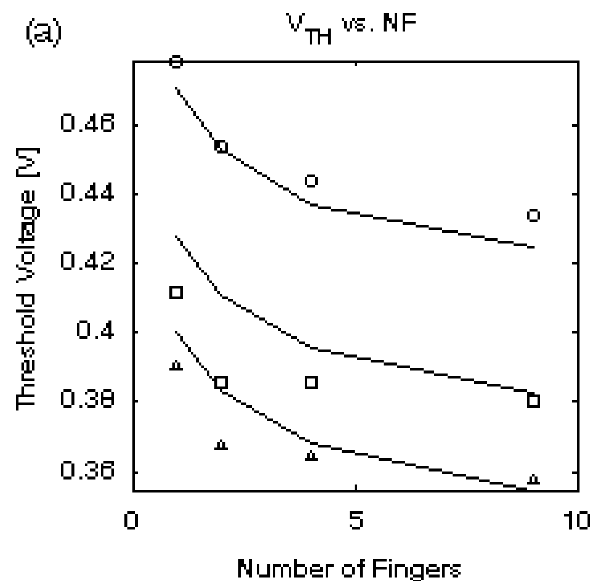


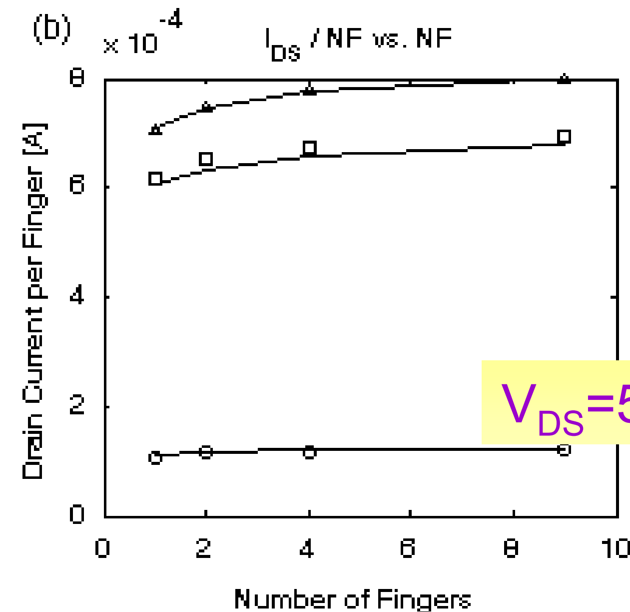


Bazigos e.a., Physica Status Solidi C(5), 2008

- Layout of RF multi-finger MOSFET
  - ✓ Number of fingers – N_F
  - ✓ Finger Width – W_f
  - ✓ Gate Length – L
- Ground-Signal-Ground (GSG) RF Pads
  - ✓ 2 port configuration
- Open-Short de-embedding structures

STI stress in multi-finger RF MOSFETs





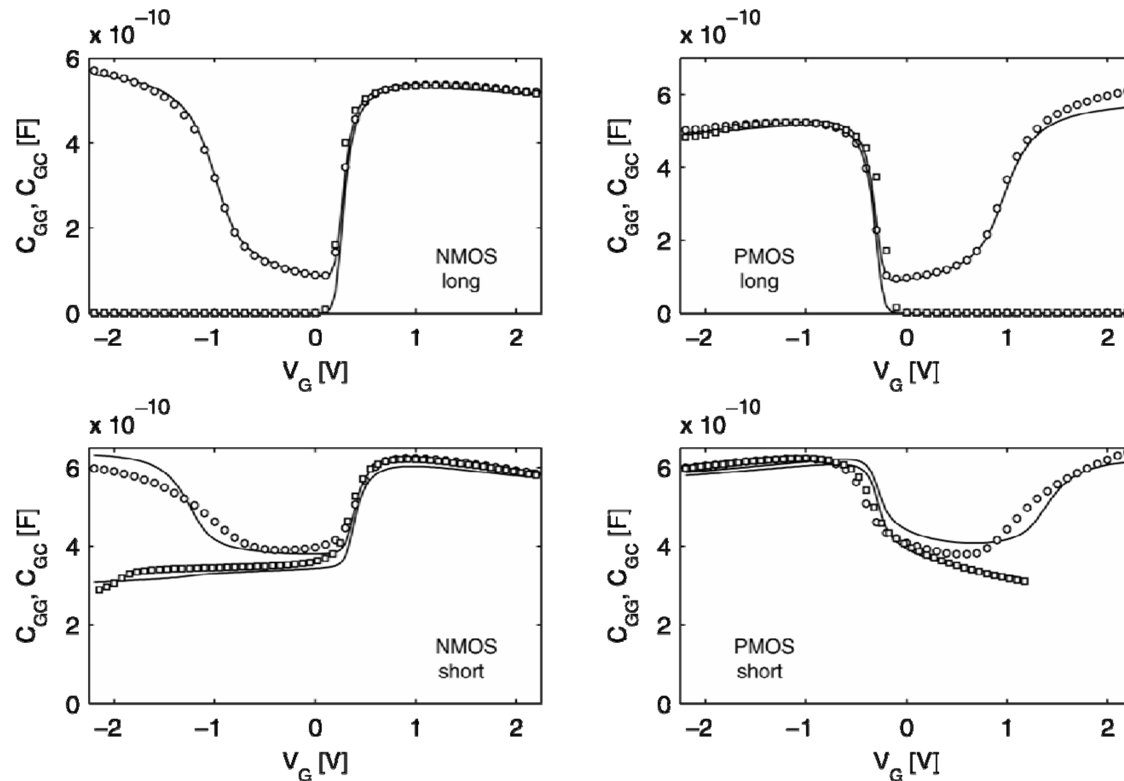
– EKV3
□ meas.

V_{DS}=50m, 0.5, 1V

Bazigos e.a., Physica Status Solidi C(5), 2008

- NMOS, L=180nm, W_f=2µm
- Layout-dependent stress effects due to shallow-trench isolation (STI)
  - ✓ Threshold voltage dependence V_T vs. N_F
  - ✓ Max. drain current dependence I_D / N_F vs. N_F

CV

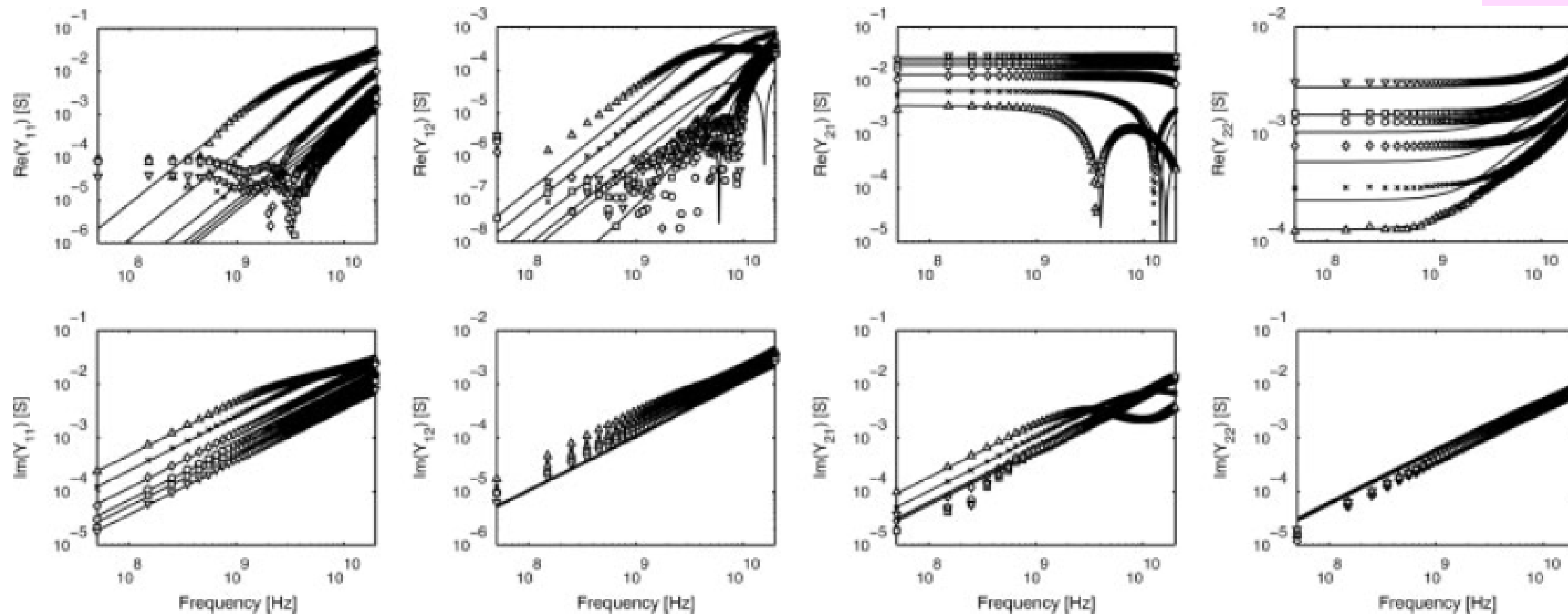


Bucher e.a., RFMiCAE(18), 2008

- Long/short gate and inversion capacitance

EKV3 RF scalability with L

– EKV3
☐ meas.

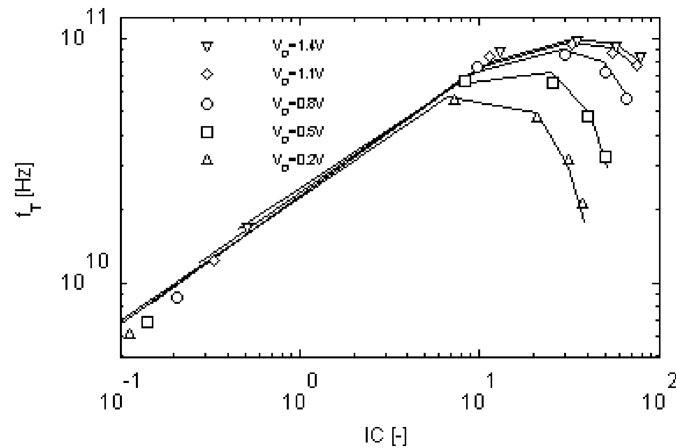


Bucher e.a., RFMiCAE(18), 2008

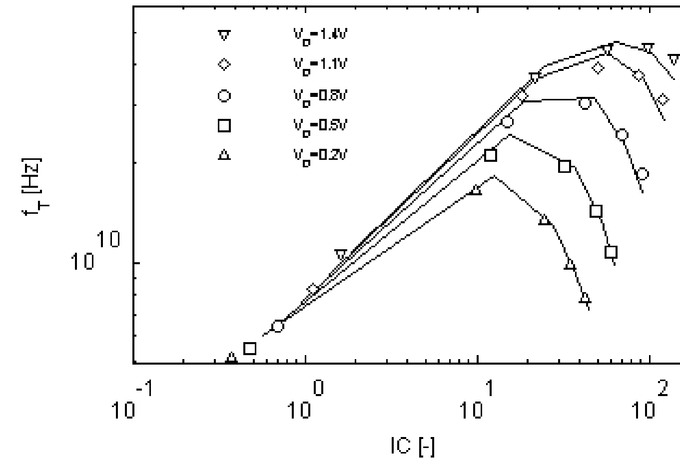
- Y parameter scalability over channel length for NMOS
  - ✓ L=110 nm, 180 nm, 250 nm, 450 nm, 1 um, 2um
  - ✓ W=5 um, NF=10
  - ✓ VG=0.6V, VD=0.5V

EKV3 F_T modelling

– EKV3
☐ meas.



NMOS, L = 110nm

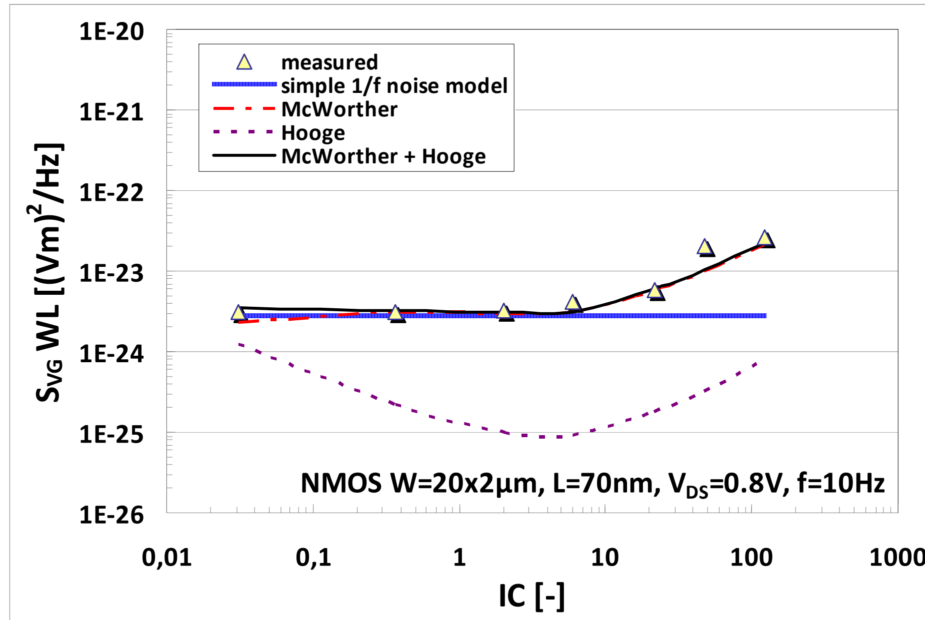


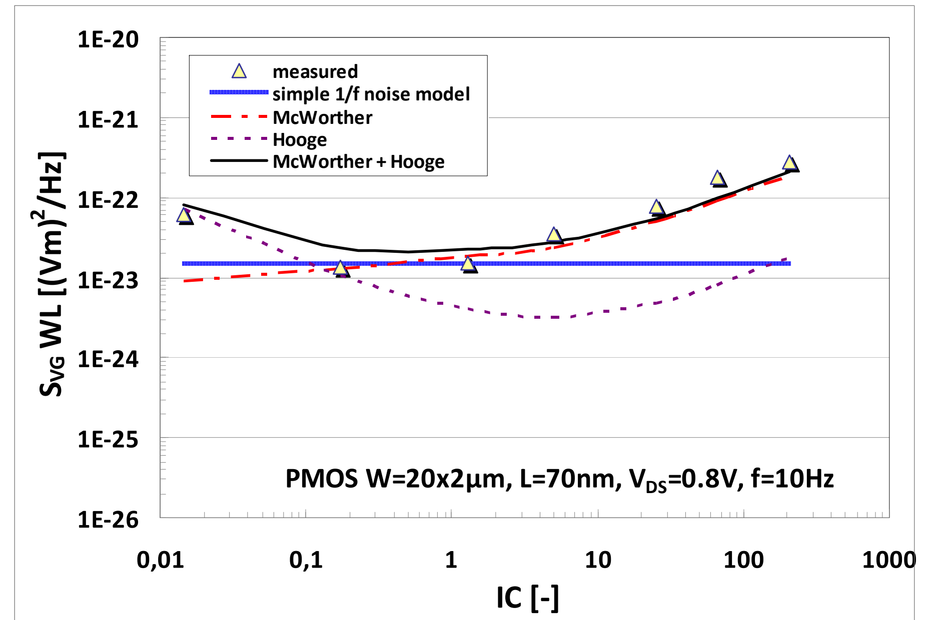
PMOS, L=110nm

Bucher e.a., RFMiCAE(18), 2008

- F_T versus IC in 110nm CMOS, EKV301.02 model
- Highest F_T is reached at IC ~10-30 (!)
- Most probable range for biasing of RF circuits for low noise is:
  1 < IC < 20 (depending on technology and application)

Low frequency noise with EKV3.1





Mavredakis e.a., WCM-NanoTech, 2010

- Bias dependence of low frequency noise covered (EKV3.1)
- Combines carrier number and mobility fluctuations
- Increase in noise in strong inversion
- Increase in noise (referred to gate) may also be observed in weak inversion

Outline

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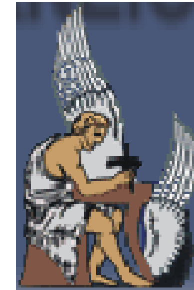
Conclusions

- Moderate inversion design even at RF (scaling!)
- Future (today!) DG and FinFET technologies give:
  - better short-channel behaviour, higher intrinsic gain. FT may be degraded @same channel length
- EKV3: analog/RF IC design-oriented, charge-based, compact model
  - ✓ Native implementations in: ELDO (Mentor Graphics), Smash (Dolphin), Spectre (Cadence), Smartspice (Silvaco).
  - ✓ Parameter extraction support (GMC Suisse & AdMOS)
  - ✓ Model covers all RF aspects from DC to RF (small/large signal including NQS) and Noise.
  - ✓ Extended RF validations in 180nm, 110nm, 90nm CMOS.
  - ✓ Fully scalable with L, W, NF, bias, f, technology.
  - ✓ Simple model structure & parameter extraction.
- EKV3.1 new model release in 1st quarter 2012.

Acknowledgments



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