A Scalable Advanced RF IC Design-Oriented MOSFET Model

Matthias Bucher,[1] Antonios Bazigos,[2] Sadayuki Yoshitomi,[3] Nobuyuki Itoh[3]

[1] Department of Electronics and Computer Engineering, Technical University of Crete (TUC), 73100 Chania, Greece
[2] Department of Electrical and Computer Engineering, National Technical University of Athens (NTUA), 15773 Athens, Greece
[3] TOSHIBA Corporation, Semiconductor Company, Tokyo, Japan

ABSTRACT: This article presents a validation of the EKV3 MOSFET compact model dedicated to the design of analogue/RF ICs using advanced CMOS technology. The EKV3 model is compared with DC, CV and RF measurements up to 20 GHz of a 110 nm CMOS technology. The scaling behaviour over a large range of channel lengths and bias conditions is presented. Long-channel devices show significant non-quasi static effects while in short-channel devices the parasitics modelling is critical. This is illustrated with Y-parameters and f_t vs. I_D in NMOS and PMOS devices, showing good overall RF modelling abilities of the EKV3 MOSFET model. © 2008 Wiley Periodicals, Inc. Int J RF and Microwave CAE 18: 314–325, 2008.

Keywords: MOSFET; compact model; analogue/RF IC design; RF modelling; NQS effect; scaling

I. INTRODUCTION

The key to designing analogue/RF integrated circuits in advanced CMOS technology [1] lies in successfully trading-off design constraints, such as power consumption, supply voltage, noise, linearity, gain, etc [2]. The circuit simulation model of the MOS transistor should predict electrical behaviour including noise over a very wide range of geometry, bias, temperature and frequency [3, 4]. Non-quasi static (NQS) effects [5] occurring in the intrinsic channel may affect particularly long-channel devices and even more importantly in weak inversion, while extrinsic parasitic elements are particularly important for short-channel devices [6]. Although significant effort has been deployed over the last years to develop scalable RF MOSFET compact models for circuit simulation, it is very rare that their validity is shown simultaneously over a wide range of the above aspects. In the present work, a consistent and extended validation of the recently available charge-based EKV3 [7] MOSFET model will be presented.

The present study is based on a 110 nm CMOS technology featuring a triple well with shallow-trench isolation (STI), with multi-V_{TH} MOSFETs at 1.5 V/ 2.5 V. The gate and source-drain use Co-silicidation while the oxide uses oxynitride as an insulator. The channels are halo-implanted as shown in Figure 1. Further detail of device fabrication may be found in [8–10].

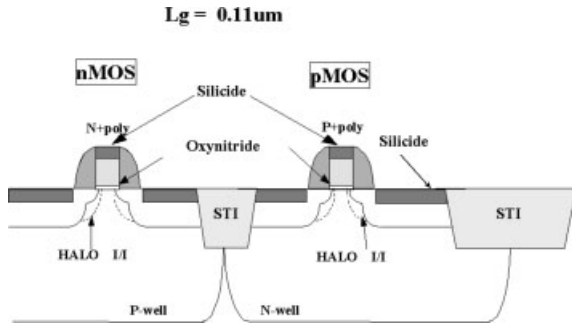**Figure 1.** Cross-section of NMOS and PMOS transistors with minimum $L = 0.11$ μm, $T_{ox} = 2.3$ nm.

Available devices for RF characterization are NMOS and PMOS type transistors within a classic multi-finger layout as shown in Figure 2. Gate lengths considered in the present work range from $L_f = 110$ nm to 2 μm, with a fixed finger width $W_f = 5$ μm and a number of fingers $N_f = 10$. The sources of the transistors are grounded.

The study is organized as follows. The static EKV3 charge-based model structure is first presented. High-frequency equivalent circuit and corresponding equations are introduced and the RF parasitics network is discussed. DC, CV and RF operation of the devices is then presented with emphasis on scaling over bias conditions and channel length. All aspects are illustrated equally for both NMOS and PMOS transistors.

II. STATIC MODEL: THE CHARGE-BASED EKV MOSFET MODEL

In the EKV model, the pinch-off voltage V_P serves as a reference for the channel voltage. V_P is conveniently expressed as [11],

$$V_P \cong \frac{V_G - V_{TO}}{n} \quad n = 1 + \frac{\gamma}{2\sqrt{V_P + \phi}} \quad (1)$$

where V_{TO} is the threshold voltage and n the slope factor. The latter depends in turn on the body effect factor γ and (twice) the Fermi potential Φ. Inversion charge at source and drain q_s and q_d are related to the quantities $V_P - V_S$ and $V_P - V_D$, respectively, as [12, 13]

$$\frac{V_P - V_S}{U_T} = 2q_s + \ln q_s$$
$$\frac{V_P - V_D}{U_T} = 2q_d + \ln q_d \quad (2)$$

where U_T is the thermodynamic potential. On the other hand, the drain current I_D is expressed as,

$$I_D = I_{SPEC} \cdot (i_f - i_r) \quad (3)$$

where I_{SPEC} is the so-called specific current of the device, and the forward and reverse currents i_f and i_r are related to the inversion charge q_s and q_d as,

$$i_f = q_s^2 + q_s$$
$$i_r = q_d^2 + q_d \quad (4)$$

In turn, the transconductances are related to inversion charges,

$$g_{ms} = q_s \cdot \frac{I_{SPEC}}{U_T}$$
$$g_{md} = q_d \cdot \frac{I_{SPEC}}{U_T}$$
$$g_m = \frac{g_{ms} - g_{md}}{n} \quad (5)$$
$$g_{mb} = \frac{n - 1}{n} \cdot (g_{ms} - g_{md})$$

The ratio of transconductance to current, an important design quantity in analogue circuits, is again directly related to inversion charge or forward current [12–14],

$$\frac{g_{ms} U_T}{I_D} = \frac{1}{1 + q_s} = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_f}}$$
$$\frac{g_m U_T}{I_D} = \frac{1}{n} \cdot \frac{1}{1 + q_s} = \frac{1}{n} \cdot \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + i_f}} \quad (6)$$
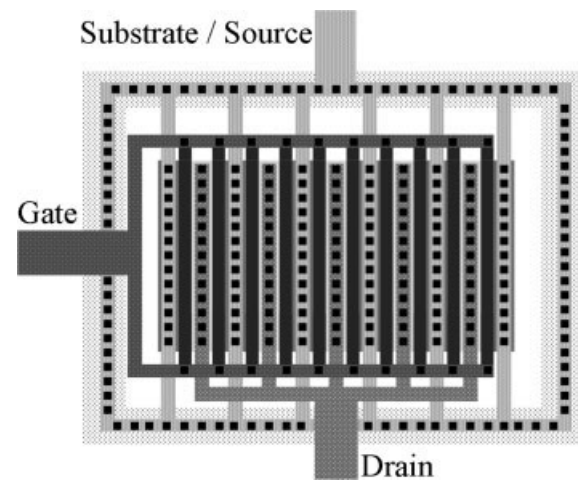

Figure 2. Layout of multi-finger RF transistors, with variable $L_f = 0.11$, 0.18, 0.25, 0.45, 1, 2 μm, $W_f = 5$ μm, $N_f = 10$. The transistors are embedded in a Ground-Signal-Ground (GSG) padframe with grounded source.
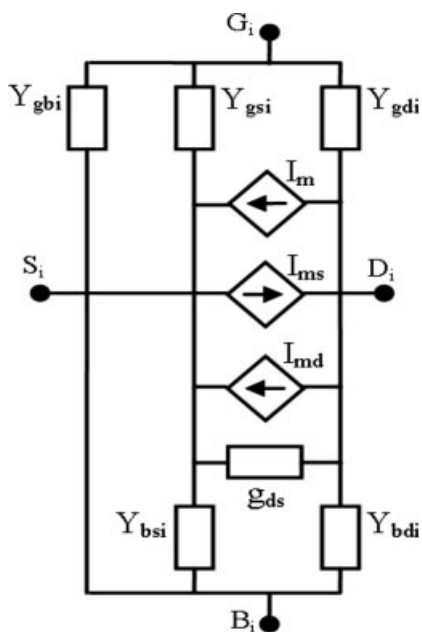
Figure 3. Small-signal equivalent circuit of the NQS intrinsic MOSFET.

Figure 4. RF model of the MOS transistor with extrinsic elements for gate- and substrate-parasitics network.

a relationship which holds in saturation from weak inversion ($i_f < 0.1$) to moderate ($0.1 < i_f < 10$) and strong inversion ($i_f > 10$).

The model presented so far is ideal and does not yet include higher-order effects such as short-channel effects, nor parasitics. Of course these need to be included in the full computer simulation model. Polydepletion and quantum effects are among the fundamental effects affecting device performance [15]. Important mobility and velocity saturation effects are the cause of reduced device mobility and therefore are a significant limit for short-channel performance [7, 11]. Furthermore, other important short-channel effects affecting notably threshold voltage—namely reverse short-channel effect and drain induced barrier lowering (DIBL)—and substrate effect due to charge-sharing, as well as channel length modulation need to be considered. The halo-doping implants are indispensable to control DIBL in short-channel devices, however, they are the cause of degradation in terms of analogue performance at long channel [7]. Layout-dependent stress is finally an important source of deviation of device behaviour in advanced CMOS technology [10]. Another important parasitic effect in advanced CMOS is also gate tunnelling leakage. The EKV3 model has a comparatively low number of parameters to efficiently cope with all these effects [7].
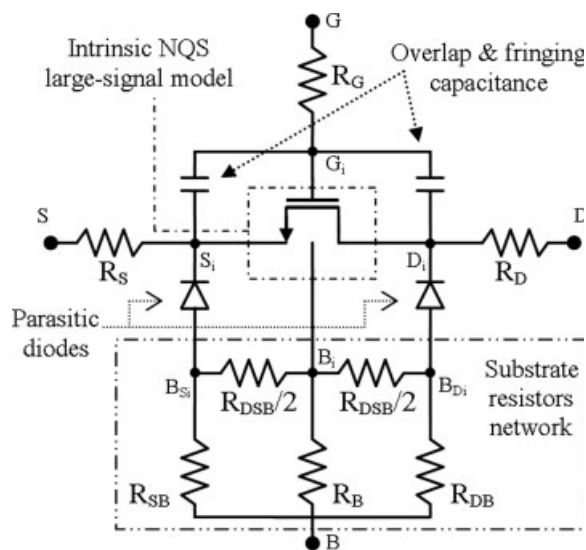
III. MODEL AT HIGH FREQUENCIES

High-frequency operation of MOSFETs requires above all accounting for the frequency response of the intrinsic channel—basically, a transmission line effect leading to the NQS phenomena. Figure 3 presents a general equivalent small-signal circuit of the MOSFET in NQS operation [3, 5].

The three voltage controlled current sources are characterized by three respective transadmittances Y_m, Y_{ms} and Y_{md}.

$$
\begin{aligned}
Y_{ms} &\cong g_{ms} \cdot \frac{1}{1 + j \cdot \omega\tau_{qs}} \\
Y_{md} &\cong g_{md} \cdot \frac{1}{1 + j \cdot \omega\tau_{qs}} \\
Y_m &= \frac{Y_{ms} - Y_{md}}{n}
\end{aligned}
\tag{7}
$$

The five admittances Y_{gsi}, Y_{gdi}, Y_{gbi}, Y_{bsi} and Y_{bdi} are related to each other as,

TABLE I.   Scaling Rules for Resistors in the Extrinsic Gate- and Substrate-Parasitics Network for Multi-Finger Devices

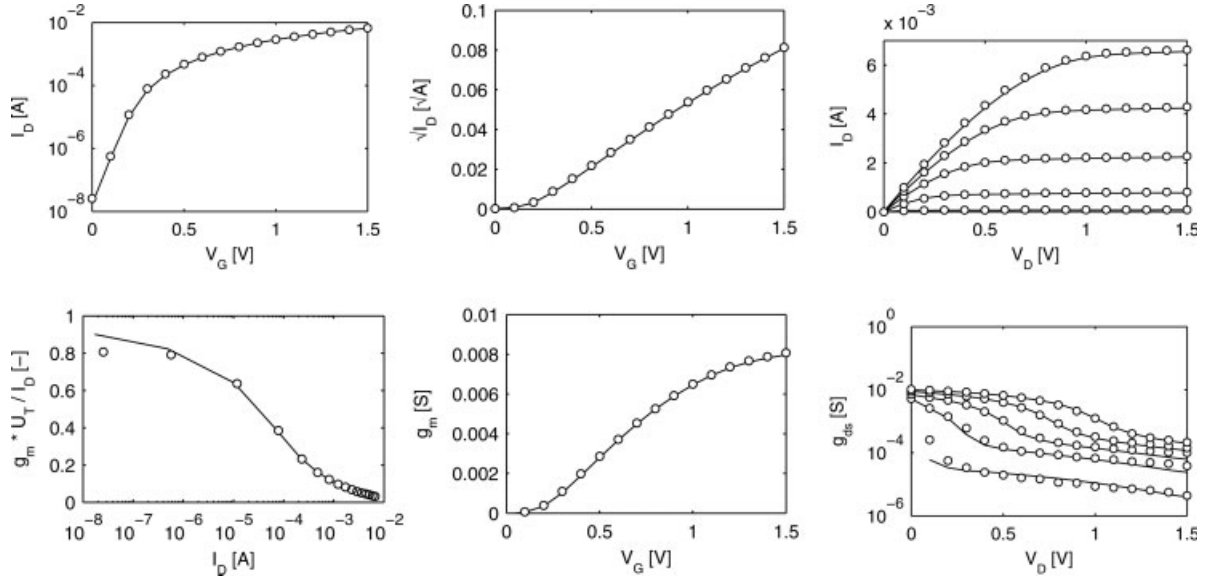|	Scaling Rule
R_G	$\propto W_f/(L_f \times N_f)$
R_{SB}, R_{DB}	$\propto 1/W_f$
R_B	$\propto 1/W_f$
R_{DSB}	$\propto L_f/(W_f \times N_f)$

Figure 5. Static characteristics of a long channel NMOS transistor, $L_f = 2$ μm, $W_f = 5$ μm, N_f = 10. I_D versus V_G with $V_D = 1.5$ V and I_D versus V_D with $V_G = 0.3, 0.6, 0.9, 1.2, 1.5$ V and $V_S = V_B = 0$ V. Markers: measured data, Lines: EKV3 model.

$$
\begin{aligned}
Y_{gsi} &\cong j\omega C_{gsi} \cdot \frac{1}{1 + j \cdot \omega\tau_{qs}/2} \\
Y_{gdi} &\cong j\omega C_{gdi} \cdot \frac{1}{1 + j \cdot \omega\tau_{qs}/2} \\
Y_{gbi} &= \frac{n-1}{n} \cdot (j\omega C_{ox} - Y_{gsi} - Y_{gdi}) \\
Y_{bsi} &= n - 1 \cdot Y_{gsi} \\
Y_{bdi} &= n - 1 \cdot Y_{gdi}
\end{aligned}
\tag{8}
$$

where C_{gsi} and C_{gdi} are defined as,

$$
\begin{aligned}
\frac{C_{gsi}}{C_{ox}} &= \frac{q_s}{3} \frac{2q_s + 4q_d + 3}{(q_s + q_d + 1)^2} \\
\frac{C_{gdi}}{C_{ox}} &= \frac{q_d}{3} \frac{2q_d + 4q_s + 3}{(q_s + q_d + 1)^2}
\end{aligned}
\tag{9}
$$

In the above Y-parameters, a characteristic intrinsic time constant τ_{qs} for the NQS effects is defined as [3],
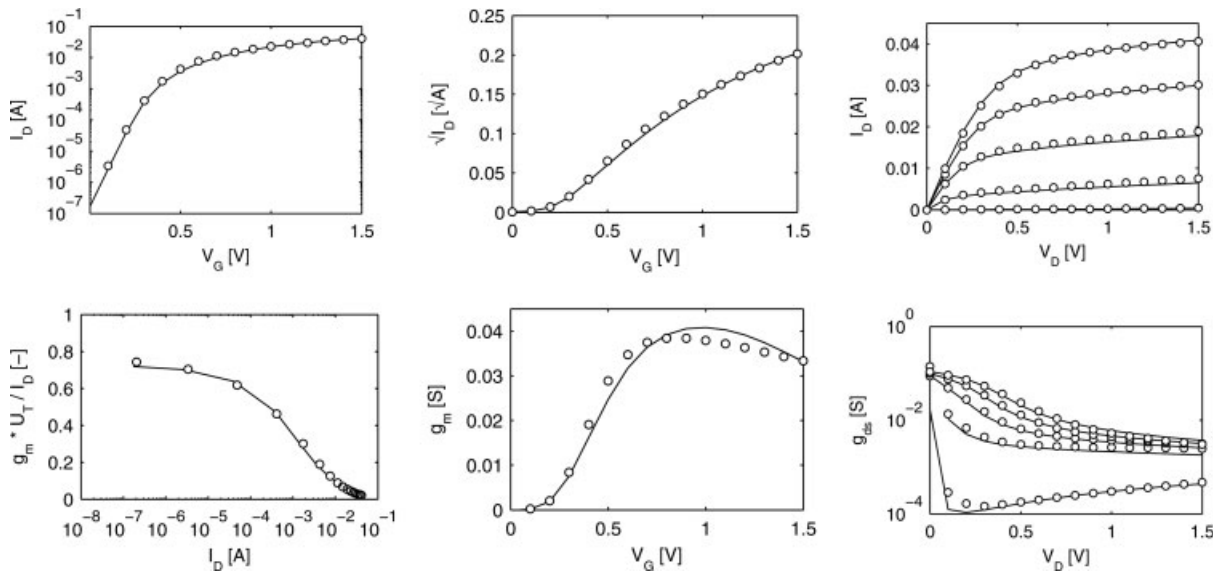

Figure 6. Static characteristics of a short channel NMOS transistor, $L_f = 0.11$ μm, $W_f = 5$ μm, $N_f = 10$. I_D versus V_G with $V_D = 1.5$ V and I_D versus V_D with $V_G = 0.3, 0.6, 0.9, 1.2, 1.5$ V and $V_S = V_B = 0$ V. Markers: measured data, Lines: EKV3 model.
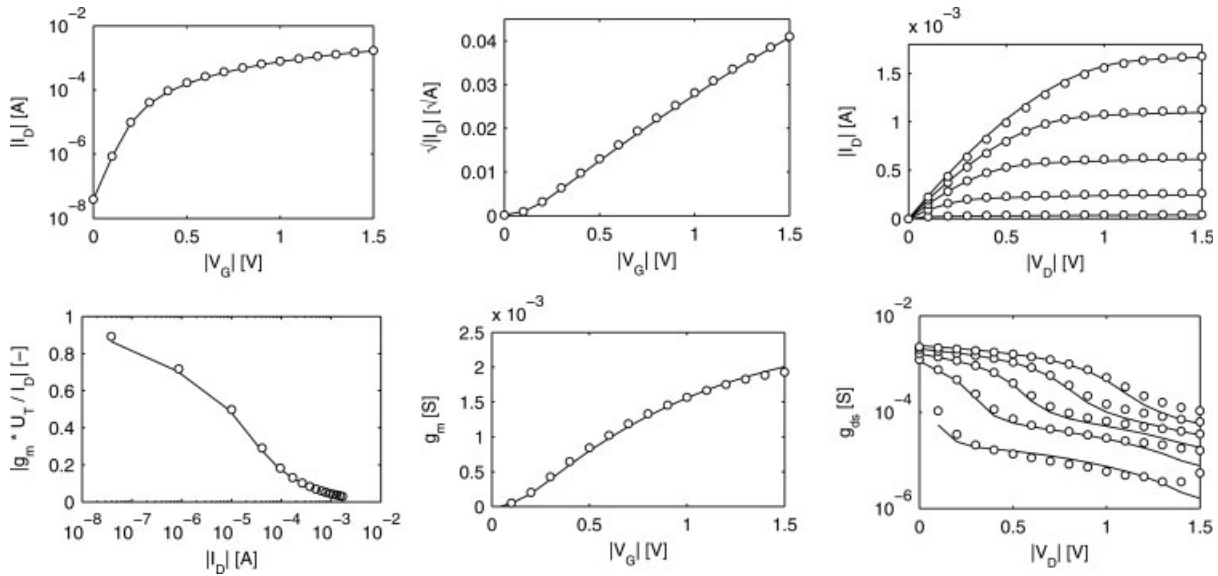
Figure 7. Static characteristics of a long channel PMOS transistor, $L_f = 2~\mu m$, $W_f = 5~\mu m$, $N_f = 10$. I_D versus V_G with $|V_D| = 1.5$ V and I_D versus V_D with $|V_G| = 0.3, 0.6, 0.9, 1.2, 1.5$ V and $|V_S| = |V_B| = 0$ V. Markers: measured data, Lines: EKV3 model.

$$\tau_0 = \frac{L^2}{\mu U_T}$$

$$\frac{\tau_{qs}}{\tau_0} = \frac{1}{30} \frac{4q_s^2 + 10q_s + 12q_sq_d + 10q_d + 4q_d^2 + 5}{(q_s + q_d + 1)^3} \tag{10}$$

which scales essentially with the square of the channel length, and inversely proportional to mobility μ and U_T. In saturation, the intrinsic time constant is,

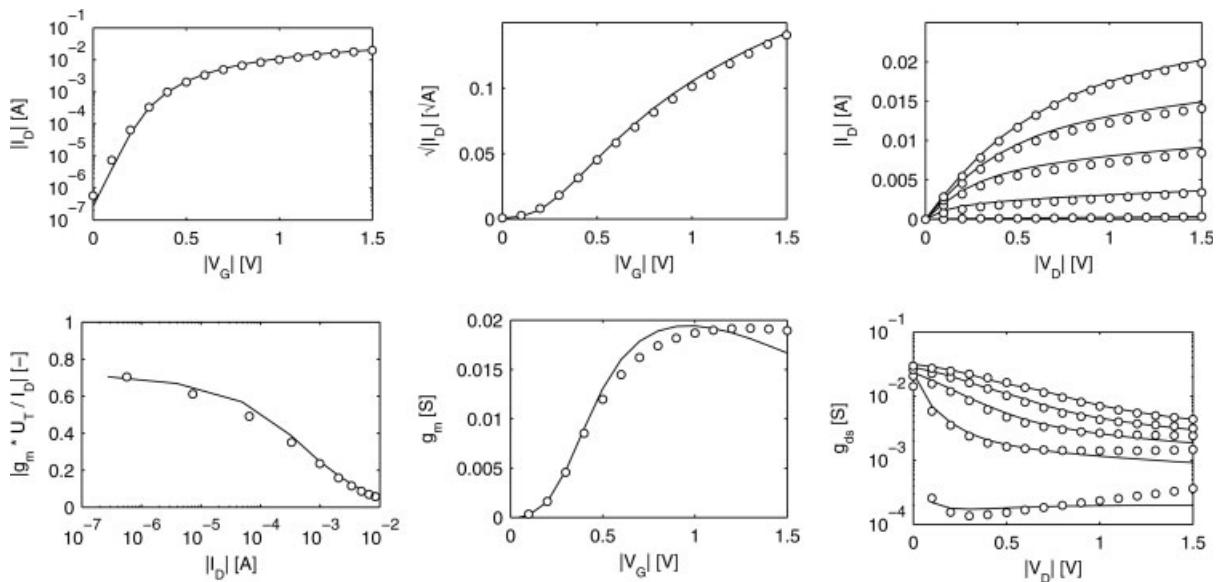$$\frac{\tau_{qs|saturation}}{\tau_0} = \frac{1}{30} \frac{4q_s^2 + 10q_s + 5}{(q_s + 1)^3} \tag{11}$$

Figure 8. Static characteristics of a short channel PMOS transistor, $L_f = 0.11~\mu m$, $W_f = 5~\mu m$, $N_f = 10$. I_D versus V_G with $|V_D| = 1.5$ V and I_D versus V_D with $|V_G| = 0.3, 0.6, 0.9, 1.2, 1.5$ V and $|V_S| = |V_B| = 0$ V. Markers: measured data, Lines: EKV3 model.
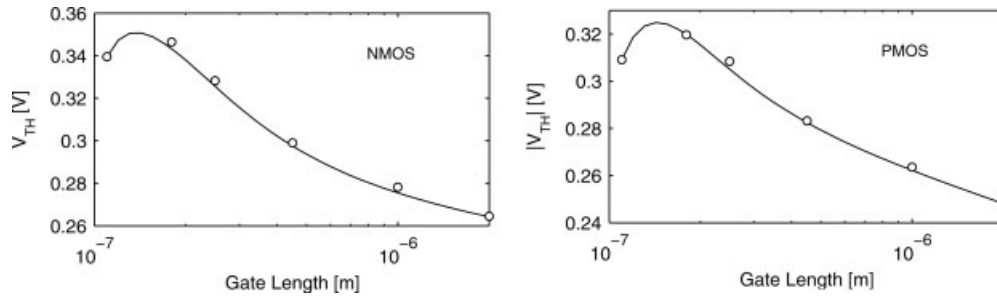
Figure 9. Threshold voltage V_{TH} versus channel length L for the NMOS and PMOS transistors in saturation. $|V_D| = 1.5$ V. Extraction of V_{TH} is based on a current criterion $I_D = I_{TH\square} * W/L$, NMOS: $I_{TH\square} = 1.6$ μA; PMOS: $I_{TH\square} = 0.8$ μA. Markers: measured data, Lines: EKV3 model.

We then define a transcapacitance as,

$$C_m = g_m \cdot \tau_{qs} \qquad (12)$$

Short-channel devices are significantly affected by the extrinsic parasitics, mostly gate and substrate resistances and overlap and fringing capacitances. A subcircuit as shown in Figure 4 is used to represent these effects. The scaling of the parameters follows the rules shown in Table I.

Y-parameters are a convenient means to interpret a number of MOS transistor parameters [3] in terms of transconductances, transcapacitances and access resistances. Combining the preceding small-signal analysis of the intrinsic MOSFET with the effect of R_G and R_B, assuming however $R_{SB} = R_{DB} = \infty$ and $R_{DSB} = 0$, the Y-parameters may be expressed in the case of the 2-port configuration in saturation, as [16],
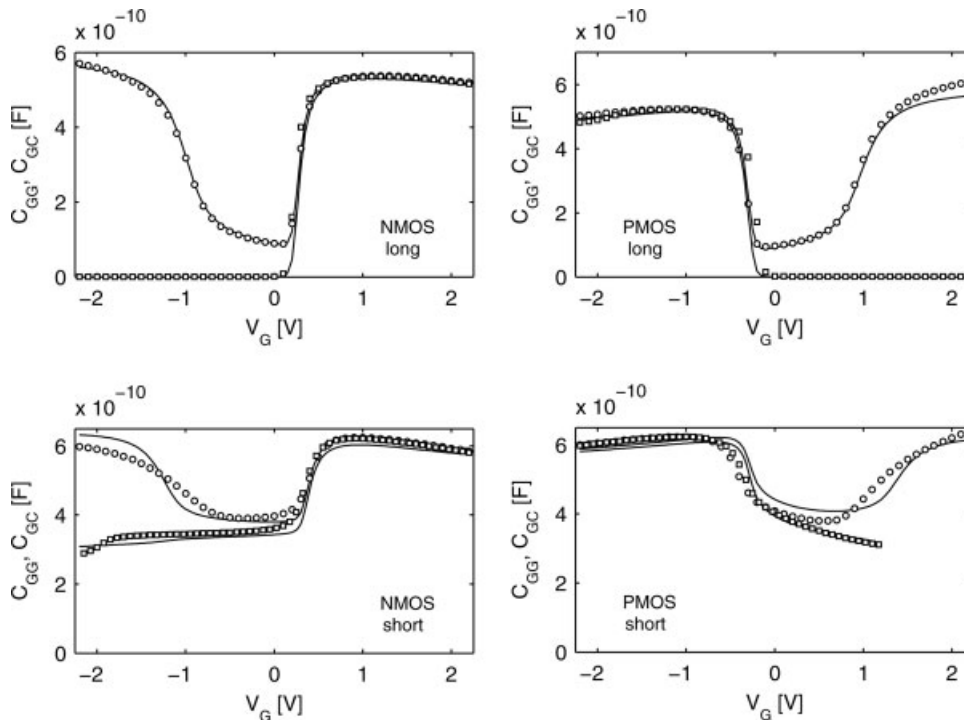

Figure 10. CV characteristics of long ($L = 200$ μm, $W = 250$ μm, $M = 1$) and short ($L = 0.11$ μm, $W = 101$ μm, $M = 4500$) NMOS and PMOS transistors. Markers: measured data, Lines: EKV3 model.
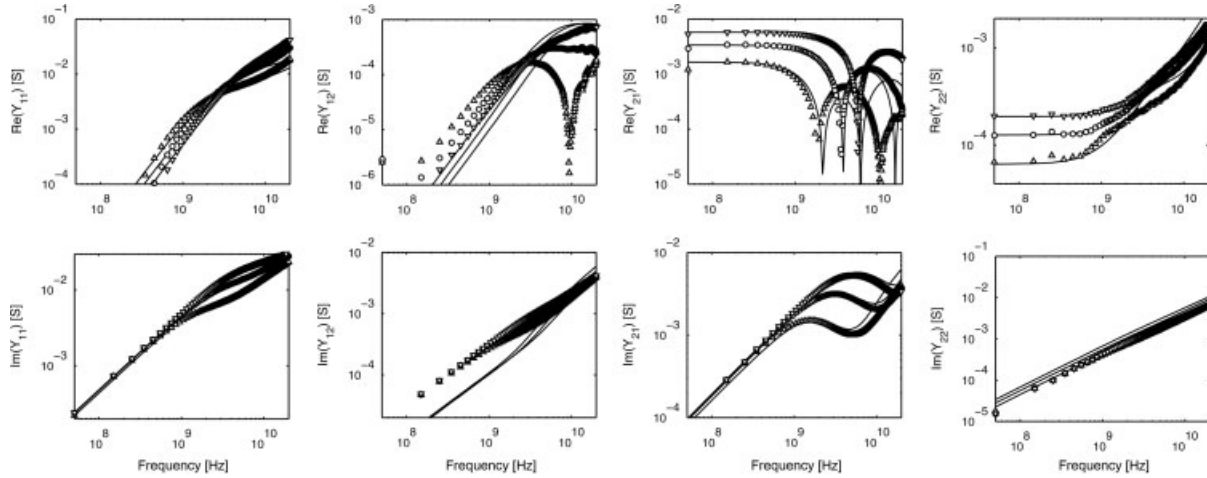
Figure 11. Y-parameters for a multi-finger NMOS transistor with $L_f = 2$ μm, $W_f = 5$ μm, $N_f = 10$. $(V_G, V_D) = (0.4$ V, 0.3 V)[▼], (0.6 V, 0.5 V)[■], (0.9 V, 0.8 V)[▲]. Markers: measured data, Lines: EKV3 model.

$$Y_{11} \cong \omega^2 R_g C_{gg}^2 + j\omega C_{gg}$$

$$Y_{12} \cong -\omega^2 R_g C_{gg} C_{gd} - j\omega C_{gd}$$

$$Y_{21} \cong g_m - \omega^2 R_g C_{gg}(C_m + C_{gd})$$
$$- j\omega(C_m + C_{gd} + g_m R_g C_{gg})$$

$$Y_{22} \cong g_{ds} + \omega^2$$
$$\left[\begin{array}{l} R_g C_{gd}(C_{gd} + g_m R_g C_{gg}) \\ + R_b C_{bd}(C_{bd} + g_{mb} R_b(C_{bd} + C_{bs} + C_{gb})) \end{array} \right]$$
$$+ j\omega(C_{gd}(1 + g_m R_g) + C_{bd}(1 + g_{mb} R_b)) \quad (13)$$

where the overlap and junction capacitance components are added to the intrinsic capacitances,

$$
\begin{aligned}
C_{gg} &= C_{gs} + C_{gd} + C_{gb} \\
C_{gs} &= C_{gsi} + C_{gso} \\
C_{gd} &= C_{gdi} + C_{gdo} \\
C_{gb} &= C_{gbi} + C_{gbo} \\
C_{bs} &= C_{bsi} + C_{bsj} \\
C_{bd} &= C_{bdi} + C_{bdj}
\end{aligned}
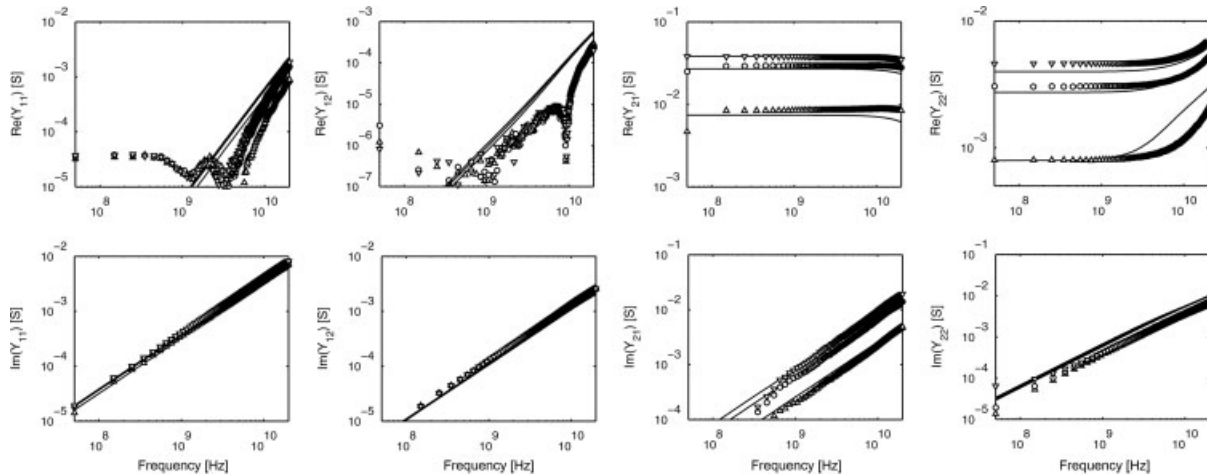\quad (14)
$$

Figure 12. Y-parameters for a multi-finger NMOS transistor with $L_f = 0.11$ μm, $W_f = 5$ μm, $N_f = 10$. $(V_G, V_D) = (0.4$ V, 0.3 V)[▼], (0.6 V, 0.5 V)[■], (0.9 V, 0.8 V)[▲]. Markers: measured data, Lines: EKV3 model.

Figure 13. Y-parameters for a multi-finger PMOS transistor with $L_f = 2$ μm, $W_f = 5$ μm, $N_f = 10$. $(-V_G, -V_D) = (0.4$ V, 0.3 V)[▼], $(0.6$ V, 0.5 V)[■], $(0.9$ V, 0.8 V)[▲]. Markers: measured data, Lines: EKV3 model.

$$R_G = k \frac{1}{3} \frac{W_f}{N_f L_g} \text{RGSH} \tag{15}$$

IV. VALIDATION FROM DC TO RF

In this Section, DC, CV and RF characteristics will be presented. Static and RF characteristics are obtained from the structures presented in Figure 2, while CV characteristics are obtained from separate standard CV characterization structures. We note that one single, scalable model is used coherently for all device characteristics, for either NMOS or PMOS devices.

Static characteristics, including transfer characteristics, gate transconductance, transconductance to current ratio, output characteristics and output conductances are presented in Figures 5–8 for long and short NMOS and PMOS devices, respectively. The threshold voltage evaluated over the range of channel lengths is presented in Figure 9. Good overall fits are obtained with EKV3.

Capacitance-voltage characteristics from accumulation to inversion are presented for long and short NMOS and PMOS devices in Figure 10. Note the bias-dependent overlap capacitances appearing in the short-channel devices, as well as the correct modelling of fringing capacitances at the onset of strong inversion.
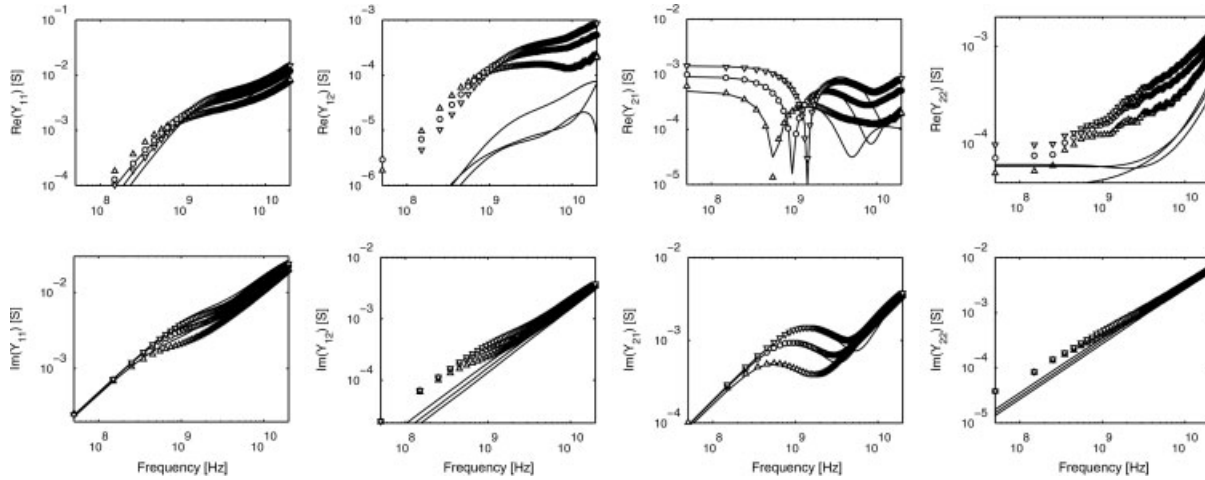
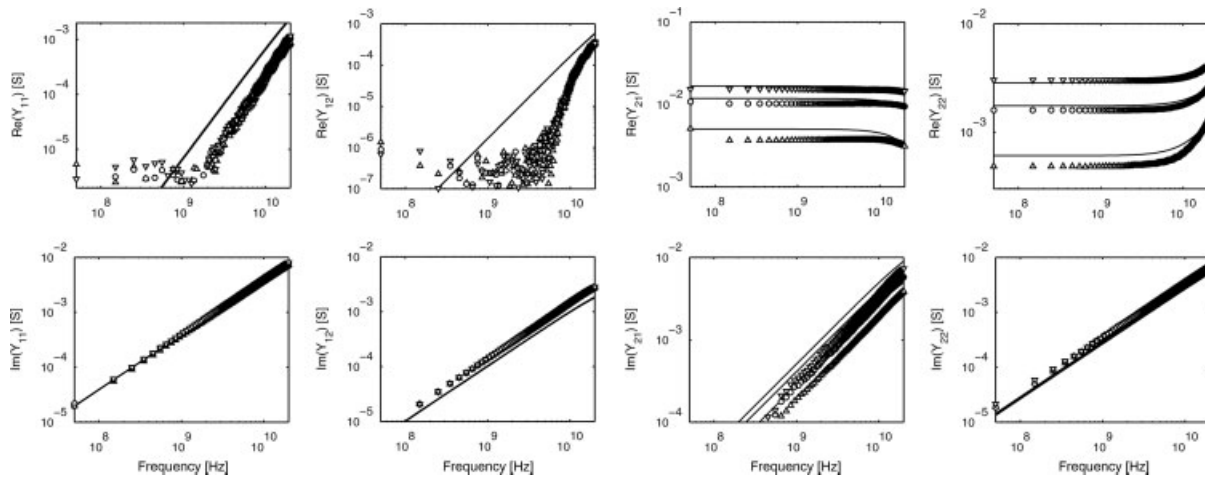

Figure 14. Y-parameters for a multi-finger PMOS transistor with $L_f = 0.11$ μm, $W_f = 5$ μm, $N_f = 10$. $(-V_G, -V_D) = (0.4$ V, 0.3 V)[▼], $(0.6$ V, 0.5 V)[■], $(0.9$ V, 0.8 V)[▲]. Markers: measured data, Lines: EKV3 model.
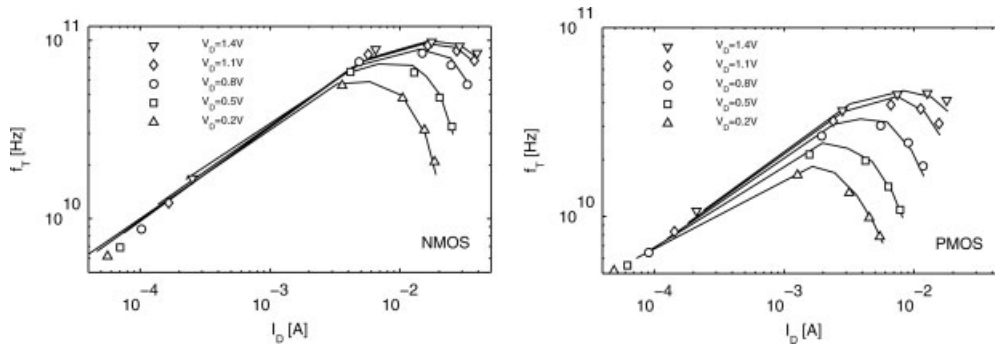
Figure 15. Transition frequency f_t versus I_D for the short NMOS and PMOS transistors with L_f = 0.11 μm, W_f = 5 μm, N_f = 10 at varying drain voltage V_D. Markers: measured data, Lines: EKV3 model.

The four Y-parameters are evaluated versus frequency up to 20 GHz. Long ($L_f = 2$ μm) and short ($L_f = 0.11$ μm) multi-finger NMOS and PMOS devices are represented in Figures 11–14. Note that the three different bias conditions in saturation represent realistic operating conditions—covering moderate to strong inversion—for RF circuits such as a low-noise amplifier (LNA). The bias- and frequency-dependence of real and imaginary parts of Y parameters are qualitatively well represented by the EKV3 model. Only the Y_{12} parameter—particularly the real part—is not ideally matched by the model. Note the small amplitude of both real and imaginary parts of Y_{12} with respect to other Y parameters particularly at low frequency; this should be of limited consequence to design. Experimental difficulties may in part also be responsible for this fact.

Long-channel devices are clearly affected by NQS effects. Note that the simulation model, EKV3, here uses a channel segmentation approach to account for NQS effects [7]. Such an approach ensures compatibility among small-signal frequency-domain and large-signal time-domain simulation. As the present results demonstrate, the five channel segments allow us to represent NQS effects accurately in $L_f = 2$ μm devices in all the available frequency range.

The transit frequency f_t of the short-channel devices were evaluated against the drain current, according to,

$$f_t = |H_{21}(f)| \times f_{spot}, \quad f_{spot} = 10\text{GHz} \qquad (16)$$

The result in Figure 15 shows that EKV3 can accurately reproduce f_t at all drain voltages V_D for all levels of current and for both NMOS and PMOS devices equally well.

Finally, the scaling abilities of the model in terms of Y-parameters are further illustrated in Figures 16

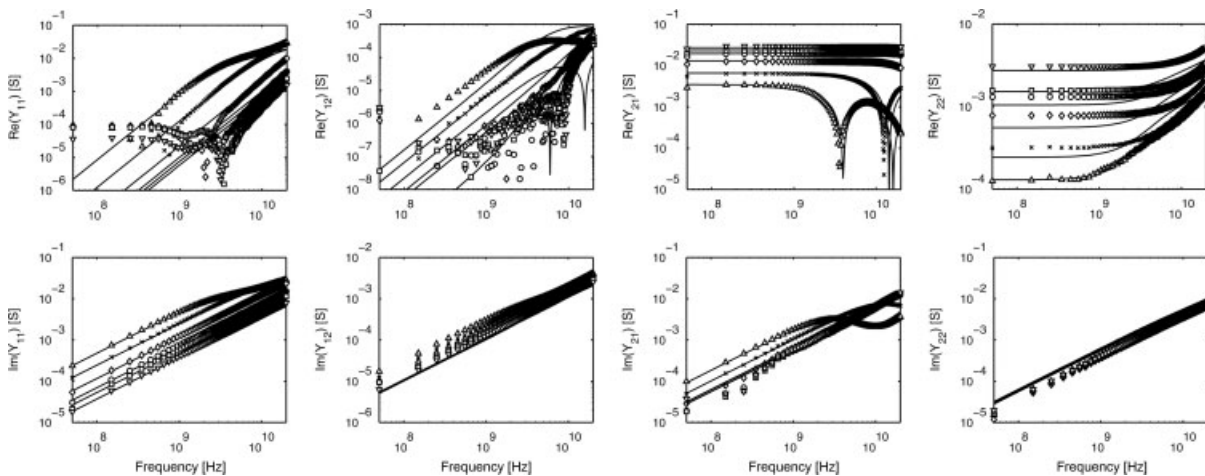**Figure 16.** Y parameters for multi-finger NMOS transistors with L_f = 0.11 μm [▼], 0.18 μm [■], 0.25 μm [○], 0.45 μm [◇], 1 μm [x], 2 μm [▲], W_f = 5 μm, N_f = 10. (V_G,V_D) = (0.6 V, 0.5 V). Markers: measured data, Lines: EKV3 model.
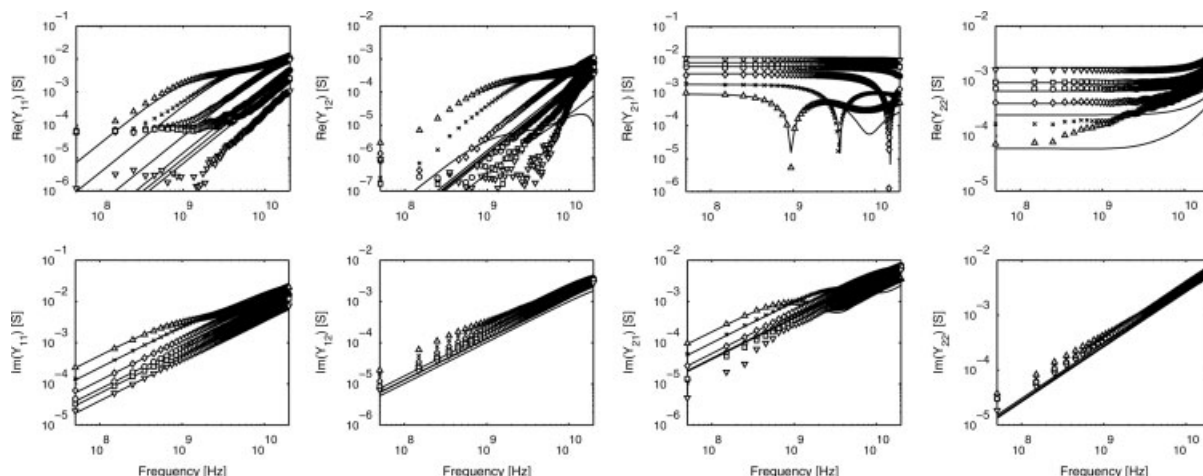
Figure 17. Y parameters for multi-finger PMOS transistors with $L_f = 0.11$ μm [▼], 0.18 μm [■], 0.25 μm [○], 0.45 μm [◇], 1 μm [x], 2 μm [▲], $W_f = 5$ μm, $N_f = 10$. ($|V_G|, |V_D|$) = (0.6 V, 0.5 V). Markers: measured data, Lines: EKV3 model.

and 17 for NMOS and PMOS devices, respectively, for the whole range of channel lengths at the median condition of gate and drain bias.

A comment on the appreciation of the overall modelling quality is in order. The overall good qualitative behaviour—bear in mind that single, scalable parameter sets are used to encompass all device characteristics from static to RF and over all geometry and bias conditions—largely outweighs the occasional imperfect fitting.

Investigation of other scaling aspects, such as dependence on varying number of fingers and different finger width, as well as presentation of RF parameter extraction procedures [3, 4, 6, 16], are beyond the scope of the present work and will be presented elsewhere.

V. CONCLUSIONS

In summary, an extended validation of the charge-based EKV3 MOSFET model for analogue/RF IC design has been presented. The EKV3 model was shown to cover qualitatively well all aspects from DC to CV characteristics and RF parameters up to 20 GHz. RF measurements of multi-finger devices include six different channel lengths ranging from 110 nm to 2 μm for both types of transistors (NMOS and PMOS), at about 25 different bias conditions each. Y-parameters were evaluated over different bias conditions and the whole range of channel lengths, and were shown to be well represented by a

single, scalable model consistent with the DC and CV results. An overall excellent qualitative fit is achieved with the EKV3 model at all bias conditions and channel lengths over the whole frequency range. Non-quasi static (NQS) effects for long-channel devices are shown to be well addressed at all bias conditions up to 20 GHz, while short-channel devices are more notably affected by the gate and substrate parasitics. Note that such extended validation covering a similarly wide geometry space, bias conditions and type of devices is rarely available in literature and has been shown for the first time for the EKV3 model here. Beyond the abilities of the circuit simulation model, the charge-model approach offers manageable expressions including in terms of RF parameters, and thereby provides significant insight into the operation of the device. This underlines the suitability of the EKV3 MOSFET model for analogue/RF CMOS design. The abilities of EKV3 in terms of scalability using advanced CMOS technology have been largely demonstrated.

REFERENCES

1. H.S. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, T. Morimoto, Y. Katsumata, and H. Iwai, High-frequency AC characteristics of 1.5nm gate oxide MOSFET's, Tech Digest Int Electron Device Meeting (1996), 105–108.
2. D.M. Binkley, C.E. Hopper, S.D. Tucker, B.C. Moss, J.M. Rochelle, and D.P. Foty, A CAD methodology for optimizing transistor current and sizing in Analog

CMOS design, IEEE Trans Computer-Aided Design Int Circuits Systems 22 (2003), 225–237.

3. C. Enz, An MOS transistor model for RF IC design valid in all regions of operation, IEEE Trans Microwave Theory Techn 50 (2002), 342–359.

4. Y. Cheng, M.J. Deen, and C.-H. Chen, MOSFET modeling for RF IC design, IEEE Trans Electron Dev 52 (2005), 1286–1303.

5. A.-S. Porret, J.-M. Sallese, and C. Enz, A compact non quasi-static extension of a charge-based MOS model, IEEE Trans Electron Dev 48 (2001), 1647–1654.

6. S. Yoshitomi, Challenges of compact modeling for deep-submicron RF-CMOS devices, Twelfth International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES 2005), Krakow, Poland, 22–25 June 2005.

7. M. Bucher, A. Bazigos, F. Krummenacher, J.-M. Sallese, and C. Enz, EKV3.0: an advanced charge based MOS transistor model, in W. Grabinski, B. Nauwelaers, D. Schreurs, Eds., Transistor Level Modeling for Analog/RF IC Design, Springer, ISBN 1-4020-4555-7, 2006.

8. H. Yoshimura, T. Nakayama, M. Nishigohri, M. Inohara, K. Miyashita, E. Morifuji, A. Oishi, N. Kawashima, M. Habu, H. Koike, H. Takato, Y. Toyoshima, and H. Ishiuchi, A CMOS technology platform for 0.13 μm generation SOC (System on a Chip), Digest Symp VLSI Technol (2000), 144–145.

9. T. Ohguro, T. Ishikawa, T. Kimura, S. Samata, A. Kawasaki, T. Nagano, T. Yoshitomi, and T. Toyoshima, High performance digital-analog mixed device on a Si substrate with resistivity beyond 1 kOhm cm, Tech Digest Int Electron Dev Meeting (2000), 757–760.

10. T. Ohguro, Y. Okayama, K. Matsuzawa, K. Matsunaga, N. Aoki, K. Kojima, H.S. Momose, and K. Ihimaru, The impact of oxynitride process, deuterium annealing and STI stress to 1/f noise of 0.11um CMOS, Symp VLSI Technol Digest (2003), 37–38.

11. C.C. Enz, F. Krumenacher, and E.A. Vittoz, An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications, Analog Integrated Circuits Signal Processing 8 (1995), 83–114.

12. M. Bucher, Analytical MOS transistor modeling for analog circuit simulation, Ph.D. Thesis, No 2114 (1999), Swiss Federal Institute of Technology, Lausanne (EPFL), Switzerland, 2000.

13. J.-M. Sallese, M. Bucher, F. Krummenacher, and P. Fazan, Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model, Solid State Electron 47 (2003), 677–683.

14. M. Bucher, D. Kazazis, F. Krummenacher, D. Binkley, D. Foty, and Y. Papananos, Analysis of transconductances at all levels of inversion in deep submicron CMOS, Proceedings of Ninth IEEE Conference on Electronics, Circuits and Systems (ICECS 2002), Vol. III, Dubrovnik, Croatia, September 15–18, 2002, pp. 1183–1186.

15. C. Lallement, J.-M. Sallese, W. Grabinski, M. Bucher, and P. Fazan, Accounting for quantum effects and polysilicon depletion from weak to strong inversion in a charge-based design-oriented MOSFET model, IEEE Trans Electron Dev 50 (2003), 406–417.

16. F. Krummenacher, M. Bucher, and W. Grabinski, HF MOSFET model parameter extraction, CRAFT deliverable D2.3, European Project No. 25710, July2000. Available at: http://www.lowpower.org/Repository/esdlpd/CRAFT/d23.pdf

BIOGRAPHIES

Matthias Bucher was born in Switzerland in 1964. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology (EPFL), Lausanne, Switzerland, in 1993 and 1999, respectively. The subject of his Ph.D. Thesis was the analytical charge-based compact modelling of MOSFETs. In 1997, he was an invited researcher with LSI Logic, Milpitas, California. From 2000 to 2003, he was a visiting researcher at the National Technical University of Athens (NTUA), Athens, Greece, and held numerous consulting mandates in microelectronics industry. In February 2004, he joined the Department of Electronics and Computer Engineering, Technical University of Crete (TUC), Chania, Greece, as an Assistant Professor. His current research interests are in the design of analogue/RF integrated circuits, and in wide-band characterization and advanced compact modelling of single- and multi-gate nanoscale CMOS as well as high-voltage MOS devices. He also has coordinated the EKV3 MOSFET compact model code development. He is a member of the IEEE and of the Technical Chamber of Greece. He is an author or co-author of over 45 publications in international journals and conferences, as well as of two book chapters.

Antonios Bazigos was born in Athens, Greece, in 1980. He received the diploma degree in electrical and computer engineering in 2003 from the National Technical University of Athens (NTUA), Athens, Greece. Since then he is working on his Ph.D. Thesis at the Laboratory of Microelectronics at NTUA. His field of research is the modelling of the MOS transistor. He is co-working, with the rest of the EKV Team, on the development and the code implementation of the EKV3 MOS transistor compact model.

Sadayuki Yoshitomi was born in Sasebo, Japan, in 1965. He received the B.E., M.E. and Ph.D. degrees from Yokohama National University, Yokohama Japan, in 1988, 1990 and 1993, respectively. The title of his doctor thesis was "Study on the silicon dioxide film deposited by liquid phase deposition (LPD)". His background is the physics of Si/SiO2 interface. In 1993, he joined the Research and Development Center, Toshiba Corporation, Kawasaki Japan, where he was engaged in the research and development of BiCMOS device technologies. Since 2002, he has been with the Analogue CAD Engineering Dept. System LSI Division II, Toshiba Corp. Semiconductor Company. His current field of interest is the investigation of newly developed Bipolar/MOSFET transistor compact models and application of advanced simulation technologies, such as system simulation, mixed-signal simulation and electro-magnetic simulation. He is a member of the organizing committee of MIXDES (International Conference on Mixed Design of Integrated Circuits and Systems).
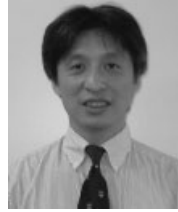
Nobuyuki Itoh was born in Tokyo, Japan, in 1960. He received B.S. and M.S. degrees in chemistry from Tokyo University of Science, Tokyo, Japan, in 1983 and 1985 respectively, and he received Ph.D. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2006. In 1985, he joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, where he was engaged in the research and development of CMOS device technologies for advanced CMOS gate arrays, bipolar device technologies and bipolar circuit design for ECL gate arrays and high-frequency analogue circuits, and RF-CMOS circuit design. He was a visiting scientist at Katholieke Universiteit Leuven, ESAT-MICAS, Leuven, Belgium, from March of 1996 to April of 1998 where he worked on design of fully integrated VCOs and PLLs using RF-CMOS. He has been engaged in the research and development of high-frequency analogue circuit at Semiconductor Company of Toshiba Corporation since 1998. His current research interests are high-frequency integrated circuit for telecommunications. Dr. Itoh is a member of the Institute of Electronics and Communication Engineers of Japan (IEICE) and member of the Institute of Electrical and Electronics Engineers (IEEE). He is also a member of program committee of Custom Integrated Circuit Conference (CICC), Bipolar/BiCMOS Circuit and Technology Meeting (BCTM), European Solid-State Circuits Research Conference (ESSCIRC) and Asia-Pacific Microwave Conference (APMC).