High-Voltage MOSFET compact modelling

The nano-tera.ch Workshop
on the Next Generation MOSFET Compact Models

Antonios Bazigos, François Krummenacher, Jean-Michel Sallese
École Polytechnique Fédérale de Lausanne

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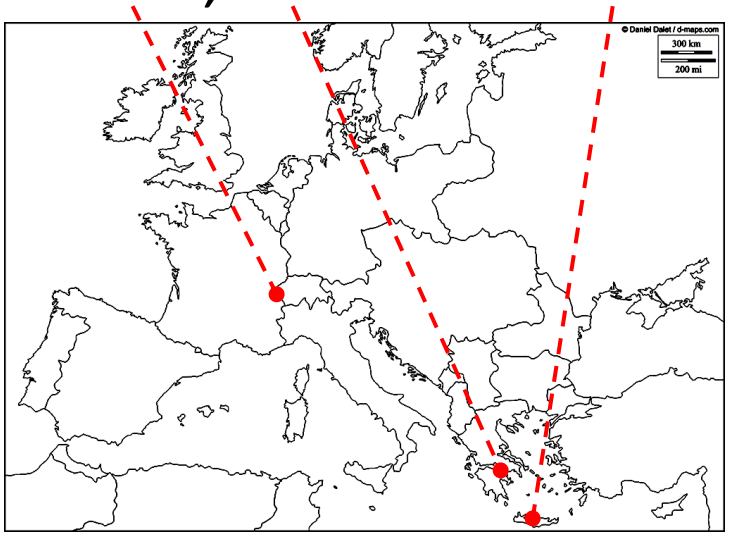
Why am I here?

- Ph.D. Thesis: MOSFET Compact Modelling
  - NTUA, Greece
  - Director: Prof. Matthias Bucher (TUC)
  - Development and implementation of the EKV3 model
  - Collaboration between EPFL, NTUA and TUC



Why am I talking about HV-MOS?

- COMON project (2009 – 2012)
  - COmpact MOdelling Network
  - Post-Doc Researcher
    - Dr. Jean-Michel Sallese (Supervisor)
    - Dr. François Krummenacher
- Three WorkGroups:
  - WG1: Multiple-Gate SOI MOSFETs
  - WG2: High Voltage MOSFETs
  - WG3: Advanced III-V HEMTs

ACKNOWLEDGEMENT: THIS WORK WAS SUPPORTED BY THE EUROPEAN COMMUNITY'S MARIE CURIE IAPP PROGRAM "COMPACT MODELLING NETWORK (COMON)", UNDER GRANT Nº 218255.

Where am I working now?

- NANOLAB
  - Nanoelectronic Devices Laboratory
  - Prof. Adrian Ionescu
  - September 2011
- Modelling and Simulation
  - NEMS/MEMS
  - Verilog-A
  - Numerical Simulations

Target of WG2 (COMON)

- Development / Implementation of a compact model for High-Voltage MOSFET
- Key partners
  - austriamicrosystems
  - Dolphin Integration
    - Simulator: SMASH

Previous Work at EPFL

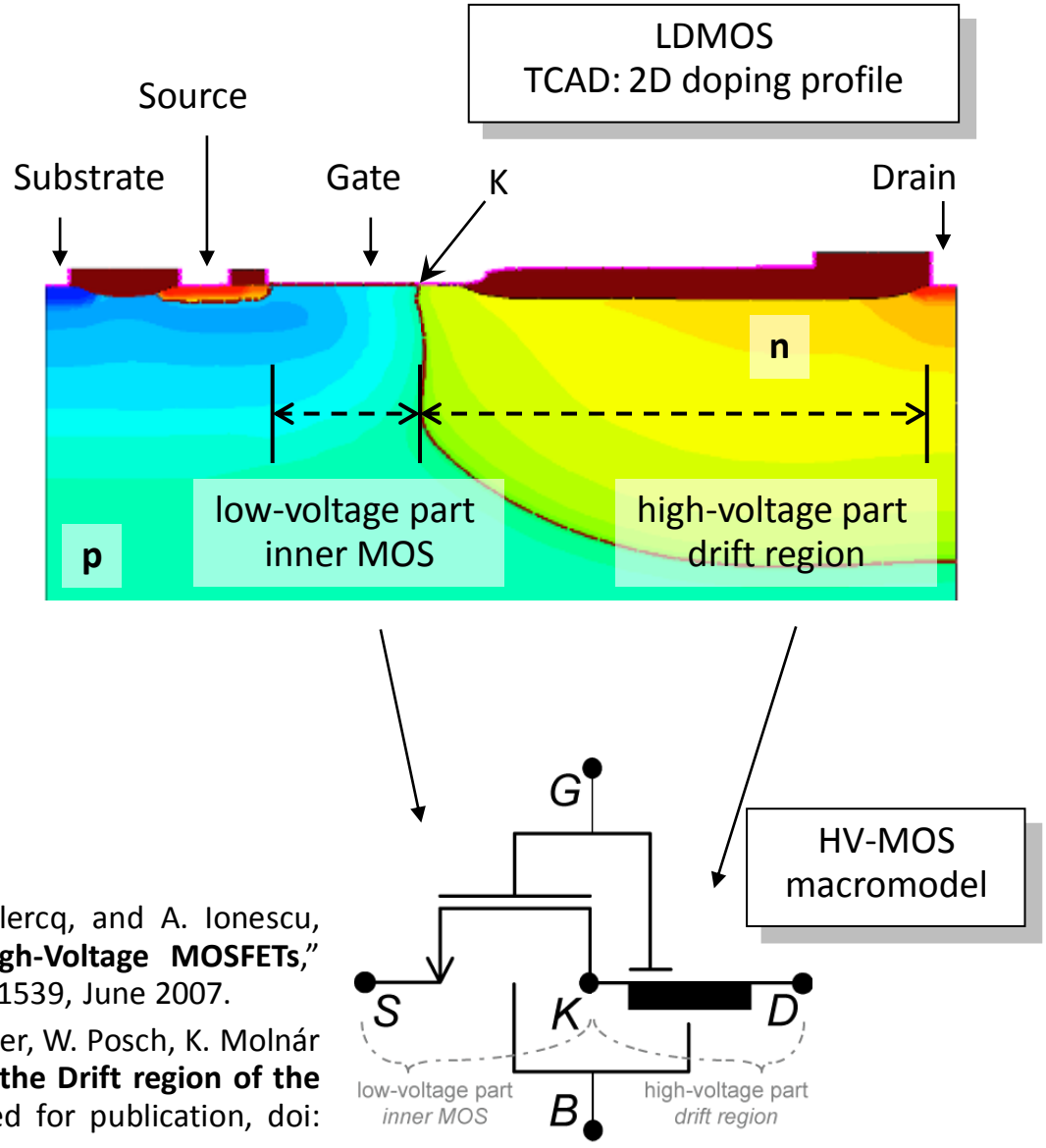
- Ph.D. Theses
  - [1] C. Anghel, “High voltage devices for standard MOS technologies,” EPFL, Lausanne, 2004.
  - [2] N. Hefyene, “Electrical characterization and modelling of lateral DMOS transistor,” EPFL, Lausanne, 2005.
  - [3] Y. S. Chauhan, “Compact modeling of high voltage MOSFETs,” EPFL, Lausanne, 2007.
- Articles
  - [4] C. Anghel et al., “New method for threshold voltage extraction of high-voltage MOSFETs based on gate-to-drain capacitance measurement,” Electron Device Letters, IEEE, vol. 27, no. 7, pp. 602-604, Jul. 2006.
  - [5] Y. S. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. J. Declercq, and A. M. Ionescu, “Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs,” IEEE Transactions on Electron Devices, v.54, n.6, pp.1527-1539, Jun. 2007
  - [6] N. Hefyene, J. M. Sallese, C. Anghel, A. M. Ionescu, S. F. Frere, and R. Gillon, “EKV Compact Model Extension for HV Lateral DMOS Transistors,” in *ASDAM 2002*, 2002.
  - [7] Y. S. Chauhan, R. Gillon, M. J. Declercq, and A. M. Ionescu, “Impact of Lateral Nonuniform Doping and Hot Carrier Injection on Capacitance Behavior of High Voltage MOSFETs,” IETE Technical Review, vol. 25, no. 5, pp. 244-250, 2008.
  - [8] Y. S. Chauhan et al., “Scalable general high voltage MOSFET model including quasi-saturation and self-heating effects,” Solid-State Electronics, vol. 50, no. 11-12, pp. 1801-1813, Nov. 2006.
  - [9] Y. S. Chauhan, R. Gillon, B. Bakeroot, F. Krummenacher, M. J. Declercq, and A. M. Ionescu, “An EKV-based high voltage MOSFET model with improved mobility and drift model,” Solid-State Electronics, vol.51, n.11-12, pp. 1581-1588, Nov. 2007

General outline of work

- Implementation of a HV-MOS compact model
- Verified the model against
  - new measurements from AMS
  - TCAD simulations
- Worked on Parameter Extraction Methodology
- Published the work
  - 1 Journal publication (DC model)
    - 1 more is currently under review (RF model)
  - 2 Workshops

Typical Structure of HV-MOS

- HV-MOS: 2 parts
  - Connection point: 'K'
  - Doping changes type
  - Between channel and drift
- Low-voltage part [1]
  - inner MOSFET
    - inner drain is 'K'
- High-voltage part [2]
  - Drift region
    - A physics-based model

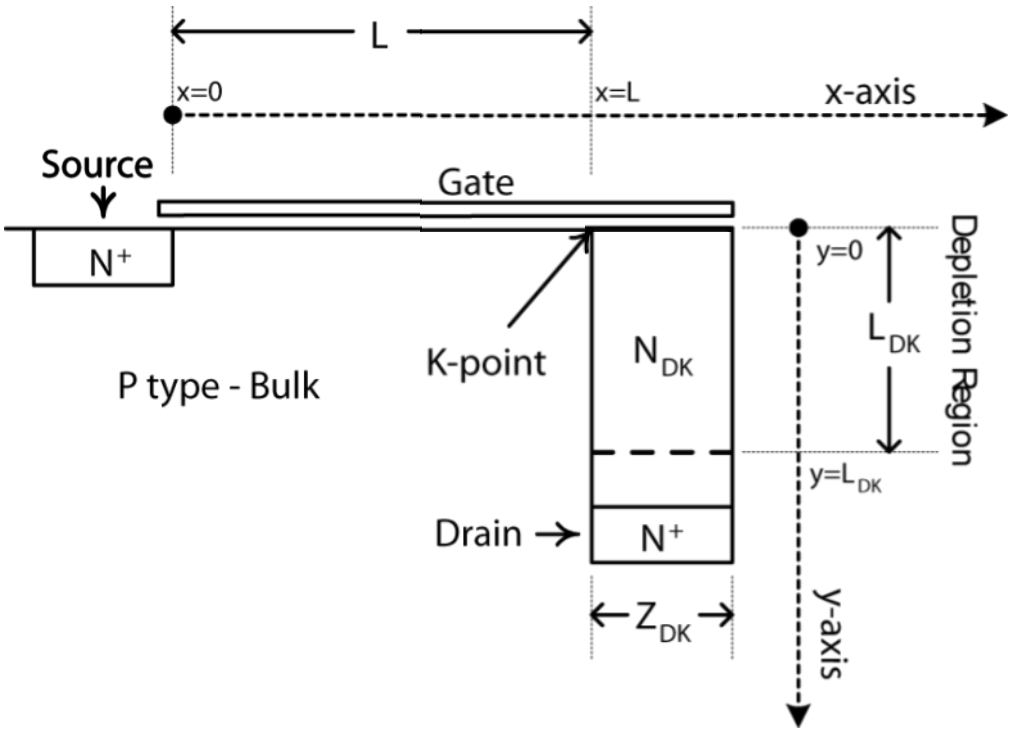


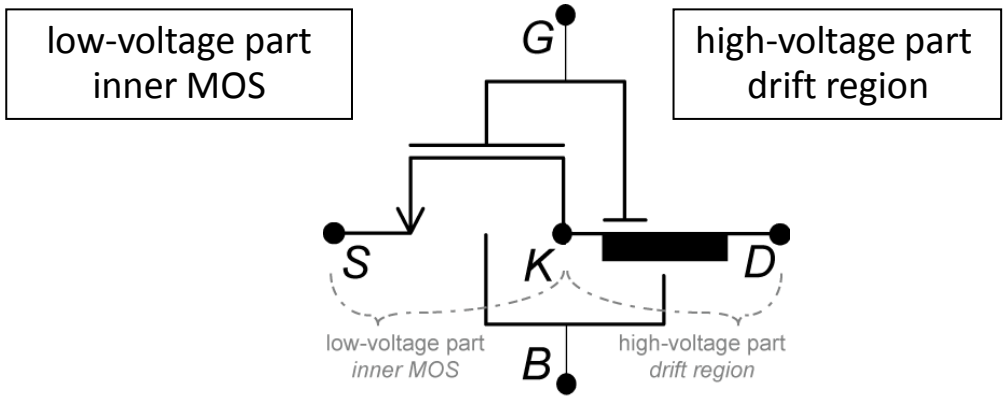
[1] Y. Chauhan, F. Krummenacher, R. Gillon, B. Bakeroot, M. Declercq, and A. Ionescu, "**Compact Modeling of Lateral Nonuniform Doping in High-Voltage MOSFETs**," Electron Devices, IEEE Transactions on, vol. 54, no. 6, pp. 1527–1539, June 2007.

[2] A. Bazigos, F. Krummenacher, J.-M. Sallese, M. Bucher, E. Seebacher, W. Posch, K. Molnár and M. Tang, "**A physics-based analytical compact model for the Drift region of the HV-MOSFET**" Electron Devices, IEEE Transactions on, Accepted for publication, doi: 10.1109/TED.2011.2119487

From “1×2D” to “2×1D”

- HV-MOS: 2D problem
  - Split into 2 axes
  - x-axis: inner MOS
    - Source to ‘K’
  - y-axis: DRIFT region
    - ‘K’ to Drain
- Simplified HV-MOS: two 1D problems
  - Solution possible





Parts of the macromodel

- Low-voltage part / inner MOS
  - any compact MOSFET model
    - Lateral Non-Uniform Doping
- High-voltage part / DRIFT region
  - A physics-based analytical compact model
    - Charge and potential analysis
      - Poisson's equation
      - Boltzmann's equation
      - drift-diffusion model

Low-voltage part: Inner MOS

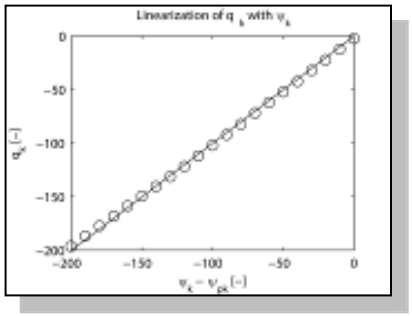
- Compact MOSFET model
  - Lateral Non-Uniform doping
  - Temperature dependence
    - Common temperature with DRIFT region
  - Self-heating effect
  - Second order mobility reduction due to vertical field
  - Geometry scaling
  - Velocity saturation
  - Channel length modulation
  - Subthreshold barrier lowering

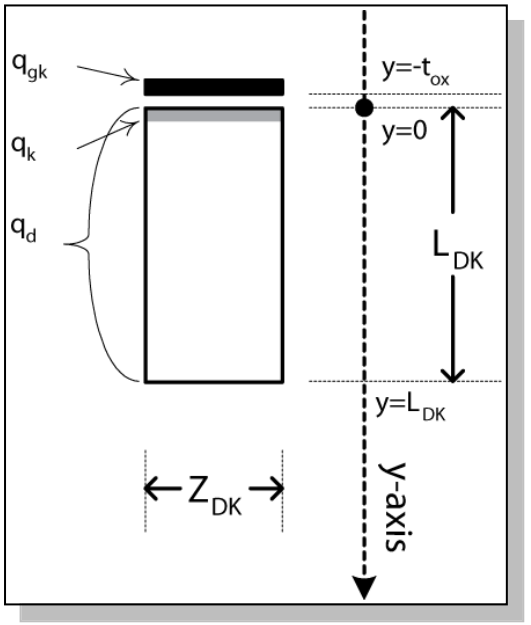
Key points of the DRIFT region model

- The electrostatic behaviour of the device depends on its current

$$\delta^2 \left(\varepsilon_d^2 - \varepsilon_k^2\right) = 1 - e^{\psi_k - v_{bi} - v_k} + i\left(1 + \frac{\psi_d - \psi_k}{\varepsilon_c}\right) - \left(\psi_d - \psi_k\right)$$

- The charge in DRIFT region (q_{dk}) is the sum of
  - q_d: Charge in depleted region
  - q_k: Charge sheet just below thin oxide
    - Linear relation with ψ_k
    - Always negative





Bottom line of the DRIFT region model

- Current is expressed as a function of
  - Drift region difference potential: V_{DK}
    - Mobility high field reduction model (1st order)
  - the average charge density of the DRIFT region
    - a function of V_{GK} and V_{DK}
    - Continuous expression
      - accumulation
      - depletion
  - denormalization factor

$$I_{DK} = I_{DK,0} \cdot \eta_{avg} \cdot \frac{v_d - v_k}{1 + \frac{v_d - v_k}{\varepsilon_c}}$$

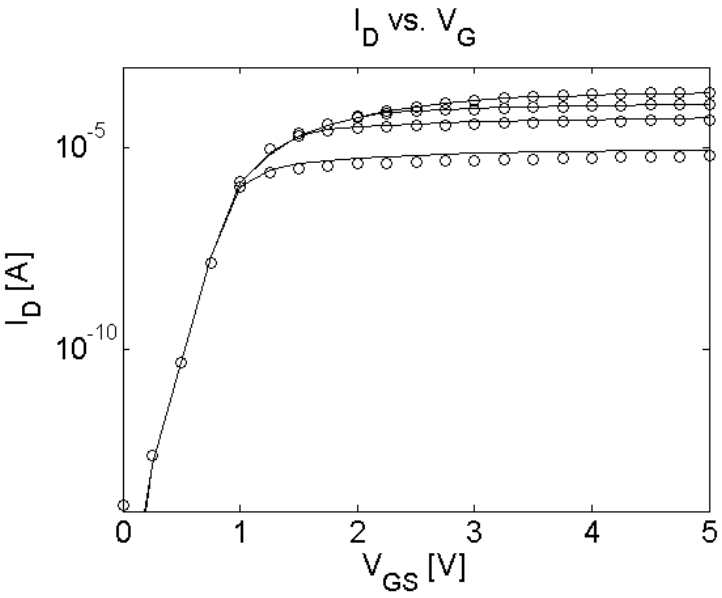
Higher order effects: DRIFT region

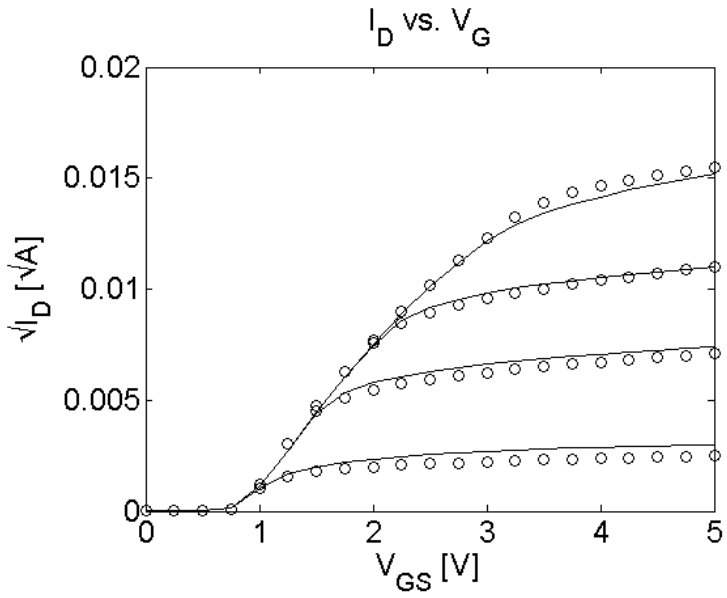
- Around the core model for DRIFT region
  - Temperature dependence
  - Self-heating effect
  - Quasi-saturation
  - Impact ionization current
  - …
  - … building up a full DRIFT region model

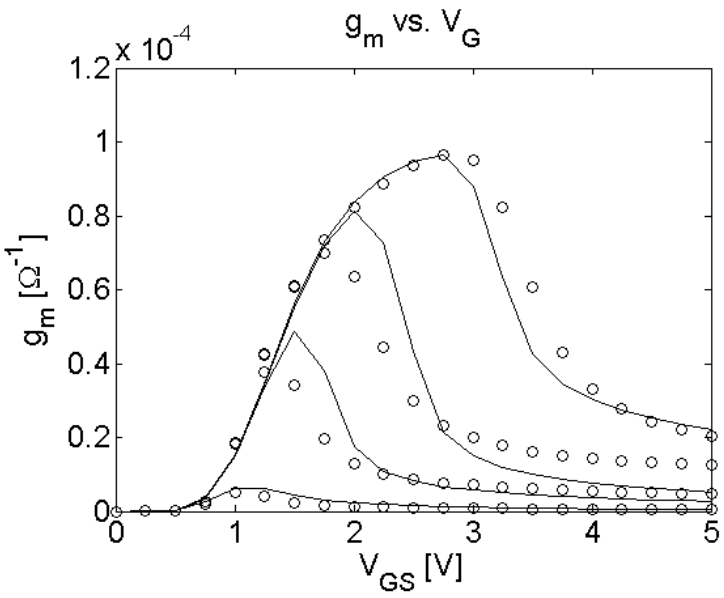
Numerical Simulations: I_D vs. V_G

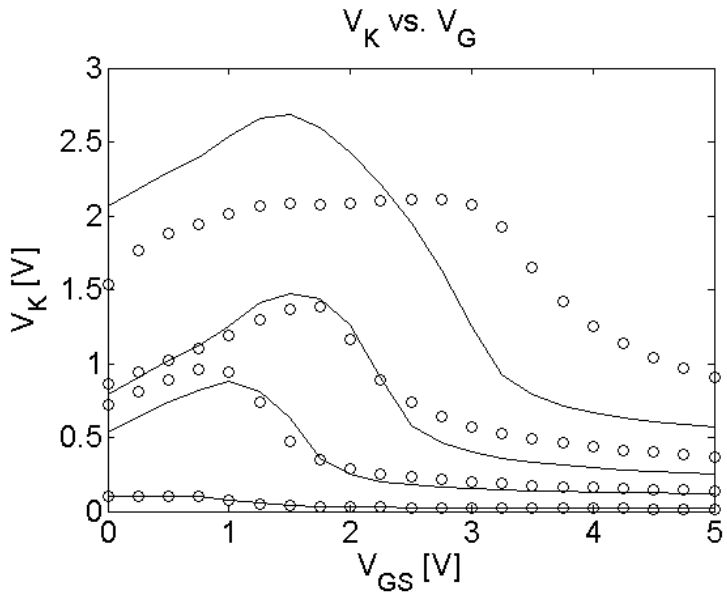
Device: LDMOS

L = 500nm
W = 1um
T_{ox} = 15nm
V_{DS} = {0.1, 1.0, 5.0, 70.0}V
V_{SB} = 0V





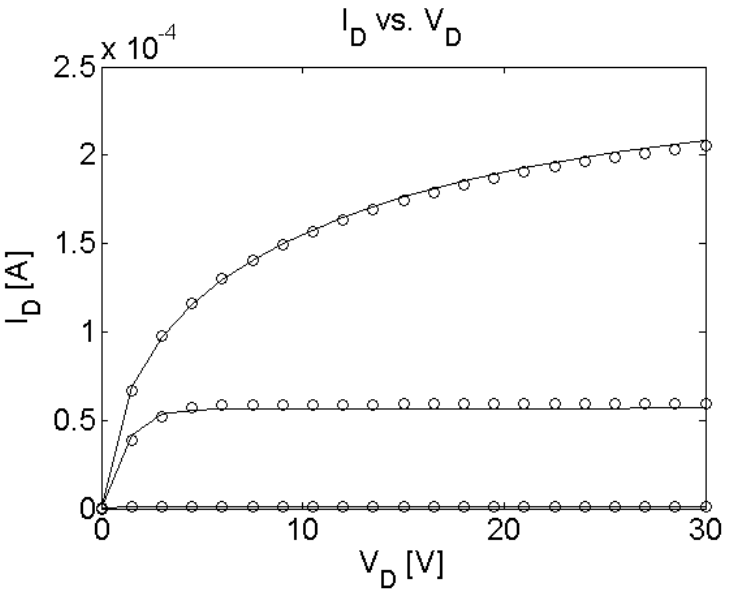


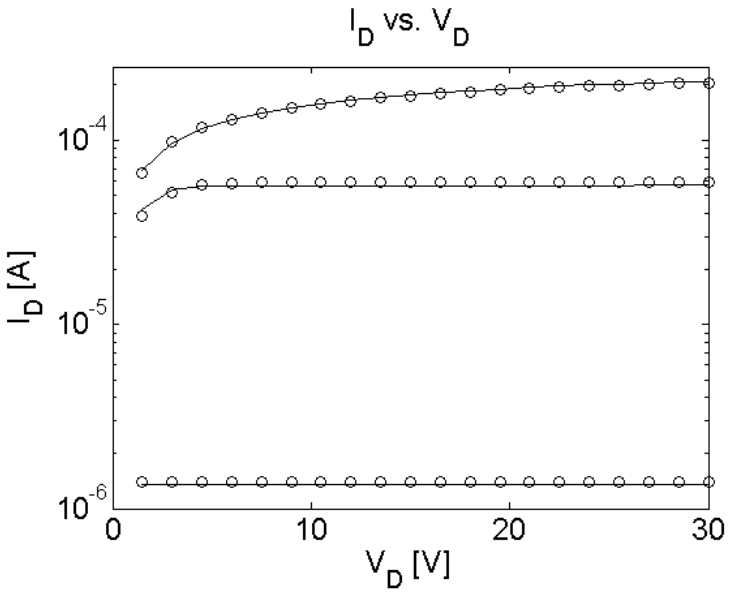


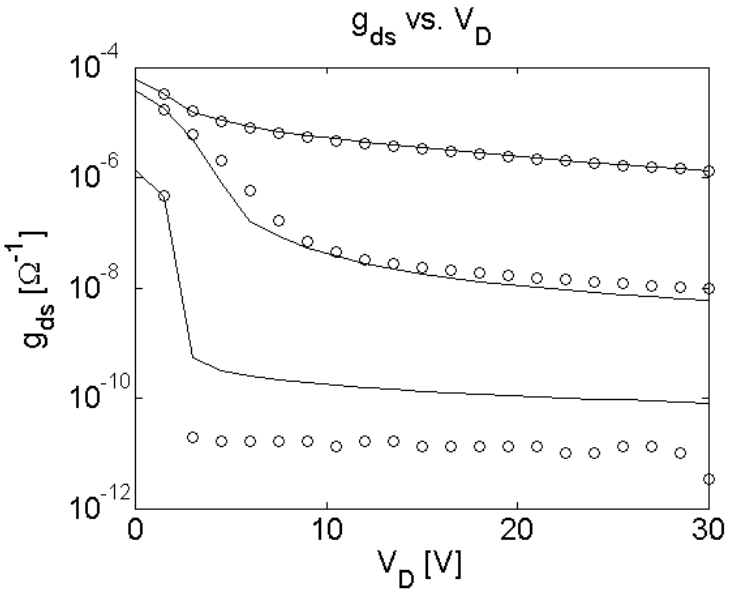
Numerical Simulations: I_D vs. V_D

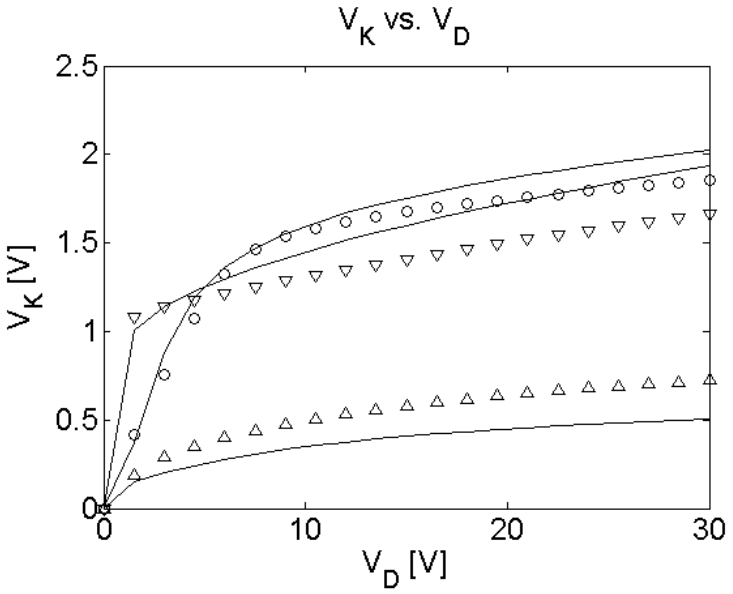
Device: LDMOS

L = 500nm
W = 1um
T_{ox} = 15nm
V_{GS} = {1.0, 2.0, 5.0}V
V_{SB} = 0V





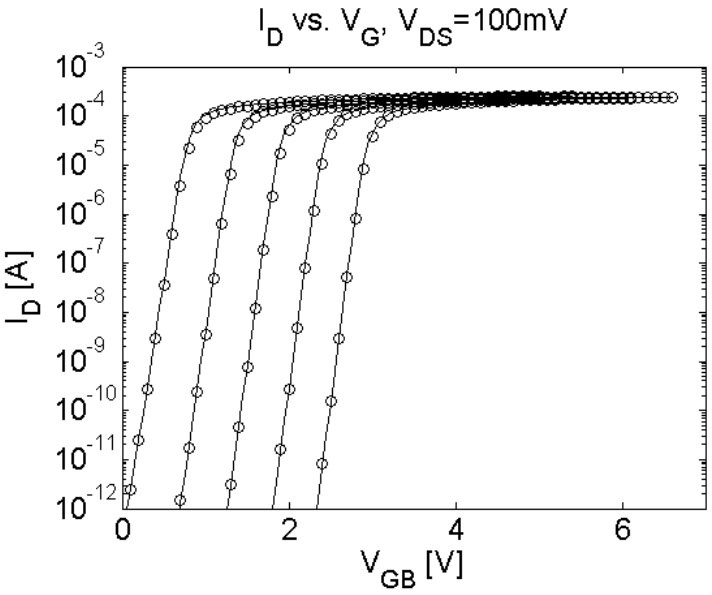


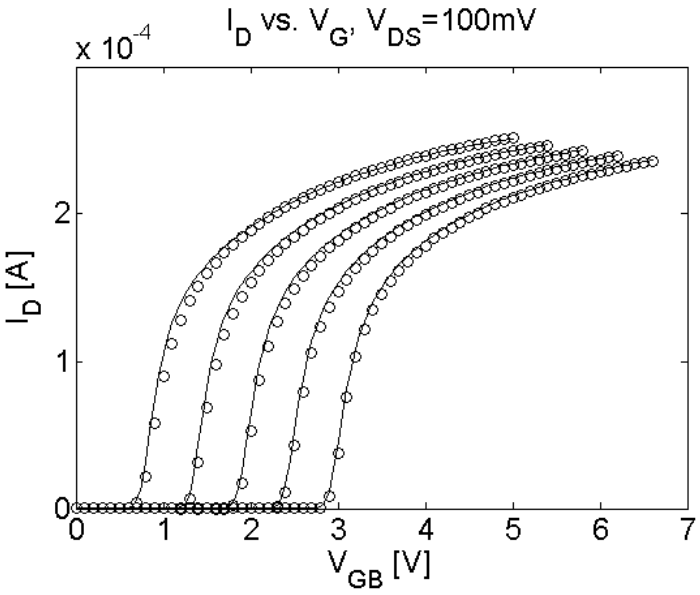


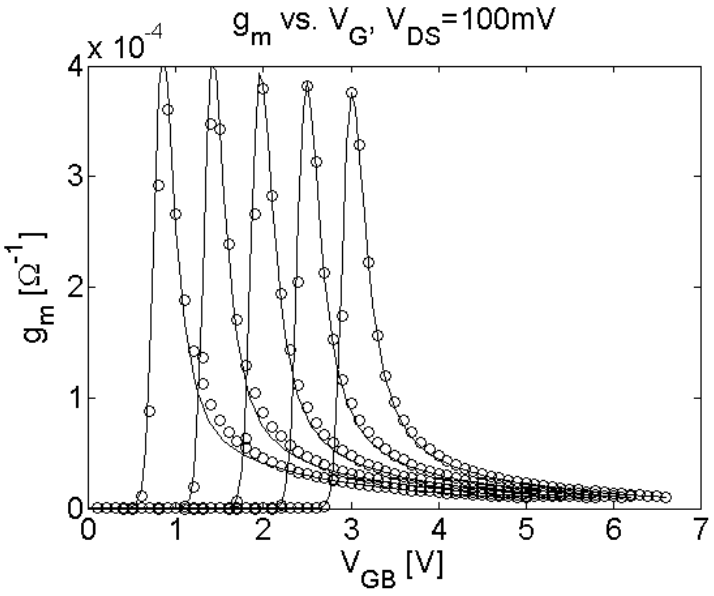
DC Measurements: I_D vs. V_G, V_{DS}=0.1V

Device: LDMOS

L = 400nm
W = 40um
T_{ox} = 15nm
V_{DS} = 100mV
V_{SB} = {0.0, 0.4, 0.8, 1.2, 1.6}V



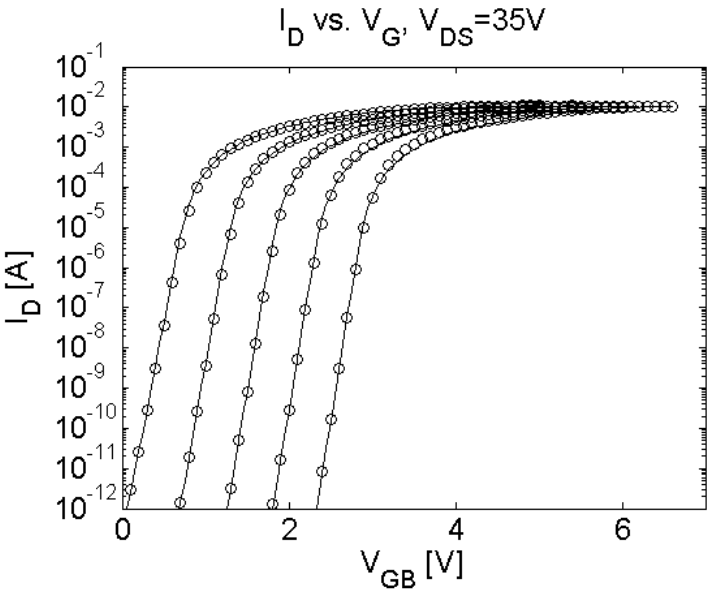


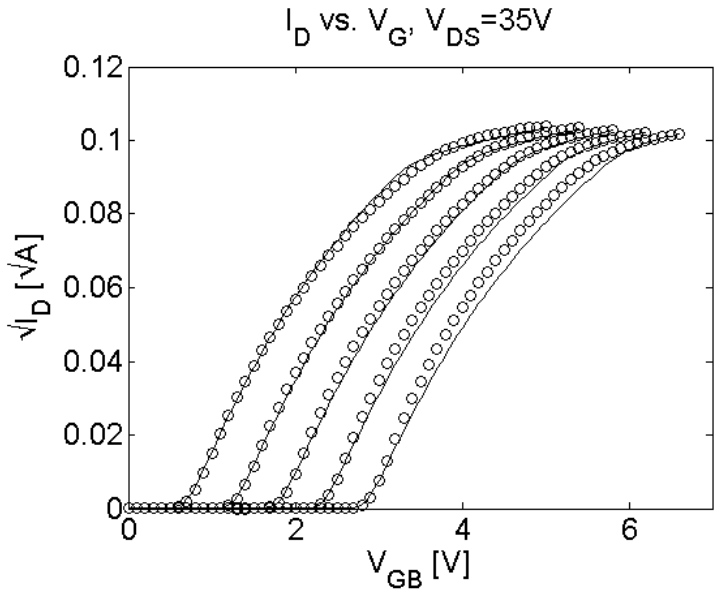


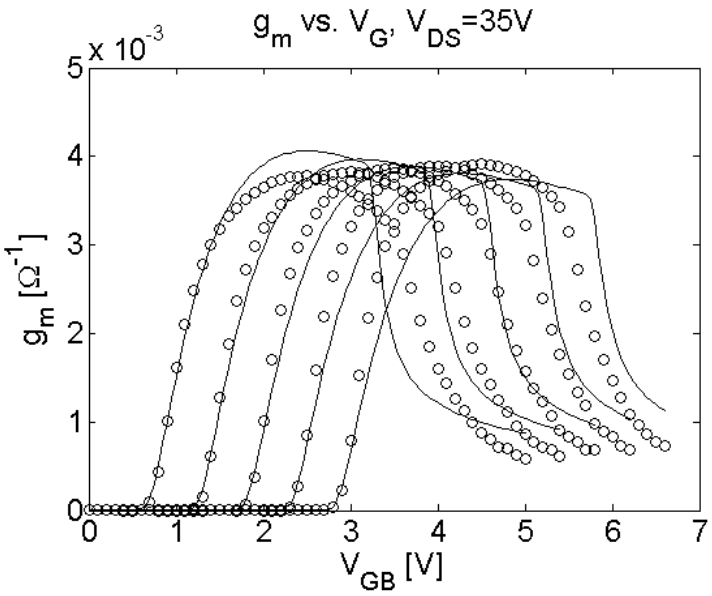
DC Measurements: I_D vs. V_G,V_{DS}=35V

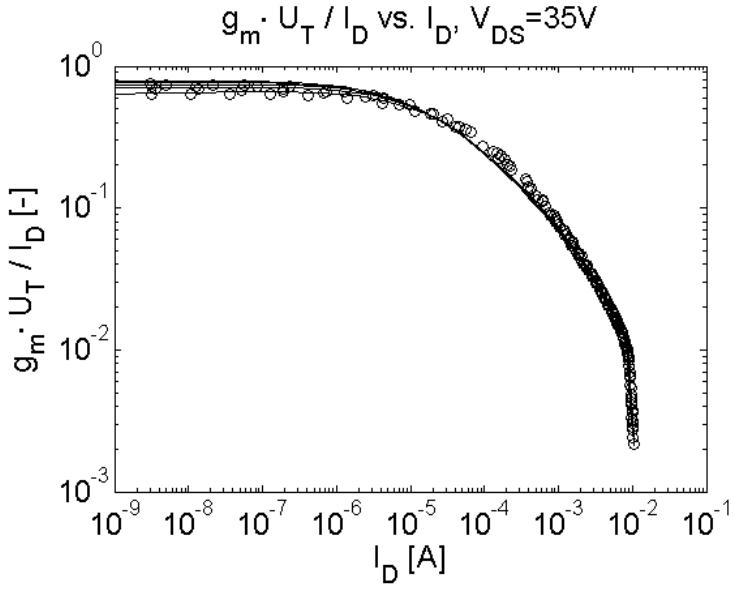
Device: LDMOS

L = 400nm
W = 40um
T_{ox} = 15nm
V_{DS} = 35V
V_{SB} = {0.0, 0.4, 0.8, 1.2, 1.6}V





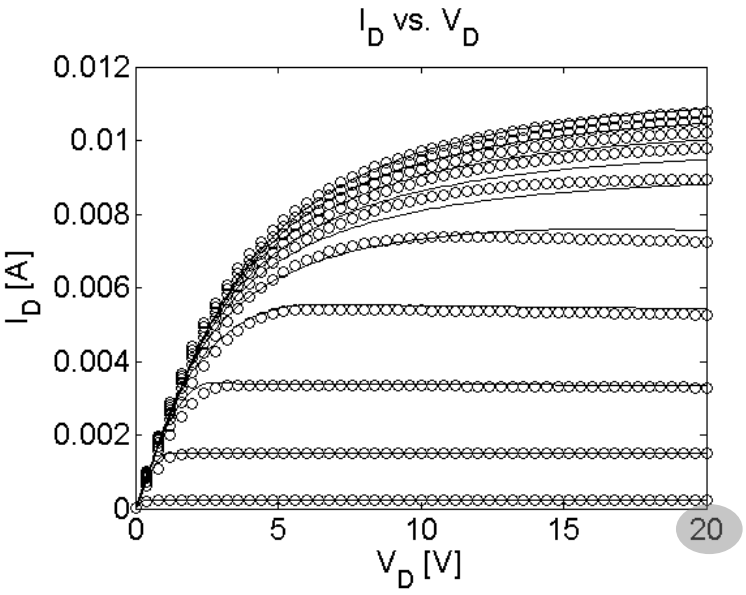


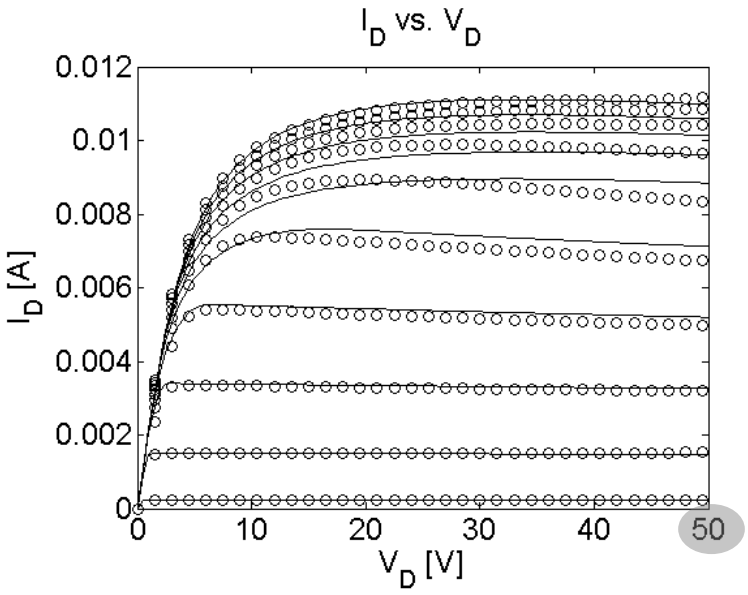


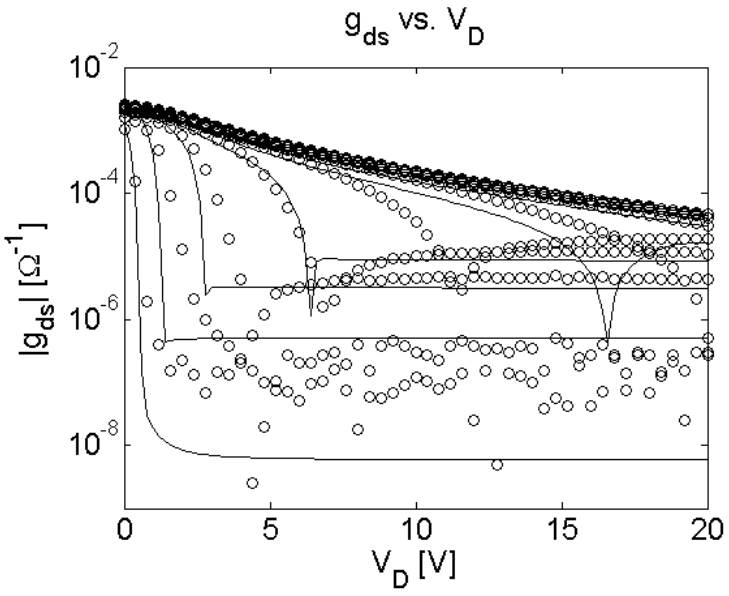
DC Measurements: I_D vs. V_D

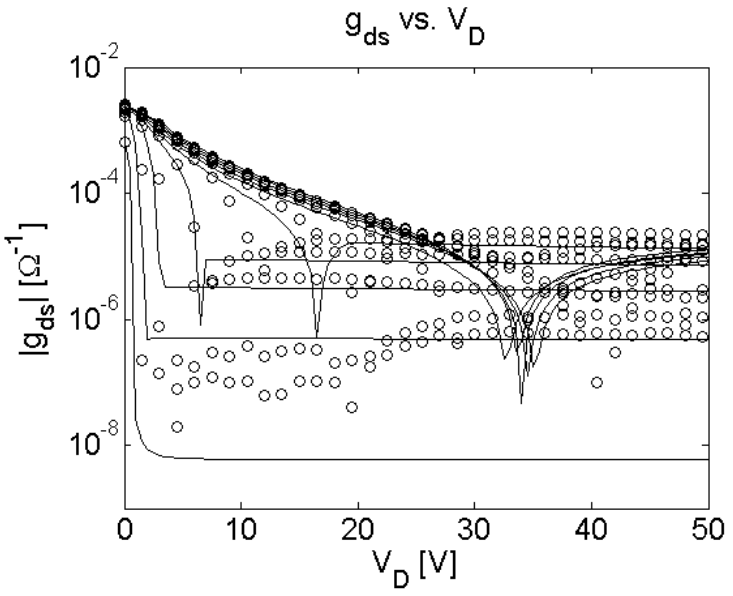
Device: LDMOS

L = 400nm
W = 40um
T_{ox} = 15nm
V_{GS} = {1.0, 1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5}V
V_{SB} = 0.0V









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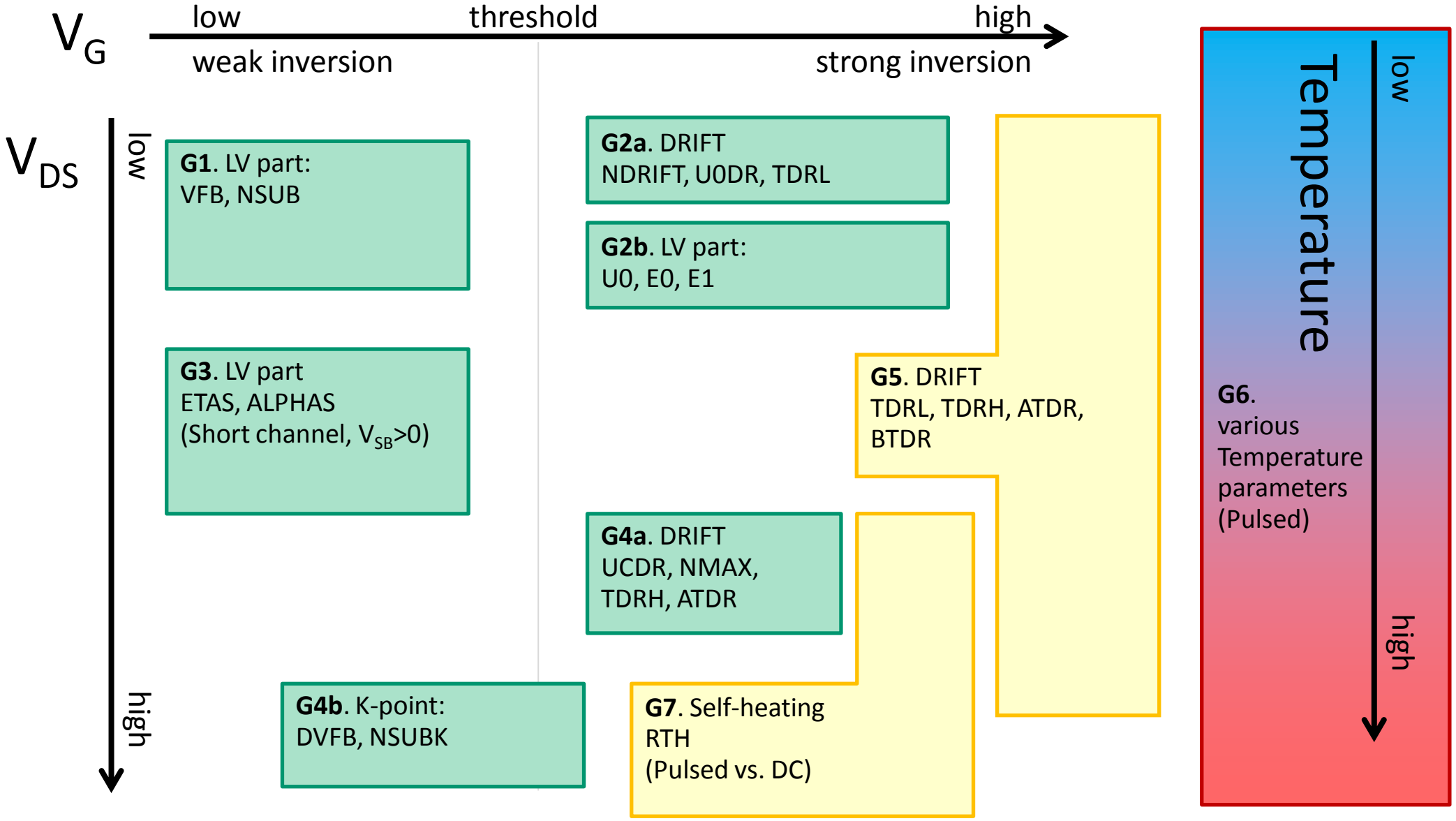
Parameter Extraction Guidelines



Parameter list (1/2)

Name	Value	Min	Max	Short Description / Notes	Unit
Instance Parameters					
W	$40 \cdot 10^{-6}$	0	∞	Drawn device Width (Width of gate region).	m
L	10^{-6}	0	∞	Drawn device Length (Length of gate region).	m
Flags and Setup Parameters					
TYPE	1	-1	1	Channel type selector, TYPE = +1 for NMOS, TYPE = -1 for PMOS.	-
SHNET	1	0	1	Internal Self-Heating network: SHNET = 0 for Self-Heating OFF, SHNET = 1 for Self-Heating ON.	-
				Low Voltage Part	
Main Physical and Electrical Parameters					
TOX	$50 \cdot 10^{-9}$	0	∞	Gate oxide thickness. If TOX = 0 then COX is used.	m
COX	$0.7 \cdot 10^{-3}$	0	∞	Gate oxide capacitance per unit area.	F/m^2
VFB	-1.1	-∞	∞	Flat-Band voltage at source end of channel. If VFB = -10^3 then VT0 is used.	V
VT0	0.8	-∞	∞	Zero-bias Threshold voltage.	V
NSUB	10^{17}	0	∞	Bulk doping concentration at source end of channel. If NSUB = 0 then GAMMA is used.	cm^{-3}
GAMMA	0.5	0	∞	Body effect factor at source side of channel.	$V^{1/2}$
PHIF	0	0	∞	Bulk Fermi potential at source end of channel. If PHIF = 0 then NSUB or GAMMA is used for the Fermi potential calculation.	V
DVFB	0	-∞	∞	Flat-Band voltage offset between source and drain end of channel. If DVFB = -10^3 then DVT is used, but then VT0 must also be used.	V
DVT0	0	-∞	∞	Threshold voltage offset between source and drain end of channel.	V
NSUBK	10^{17}	0	∞	Bulk doping concentration at drain end of channel (K-Point). If NSUBK = 0 then GAMMAK is used.	cm^{-3}
GAMMAK	0.5	0	∞	Body effect factor at drain end of channel (K-Point).	$V^{1/2}$
PHIFK	0	0	∞	Bulk Fermi potential at drain end of channel. If PHIFK = 0 then NSUBK or GAMMAK is used for the Fermi potential calculation.	V

Name	Value	Min	Max	Short Description / Notes	Unit
Mobility Parameters					
U0	600	0	∞	Low-field mobility. If U0 = 0 then KP is used.	cm^2/Vs
KP	0	0	∞	Low-field transconductance factor.	A/V^2
Mobility Reduction due to Vertical Field					
E0	$150 \cdot 10^6$	1	∞	1st-order mobility reduction characteristic field.	V/m
E1	$200 \cdot 10^6$	1	∞	2nd-order mobility reduction characteristic field.	V/m
ETA	0.6	0	1	Q_b vs. Q_i weight coefficient for the vertical field calculation.	-
Bias Dependence and Length Scaling of Equivalent Pinch-Off Voltage Gradient					
DGC1	0.25	0	1	Bulk doping gradient 1st-order inversion scaling coefficient.	-
DGC2	0	0	1	Bulk doping gradient 2nd-order inversion scaling coefficient.	-
DGE	0.5	0	1	Bulk doping gradient length scaling exponent.	-
Non-Uniform Doping Length Scaling Factor for Intermediate and Long Channel Devices					
LDG	10^{-6}	10^{-9}	∞	Bulk doping gradient characteristic length.	m
Geometrical Parameters (Short and Narrow Channel Corrections)					
DL	0	0	∞	Length offset of gate oxide region.	m
DW	0	0	∞	Width offset of gate oxide region.	m
DWD	0	0	∞	Width offset of drift region.	m
Reverse Short Channel Effect					
LR	$0.1 \cdot 10^{-6}$	0	∞	Reverse short channel characteristic length.	m
QLR	0	-∞	∞	Reverse short channel Threshold voltage coefficient.	C/m^2
NLR	0	-∞	∞	Reverse short channel body effect coefficient.	F/m^2
Subthreshold Barrier Lowering					
ETAS	0.5	0	2	Subthreshold barrier lowering characteristic length coefficient.	-
SIGMAS	0.1	0	2	Subthreshold barrier lowering body bias coefficient.	-
ALPHAS	1	0	5	Subthreshold barrier lowering smoothing coefficient.	-
BETAS	0.1	0	1	Subthreshold barrier lowering scaling factor.	-
Velocity Saturation					
VSAT	0	0	∞	Saturation velocity. If VSAT = 0 then UCRIT is used.	m/s
UCRIT	$3 \cdot 10^{-6}$	1	∞	Longitudinal critical field.	V/m
Channel Length Modulation					
LAMBDA	0	0	∞	Lambda factor for channel length modulation.	-
LC	$30 \cdot 10^{-9}$	0	∞	Characteristic length for channel length modulation.	m

Parameter list (2/2)

Name	Value	Min	Max	Short Description / Notes	Unit
				Drift Region	
Geometrical Parameters					
LDR	$4 \cdot 10^{-6}$	0	∞	Length of depleted drift region.	m
TDRL	$0.8 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at low V_{DS}.	m
TDRH	$0.5 \cdot 10^{-6}$	0	∞	Current flow thickness in drift region at high V_{DS}.	m
TDRLS	0	-∞	∞	Low V_{DS} body bias sensitivity of drift current flow thickness.	1/V
TDRHS	0	-∞	∞	High V_{DS} body bias sensitivity of drift current flow thickness.	1/V
Gate Overlap Length Over The Drift Region (used in AC behaviour)					
LOVD	0	0	∞	Thin oxide gate extension over drift region.	m
Charge-Sheet Accumulation Layer Thickness (used in AC behaviour)					
DACC	$20 \cdot 10^{-9}$	10^{-9}	LDR	Charge-sheet accumulation layer thickness.	m
Main Physical and Electrical Parameters					
NDRIFT	$5 \cdot 10^{16}$	0	∞	Drift region doping concentration. If NDRIFT = 0 then GAMMAD is used.	cm^{-3}
GAMMAD	0	0	∞	Drift region modulation factor.	$V^{1/2}$
PHIFD	0	0	∞	Drift region Fermi potential. If PHIFD = 0 then NDRIFT or GAMMAD is used for the Fermi Potential calculation.	V
Mobility Parameters					
U0DR	600	0	∞	Drift region low-field mobility. If U0DR = 0 then KPDR is used.	cm^2/Vs
KPDR	0	0	∞	Drift region low-field transconductance factor.	A/V^2
Velocity Saturation					
VSATDR	0	0	∞	Saturation velocity in drift. If VSATDR = 0 then UCDR is used.	m/s
UCDR	$3 \cdot 10^6$	1.0	∞	Longitudinal critical field in drift region.	V/m
Quasi-Saturation					
ATDR	1	0	∞	Quasi-saturation smoothing factor.	-
BTDR	0.3	0	∞	Quasi-saturation fine-tuning coefficient.	-
Maximum Doping at the Drain Side					
NMAX	10	0	∞	Maximum relative carrier concentration in the drift.	-

Name	Value	Min	Max	Short Description / Notes	Unit
Impact Ionization Current					
IBA	0	0	∞	First impact ionization coefficient.	1/m
IBB	$50 \cdot 10^6$	10^6	∞	Second impact ionization coefficient.	V/m
IBN	1	0	∞	Saturation voltage factor for impact ionization.	-
IBH1	1	0	∞	High-current roll-off factor for impact ionization.	-
IBH2	1	0	∞	High-current roll-off exponent for impact ionization.	-
Self-Heating					
RTH	0	0	∞	Thermal resistance at zero injected power.	°C/W
CTH	0	0	∞	Thermal capacitance.	s·W/°C
Temperature Parameters					
TNOM	27	-273.15	∞	Reference temperature.	°C
TCVT0	0	-∞	:∞	Temperature coefficient of threshold voltage (VT0).	V/°C
TCDVT0	0	-∞	∞	Temperature coefficient of threshold voltage offset between source and drain end of channel (DVT0).	V/°C
TCVFB	0	-∞	∞	Temperature coefficient of Flat-Band Voltage (VFB).	V/°C
TCDVFB	0	-∞	∞	Temperature coefficient of Flat-Band Voltage offset between source and drain end of channel (DVFB).	V/°C
TCRTH	0	-1	1	Temperature coefficient of RTH.	$°C^{-1}$
BEX	-1.5	-∞	∞	Mobility temperature exponent (U0).	-
BDREX	-1.5	-∞	∞	Drift region mobility temperature exponent (U0DR).	-
UCEX	1.5	-∞	∞	Longitudinal critical field temperature exponent (UCRIT).	-
UCDREX	1	-∞	∞	Drift region longitudinal critical field temperature exponent (UCDR).	-
E0EX	0	-∞	∞	Temperature exponent for E0.	-
E1EX	0	-∞	∞	Temperature exponent for E1.	-
TCNMAX	0	-1	1	Temperature coefficient of NMAX.	$°C^{-1}$
TCETAS	0	-1	1	Temperature coefficient of ETAS.	$°C^{-1}$
TCTDRL	0	-1	1	Temperature coefficient of TDRL.	$°C^{-1}$
TCTDRH	0	-1	1	Temperature coefficient of TDRH.	$°C^{-1}$
TCATDR	0	-1	1	Temperature coefficient of ATDR.	$°C^{-1}$
TCBTDR	0	-1	1	Temperature coefficient of BTDR.	$°C^{-1}$
IBBT	0	-1	1	Temperature coefficient of IBB.	$°C^{-1}$

Implementation of the HV-MOS model

- Verilog-A code
  - Current Version: 1.105 (07 June 2011)
    - Version 1.101 (25 May 2010), Version 1.100 (23 April 2010)
  - Hierarchical structure
    - 1 main file (~1000 lines)
    - 9 called-in include files (~2000 lines)
      - variables, parameters, helping and debugging functions
  - Documentation (draft) available for v1.105 (25 July 2011)
    - Parameter extraction general guidelines

One code for Two parts

- The code covers the whole HV-MOS device
  - Inner MOS / DRIFT region / Internal node ‘K’
  - Simplicity
  - Many things in common
  - Reader friendly: Seeing both parts in parallel
  - Single device with 2 parts
    - go together like a horse and carriage
    - Not 2 devices connected

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