High-Level Description of Thermodynamical Effects in the EKV 2.6 MOST Model

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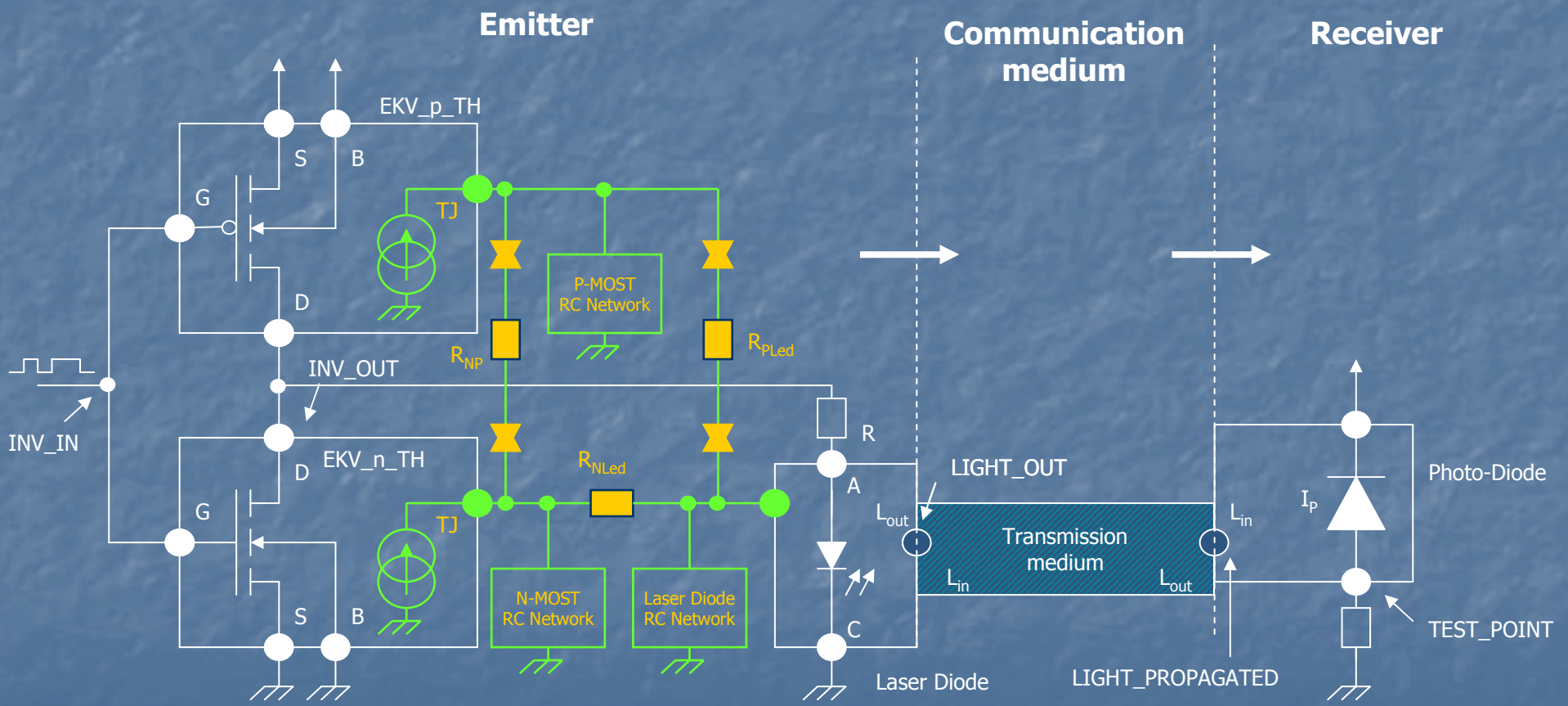
Presentation overview

- The studied transmission scheme
- One scheme, two HDLs
- Other studies on the EKV MOST Model v2.6
- Results & Ongoing researches

The transmission scheme



Mixed-Signal Model Structure

- Reference to predefined/previously defined submodels
- Declaration of the model interface
  - Generic parameters
  - Interface connection ports
- Declaration of the model contents
  - Declaration of objects used internally
  - Description of the model contents
    - Continuous (Analog) Behavior
    - Discrete (Digital) Behavior
    - Structural Description (instantiation)
  - Synchronization facilities

A model template

entity *name* **is**
model Interface
end entity name**;**

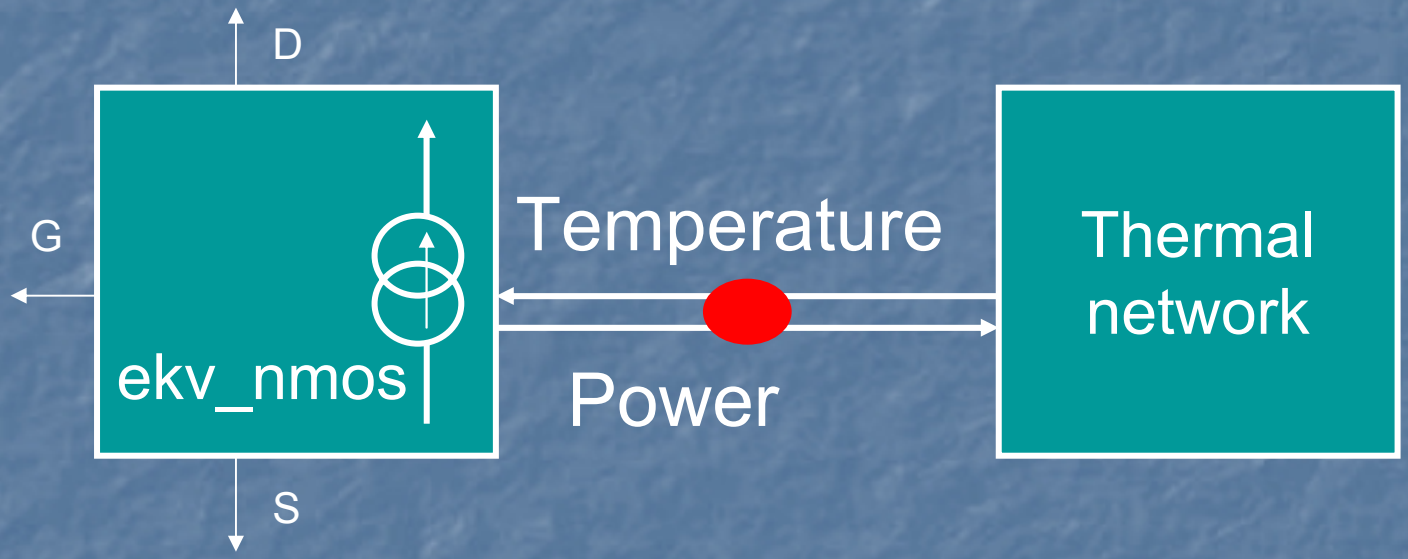
architecture equ **of** *name* **is**
model Contents
end architecture *name***;**

VHDL-AMS

module *name*
model Interface
model Contents
endmodule

Verilog-AMS

Thermo-electrical interaction



Introducing a new node, of « thermal » type in the EKV transistor interface

The two interfaces

```
❶ library disciplines;
use disciplines.electromagnetic_system.all;
use disciplines.thermal_system.all;
library ieee;
use ieee.math_real.all;

entity EKV_n_TH is
❷  generic
 (
 Weff : real := 1.5e-6;  -- channel width
 Leff : real := 0.15e-6; -- channel length
 PHI : real := 0.97; -- bulk Fermi potential
 GAMMA : real := 0.71; -- substrate factor
 KP : real := 453.0e-6; -- transconductance factor
 THETA : real := 50.0e-3; -- Mobility reduction
 VTO : real := 0.4; --long channel threshold volt.
 TCV : real := 1.5e-3; -- temperature coeff. (VTO)
 BEX : real := -1.5 -- temperature coeff.
);

❸  port (terminal d,g,s,b: electrical;
   terminal j:thermal);

end;
```

```
❶ `include "disciplines.h"

❷  module EKV_n_TH(d,g,s,b,tj);
// Node definitions (external nodes)
inout d,g,s,b,j ;
electrical d,g,s,b ;
thermal tj ;

//*** model parameter definitions
❷ parameter real boltz = 1.3806226E-23;
parameter real charge = 1.6021918E-19;
parameter real reftemp = 300.0;
//**    geometrical parameters
parameter real weff = 100.0E-6;
parameter real leff = 100.0E-6;
//*** Threshold voltage and substrate effect
//**   parameters (long-n_channel)
parameter real vto = 0.6;
parameter real gamma = 0.7;
parameter real phi = 0.5;
//*** Mobility parameters (long-channel)
parameter real kp = 20.0E-6;
parameter real theta = 50.0E-3;
//*** Temperature coefficients
parameter real tcv = 1.5E-3;
parameter real bex = -1.5;
```

Description of the model contents

- The description is achieved by use of Kirchhoff laws
- Kirchhoff laws imply energy conservation rules on **nodes**
- A **node** is associated to a **discipline** (electrical, thermal, ...)
- A **discipline** is characterized by two variables :
  - potential/across
  - flow/through
- Means to access these variables are necessary

Access to conservative variables in the EKV transistor model

VHDL-AMS

```
❶  port (terminal d,g,s,b: electrical;
    terminal j:thermal);
end;
architecture equ of ekvn is
❸  quantity vg across g to b;
 quantity vd across d to b;
 quantity vs across s to b;
 quantity id through d;
 quantity isource through s;
 quantity gpower through thermal_ground to j;
 quantity temp across j to thermal_ground;
…
 id==(ispec*(iff-ir));
   isource == -id;
   gpower == abs(id * (vd-vs));
```

Free and bound quantities.
Declare once,
Implicit reference when used

Verilog-AMS

- Access function in the ODAE
- Electrical : I() flow, V() potential
  Thermal : Pwr() flow, Temp() potential
- Access functions **scattered** throughout the code of analog behavior
- Importance of the contribution operator <+

```
❸ analog begin // EKV v2.6 long-channel
  vg = V(g,b);
  vs = V(s,b);
  vd = V(d,b);

 konq =boltz/charge;
  vt = konq * Temp(j) + 1.0E-20;
…
❹   I(d) <+ id;
    Pwr(j) <+ abs(id * (vd-vs));
end // analog
endmodule
```

Continuous Behavior Statement

Simple simultaneous Statement

Vs

Analog block

VHDL-AMS	Verilog-AMS

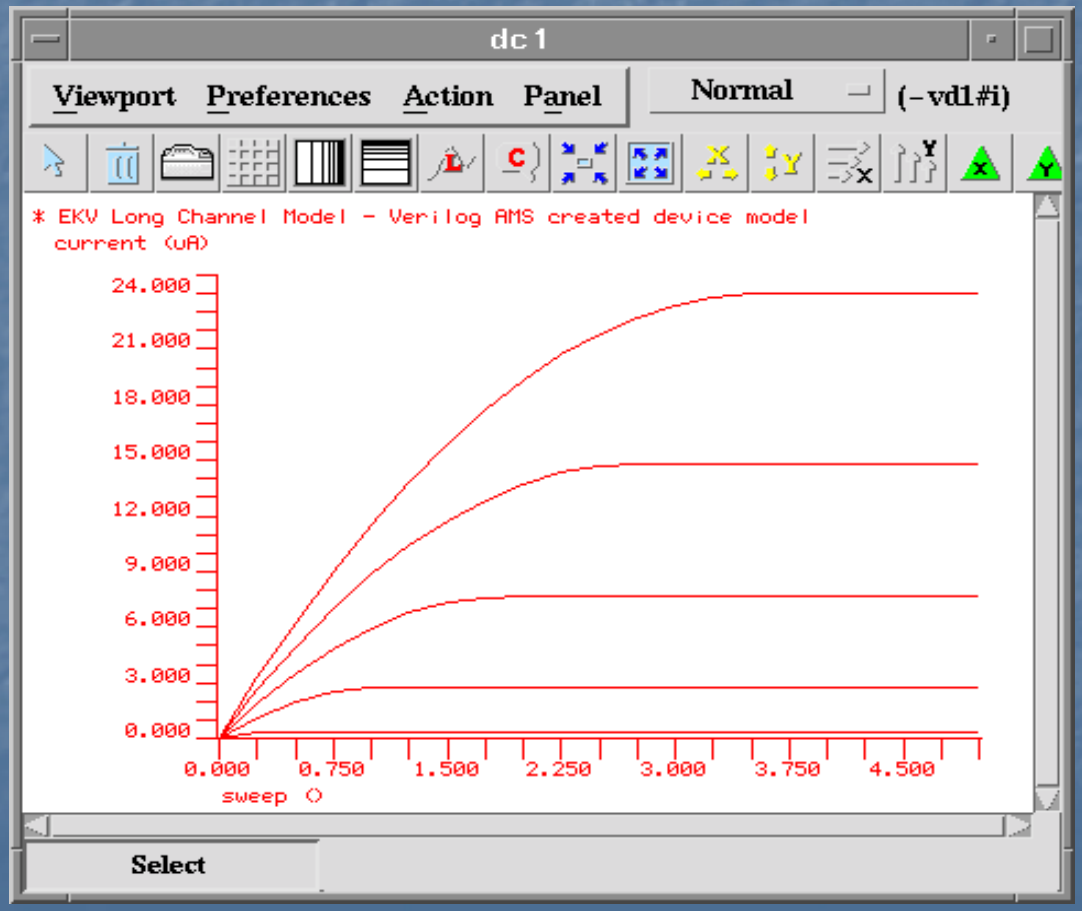
begin
  …
  exp1 == exp2 ;
  …
end;
	analog block
	  begin
	  var1 = f(exp1,exp2);
	  res <+ var1;
	  end;

if exp then use
  exp1 == exp2 ;
else
  exp1 == exp3 ;
end if;
	analog block
	  begin
	  if (exp)
	  var1 = f(exp1,exp2);
	  else
	  var1 = f(exp1,exp3);
	  res <+ var1;
	  end;

procedural
  begin
  …
  end;
	analog block
	  …
	end;

Id(Vd) Characteristic plot

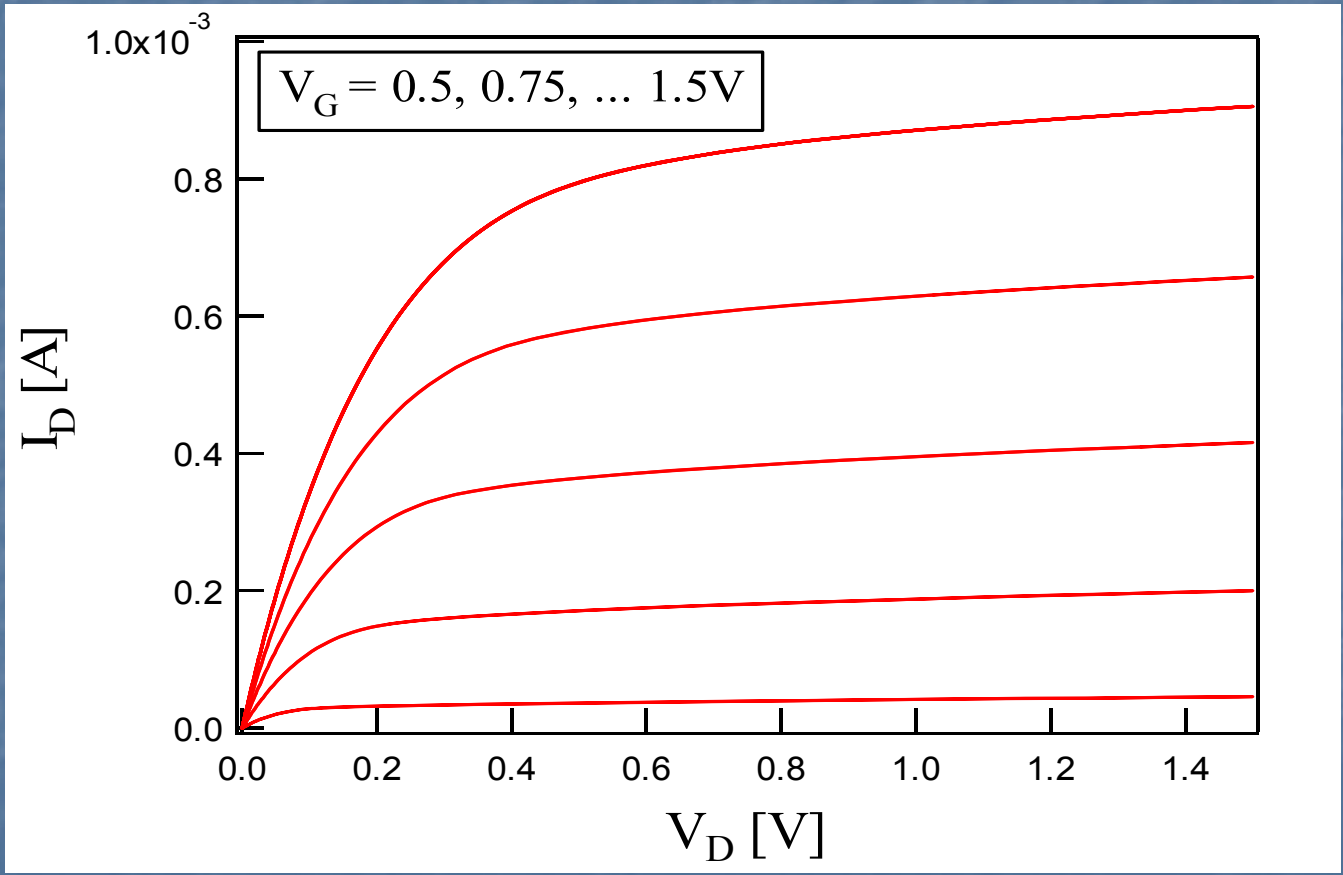
For a long channel



Without thermal effects

Verilog-AMS

Id(Vd) Characteristic plot

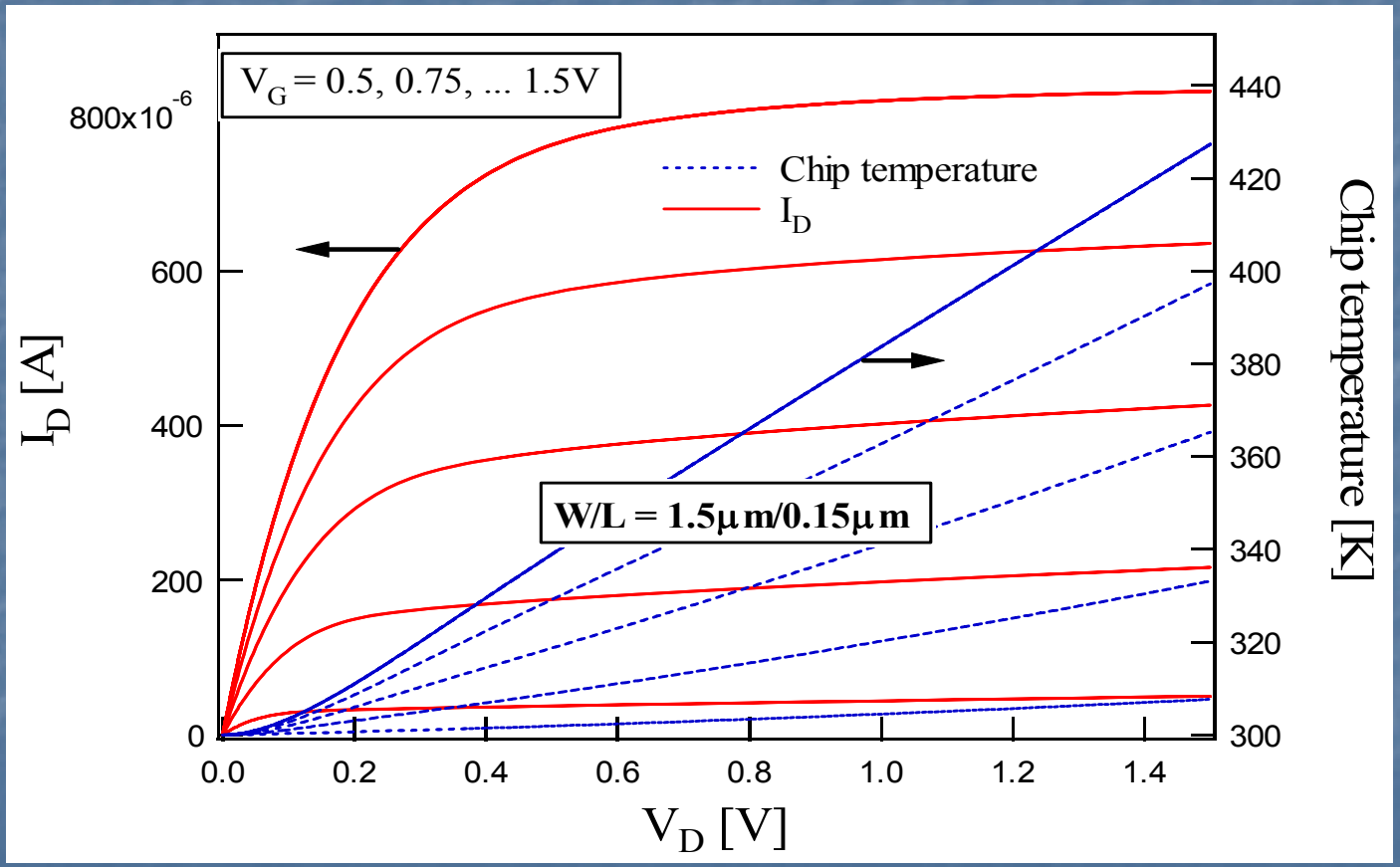


W/L = 1.5μm/0.15μm

Without thermal effects

VHDL-AMS

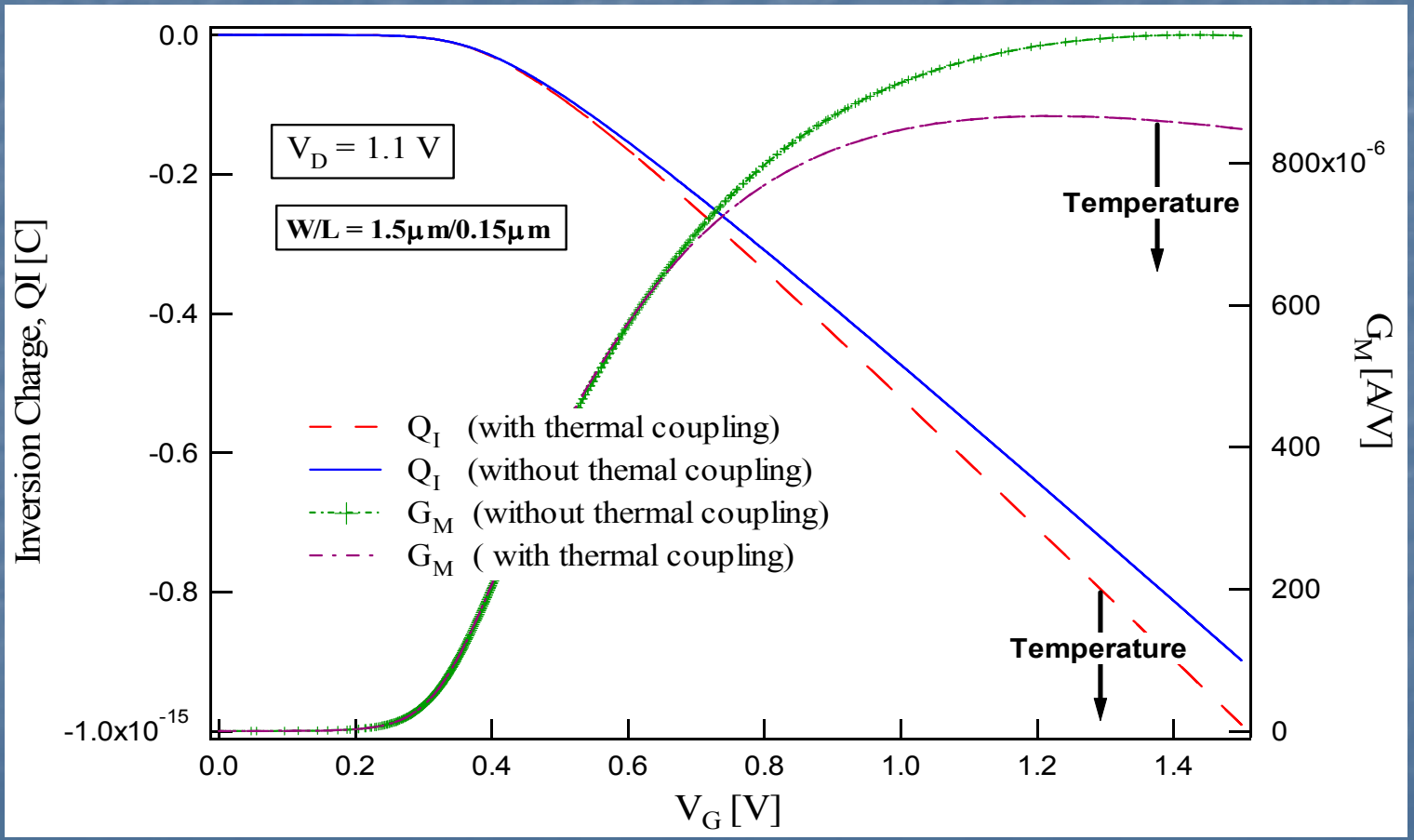
Thermal-electronic effects in action: downgrading of I_D - V_D characteristic



With thermal effects

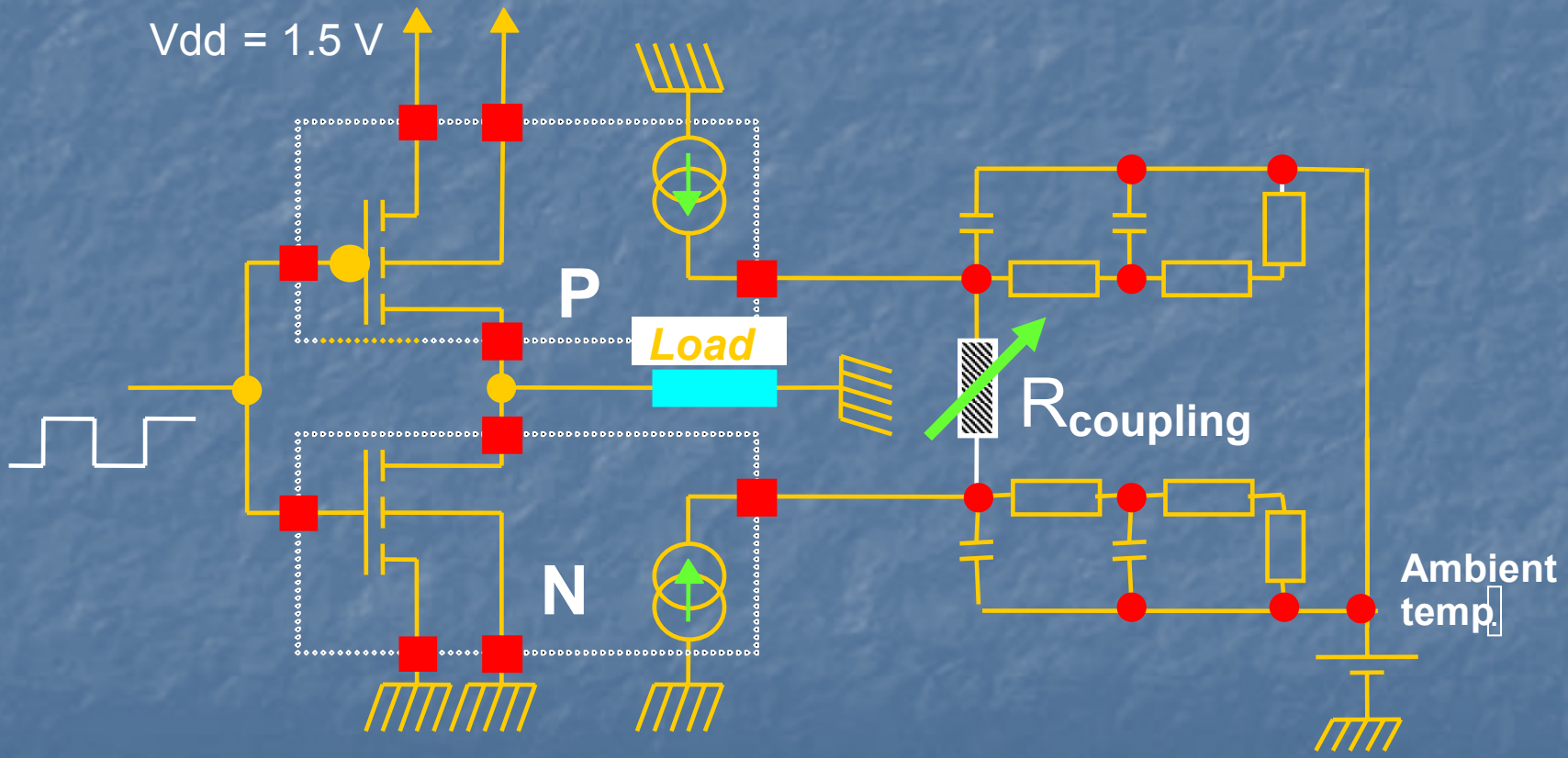
VHDL-AMS

Thermal-electronic effects in action: downgrading of Q_I/G_M - V_G characteristics

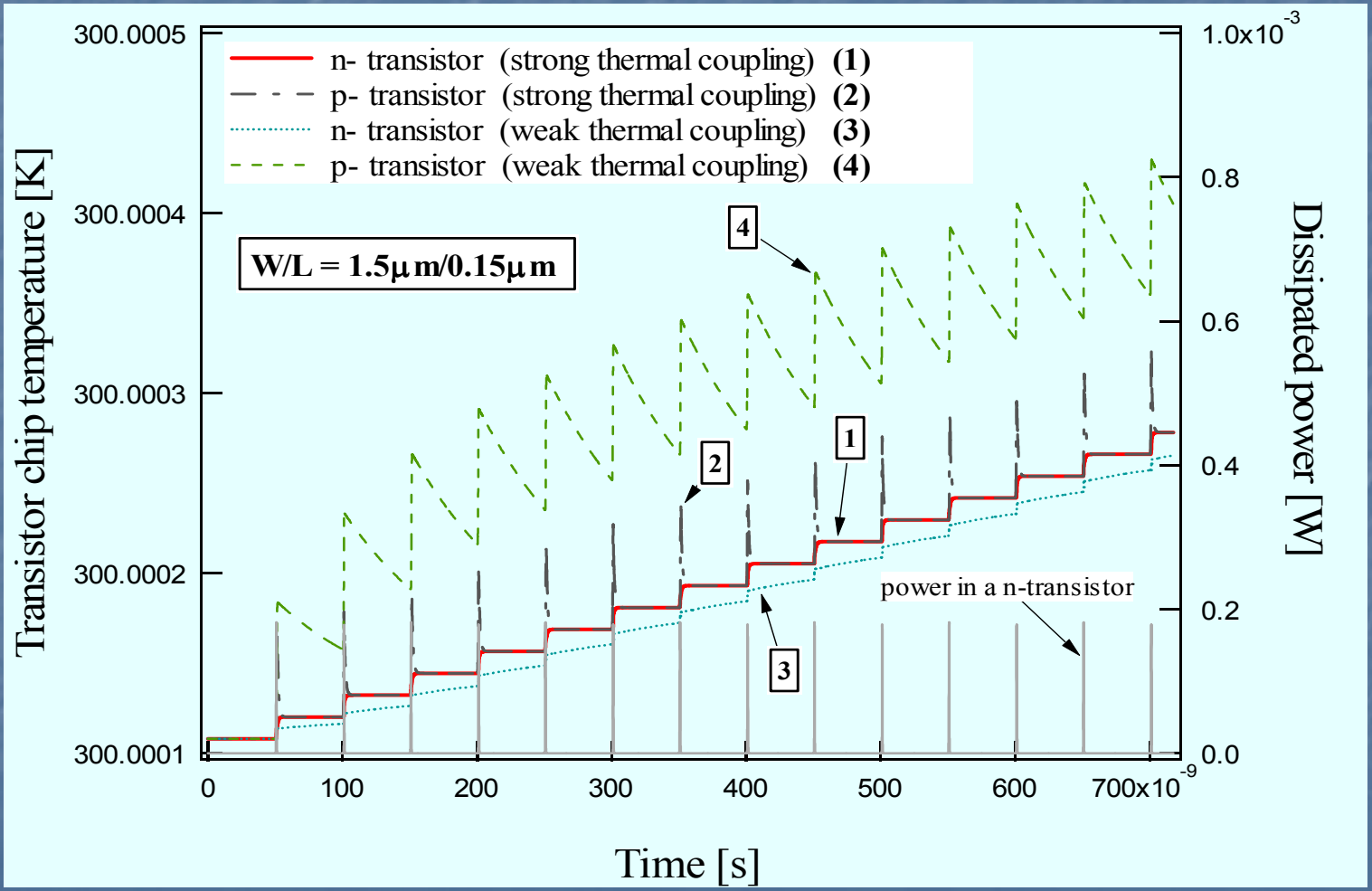


VHDL-AMS

Thermal coupling between the nMOST and the pMOST for different values of coupling

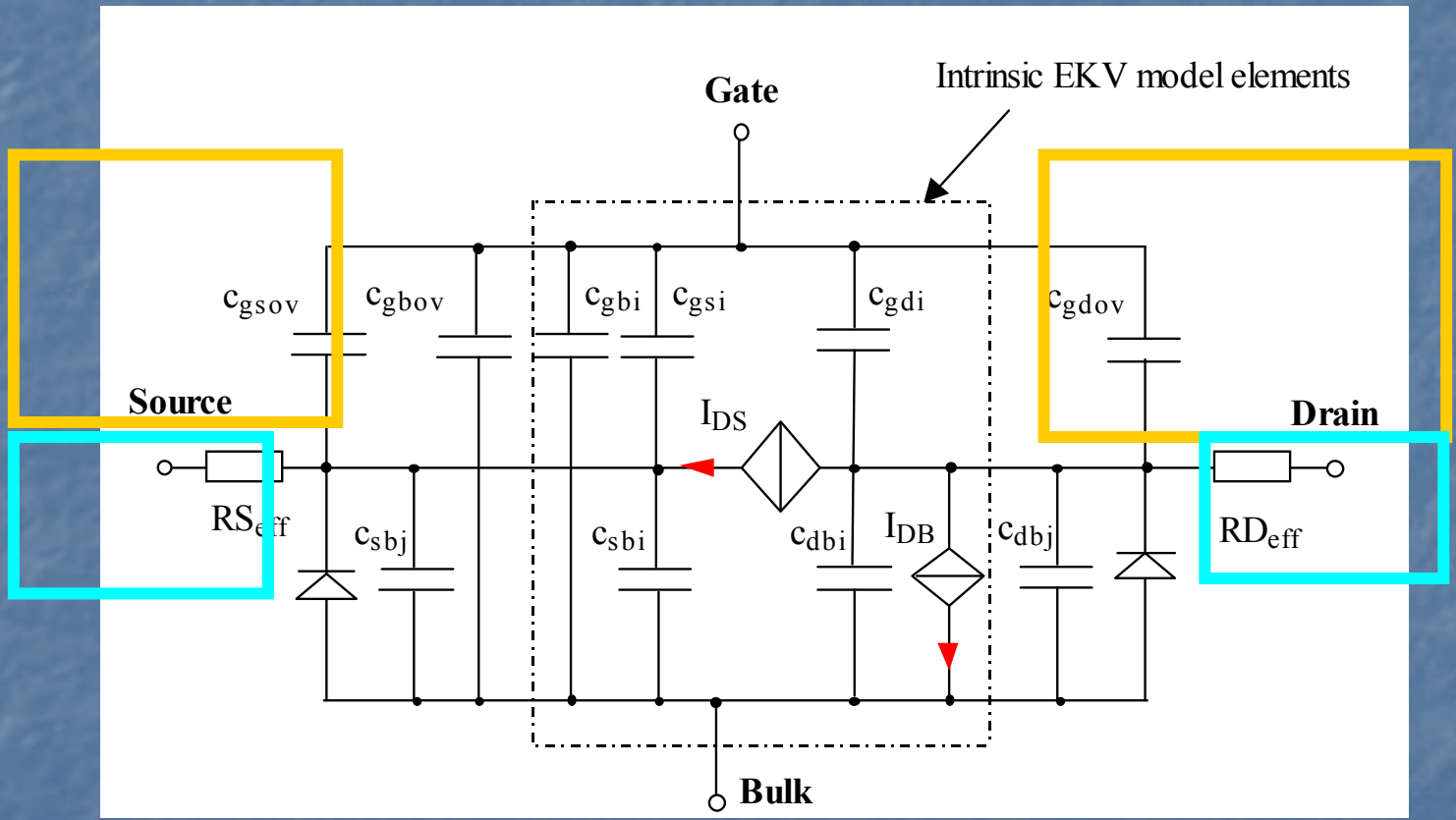


Simulation results

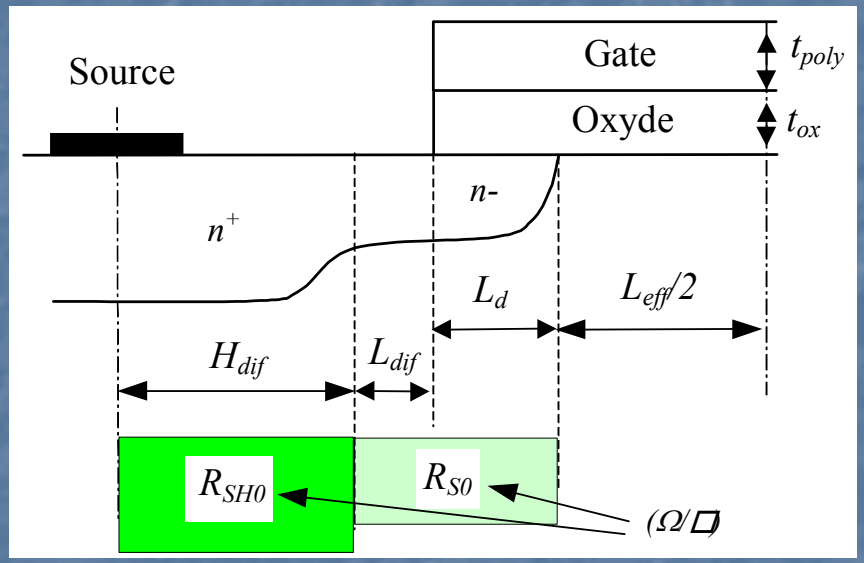


VHDL-AMS

Others studies on the EKV MOST Model v2.6

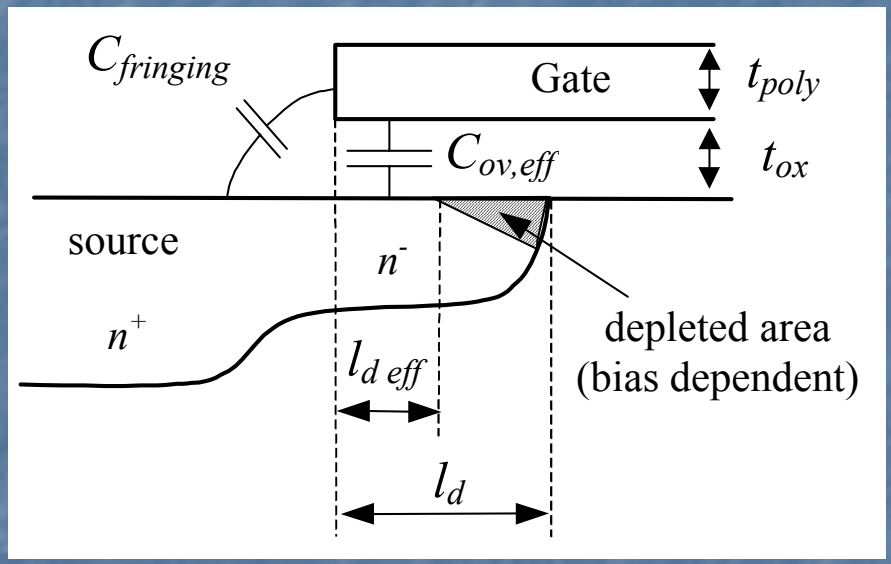


Taking Deep submicron effects into account (extrinsic aspects)



Resistances

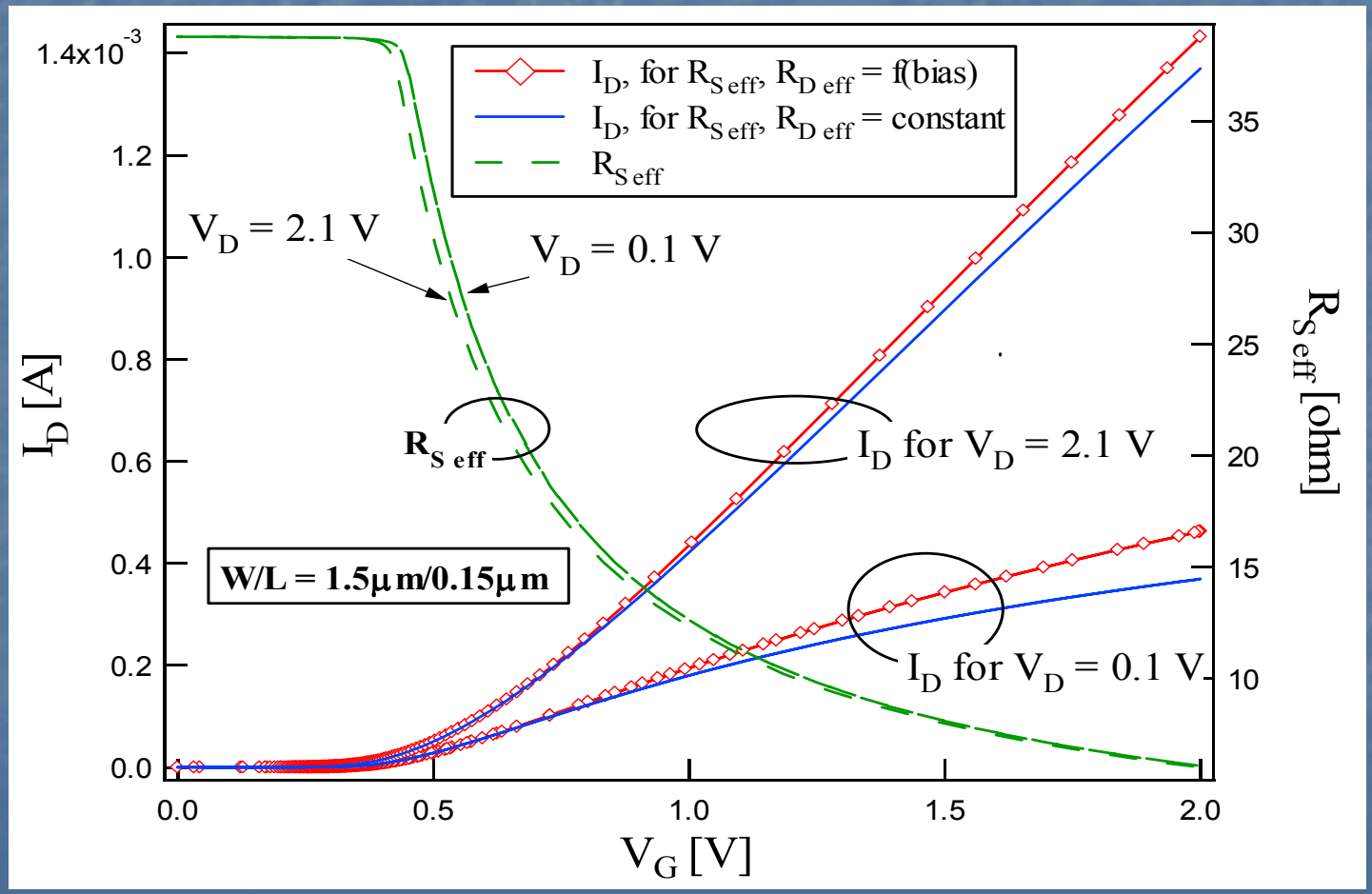
Mandatory when L ≤ 0.35 µ



Capacitances

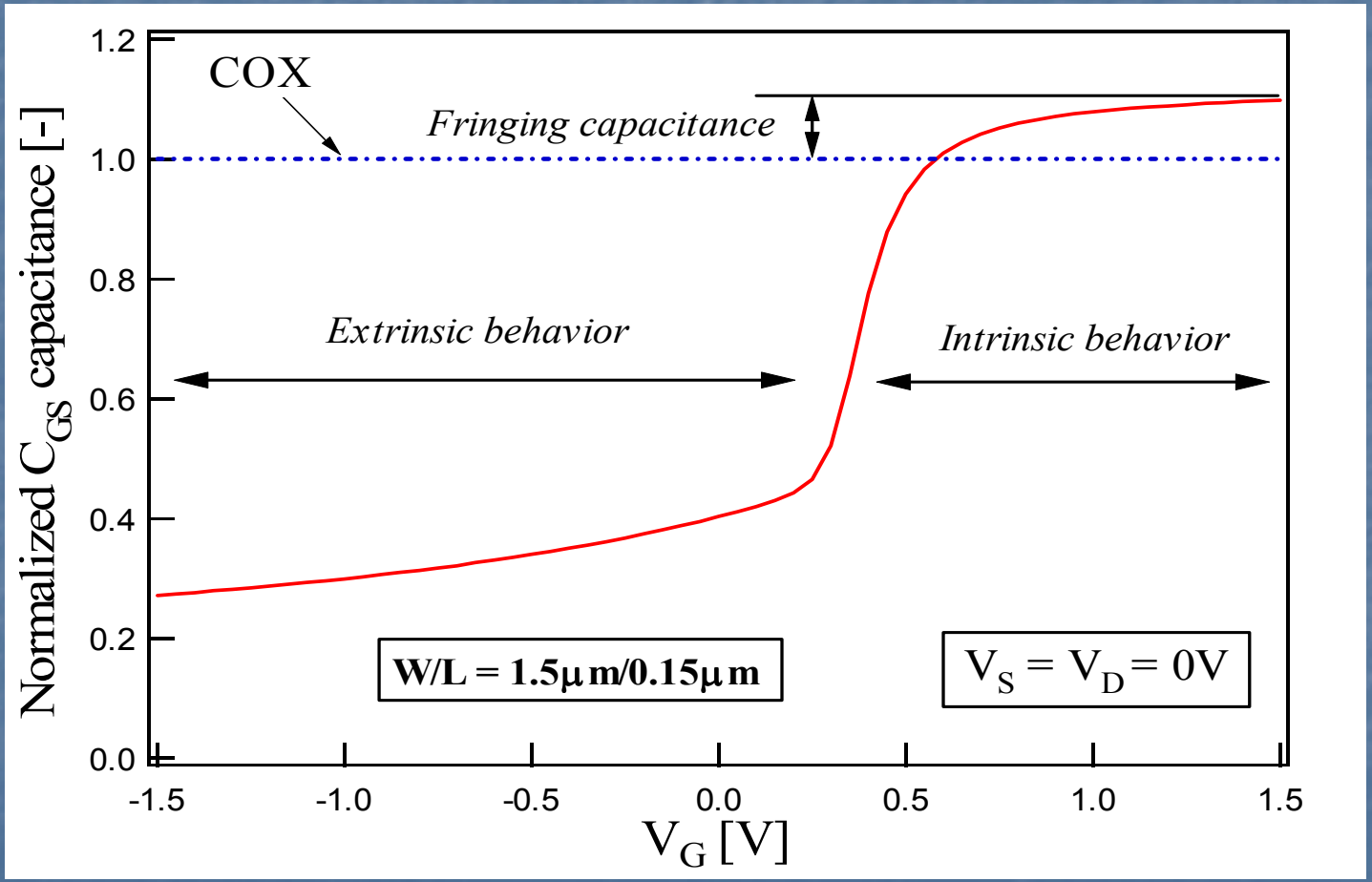
5 parameters added to the EKV model

Series parasitic resistances effects : I_D-V_G and Rs_{eff}/Rd_{eff} - V_G characteristics



VHDL-AMS

Parasitic capacitances



VHDL-AMS

Ongoing researches

- Studies on Modeling on Multi-disciplines systems (electrical, mechanical, thermal, optical, chemical)*

* F. Pécheux, C. Lallement, A. Vachoux, "VHDL-AMS and Verilog-AMS as alternative HDL's for the Efficient Modeling of Multi-disciplines Schemes," 'IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems', **February 20005**

* F. Pécheux, B. Allard, C. Lallement, A. Vachoux, H. Morel "Modeling and simulation using bond graphs and VHDL-AMS" **accepted** to the ICBGM'2005 conference, january 2005, New Orleans - USA

Conclusion

The same system can be implemented both in VHDL-AMS and Verilog-AMS

VHDL-AMS

- + Implicit construction of the Kirchhoff graph
- + Simple Simultaneous statement
- - Non mutable Ports
- - Procedural not supported yet by tools
- Powerful simultaneous statements

Verilog-AMS

- Explicit construction via contribution operator <+
- - Access functions scattered throughout the ODAE
- + Implicit declaration of nets and ports
- + Automatic insertion of connect modules
- + Major enhancements in Verilog-D 2001 but not yet supported by tools

Articles

More informations can be found in:

- F. Pécheux, C. Lallement, A. Vachoux, "VHDL-AMS and Verilog-AMS as alternative HDL's for the Efficient Modeling of Multi-disciplines Schemes," 'IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems', **February 2005**
- F. Pécheux, B. Allard, C. Lallement, A. Vachoux, H. Morel "Modeling and simulation using bond graphs and VHDL-AMS" **accepted to** the ICBGM'2005 conference, january 2005, New Orleans - USA
- F. Pécheux, C. Lallement, "VHDL-AMS and VERILOG-AMS as Competitive Solutions for the High Level Description of Thermoelectrical Interactions in Opto-Electronic Interconnection Schemes," System Specification and Design Languages, Editeurs: E. Villar, J. Mermet, Kluwer (ISBN 1-4020 - 7414-X), pp. 41 - 43, avril 2003.
- C. Lallement, F. Pécheux, W. Grabinski, "High Level Description of Thermodynamical effects in the EKV 2.6 MOST Model (Special session "MOS Modeling and Modern Mixmode Design"), " 9th International Conference Mixed Design of Integrated Circuits and Systems (MIXDES 2002), Wroclaw/Pologne, pages 45-50, juin 2002.
- C. Lallement, F. Pécheux et Y. Hervé, "A VHDL-AMS Case Study: The Incremental Design of an Efficient 3rd generation MOS Model of Deep Sub Micron Transistor," SOC Design Methodologies, Editeurs: M. Robert, B. Rouzeyre, C. Piguet, M. -L. Flottes, Kluwer Academic Publishers, Boston, Hardbound (ISBN 1-4020-7148-5), pages 349 - 360, juillet 2002.
- C. Lallement, F. Pêcheux, Y. Hervé," VHDL-AMS design of a MOST model including deep submicron and thermal-electronic effects," 2001 IEEE Workshop BMAS 2001, pp. 91-96, Santa Rosa, USA, 2001.