
**BSIM2EKV:
BSIM3.3 to EKV2v6 Model Library File
Automatic Conversion Tool**

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BSIM2EKV converter

- Tool for automatic conversion
 - of BSIM (version 3.3) model parameters
 - to EKV (version 2.6) model parameters
- Standalone application (works in interaction with an external simulator)
- Basic principle of the conversion:
 - the curves needed for the parameters extraction are simulated using the BSIM model library file
 - the extraction procedure is based on the complete EKV model parameters extraction methodology

[M. Bucher, C. Lallement, C.C. Enz, "An efficient parameter extraction methodology for the EKV MOST model", International Conference on Microelectronic Test Structures, ICMTS 1996, 25-28 March 1996, pp: 145 – 150]



EKV model

- Dedicated to the design of analog circuits
- Strongly based on device physics
- Has a small number of parameters, but very good accuracy

<http://legwww.epfl.ch/ekv>



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EKV model

- Facilitates **intuitive understanding** of analog structures behavior
- Enables to find **solutions for different input parameters** sets without using complex numerical methods
- Enables the extraction of **transistor parameters important for analog design**, such as:

inversion factor, saturation voltage, Early voltage,
small signal parameters, parasitic capacitances,
gm/ID ratio, transconductance efficiency factor

<http://legwww.epfl.ch/ekv>



BSIM model

- Industrial standard - BSIM (version 3.3)
- Good accuracy
- Large number of parameters
- High complexity



Hand calculations
Approximations
gm/ID ratio, inversion factor

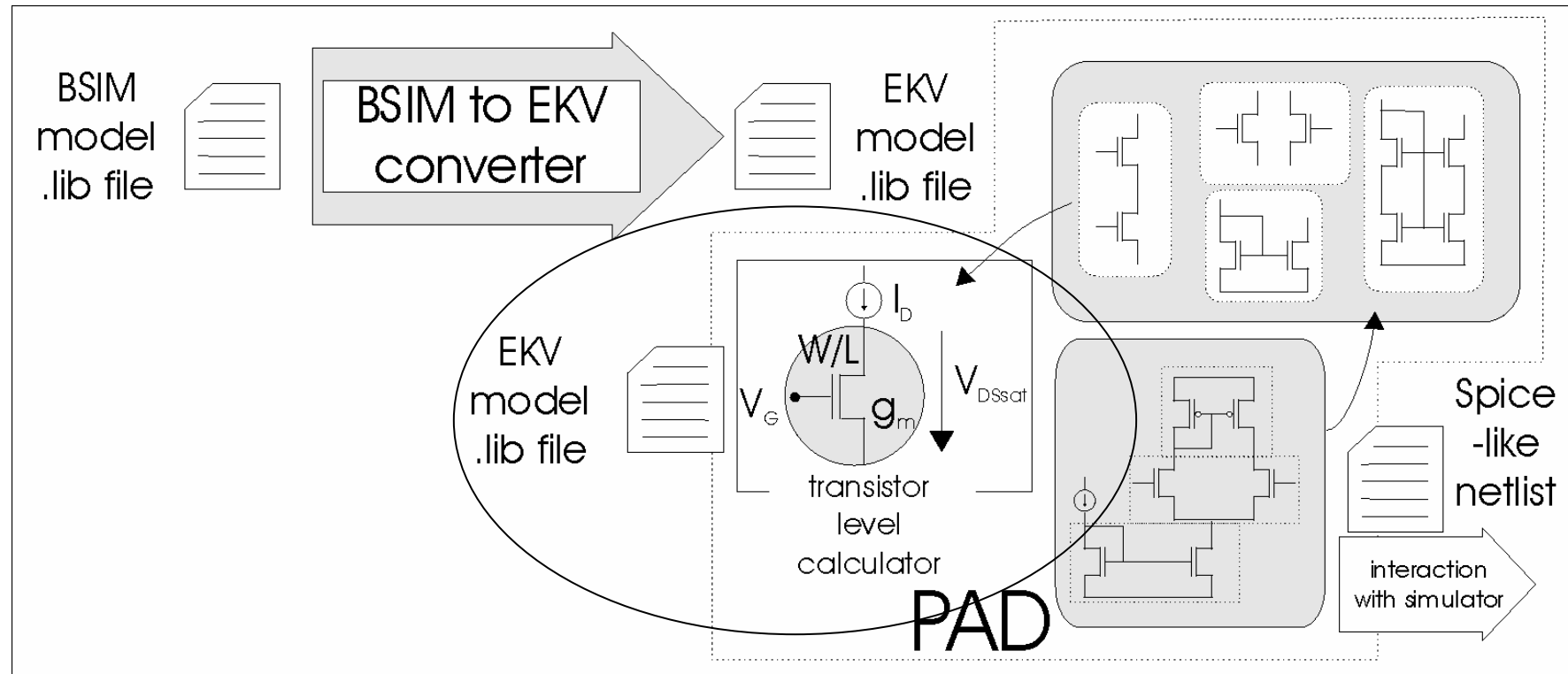
<http://www-device.eecs.berkeley.edu/~bsim>



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Procedural Analog Design



BSIM to EKV conversion

Opens new possibilities to use:

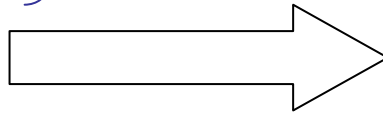
- EKV model (more extensively)
- CAD tools based on EKV model
- gm/Id design methodology



BSIM to EKV conversion

BSIM (version 3.3)

{ PSpice (level = 7)
SMASH (level = 49)



EKV (version 2.6), level = 5

- **intrinsic model parameters**
- **temperature parameters**
- **noise parameters**
- **overlap capacitances**
- **junction capacitance parameters**

Conversion algorithm

Basic concept:

- The curves required for the extraction procedure are simulated using the BSIM model
- Precise sequence of operations
- Minimum error propagation with the respect of fundamentals of two models



Conversion algorithm

The following parameters are read from the BSIM model library file:

- nominal temperature (TNOM)
- process parameters (TOX, XJ, NCH)
- parameters needed for the initial values calculation (U0, VSAT, WINT, LINT)
- gate overlap capacitances (CGBO, CGSO, CGDO)
- junction capacitance parameters (CJ, CJSW, MJ, MJSW, PB, PBSW)



Conversion algorithm

The initial values of some parameters are calculated as follows:

GAMMA	$init = \sqrt{2q\epsilon_{Si}(NSUB \cdot 1e6) / COX}, \quad COX = \epsilon_{OX} / TOX_{BSIM}, \quad NSUB = NCH_{BSIM}$
PHI	$init = 2Vt(TNOM) \ln(NSUB \cdot 1e6 / ni(TNOM))$
KP	$init = (U0 \cdot 1e - 4) COX, \quad U0 = U0_{BSIM}$
E0	$init = 0.1 / (0.4 \cdot TOX)$
DW	$= -2 \cdot WINT_{BSIM}$
DL	$init = -2 \cdot LINT_{BSIM}$
UCRIT	$init = VMAX / (U0 \cdot 1e - 4), \quad VMAX = VSAT_{BSIM}$



Conversion algorithm

The geometrical dimensions of the transistors for simulations are determined as follows:

- wide/long transistor: W_{\max}/L_{\max}
- set of wide/short transistors: (11 transistors)
 $W_{\max}/L_{\min}, 1.2L_{\min}, \dots, 2L_{\min}, 2.4L_{\min}, \dots, 4L_{\min}$
- set of narrow/long transistors: (2 transistors)
 $W_{\min}, 2W_{\min}/L_{\max}$

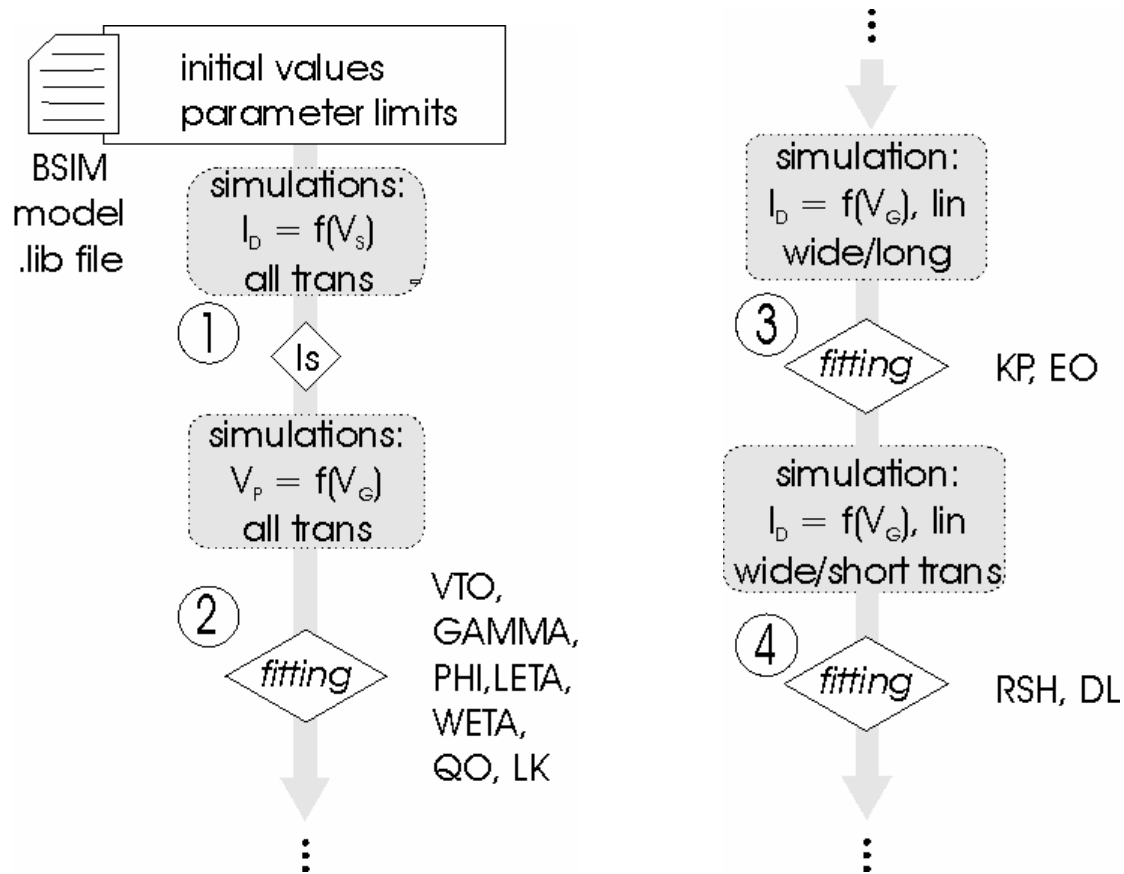


Conversion algorithm

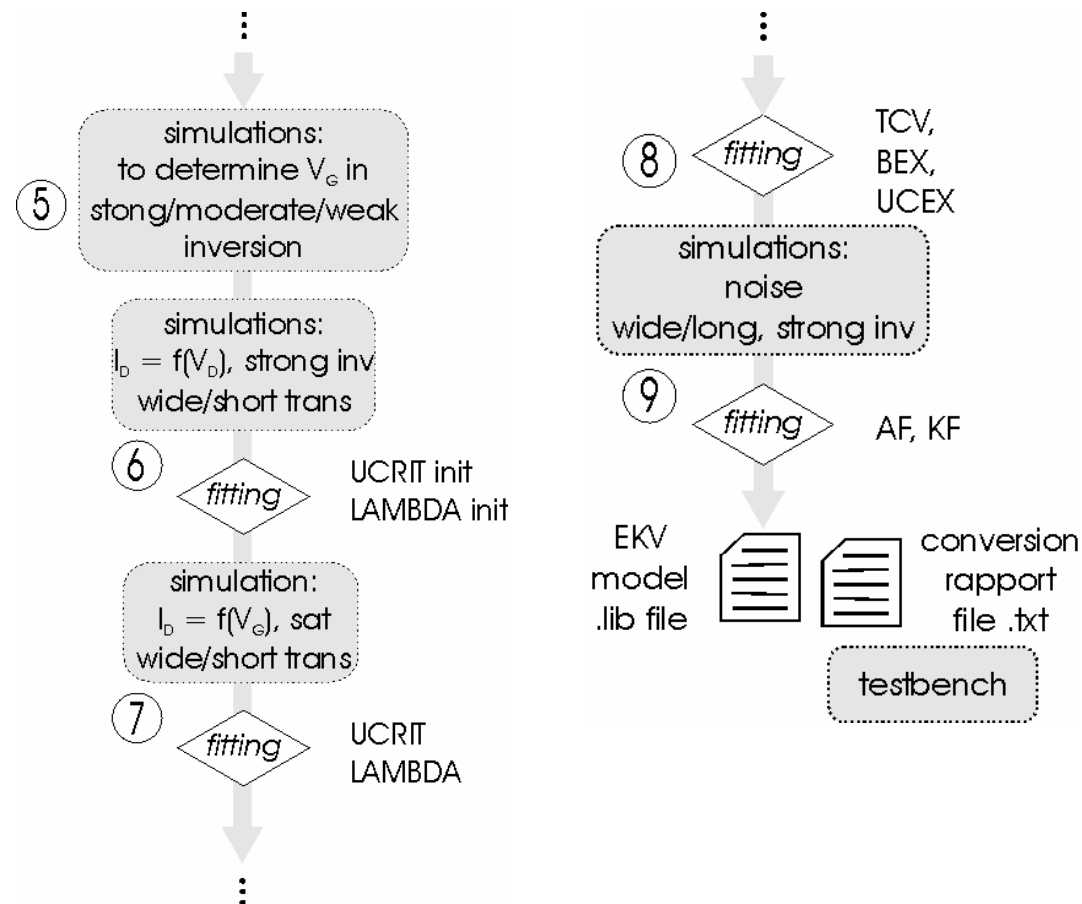
- Alternation of simulation steps and fitting steps
- Specific order of parameter extraction
- No iteration or optimization loops
- Levenberg-Marquardt non-linear least squares method for curves fitting



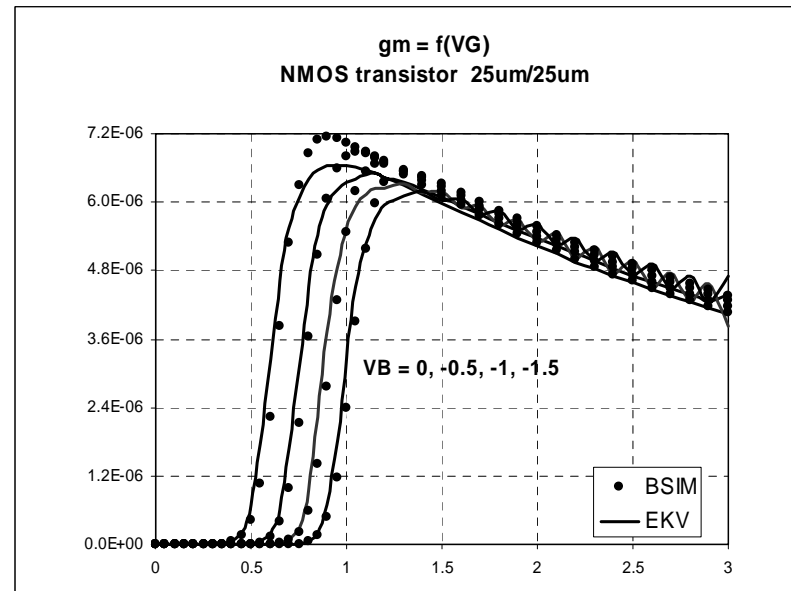
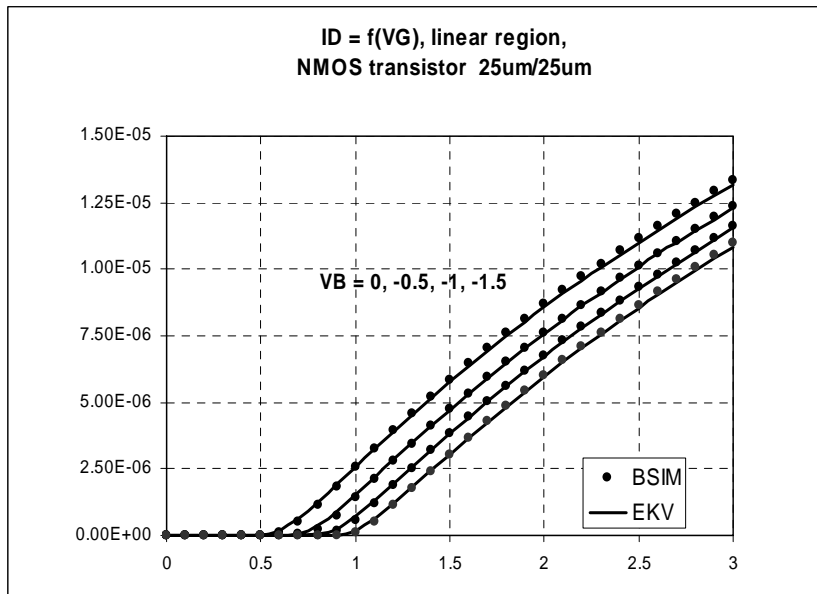
Conversion algorithm



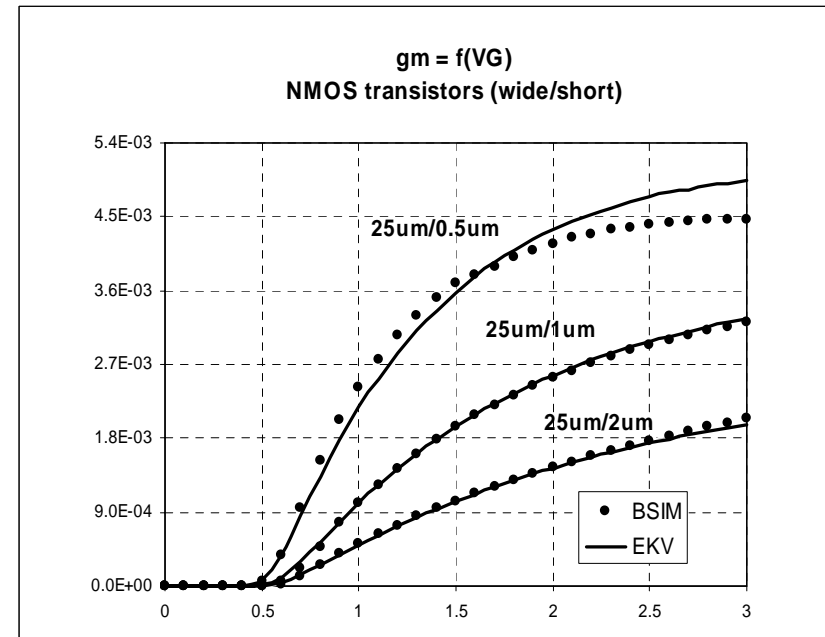
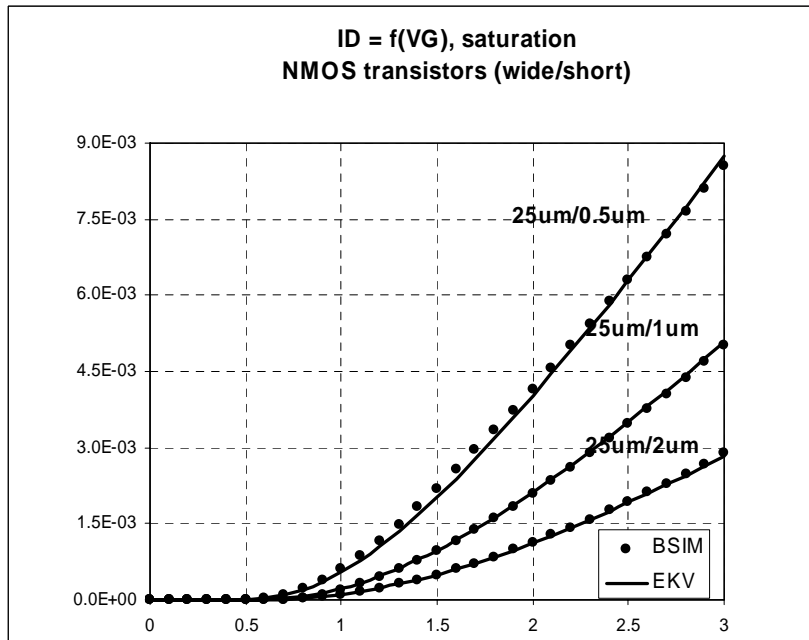
Conversion algorithm



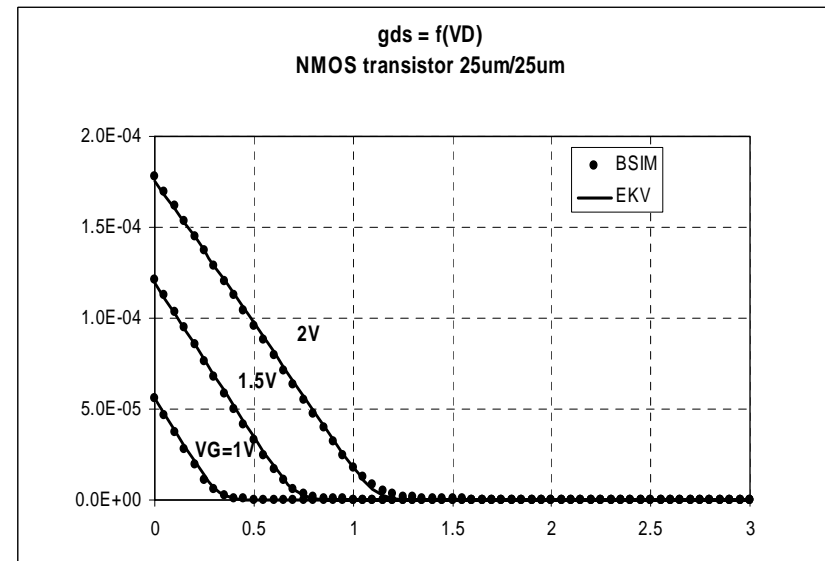
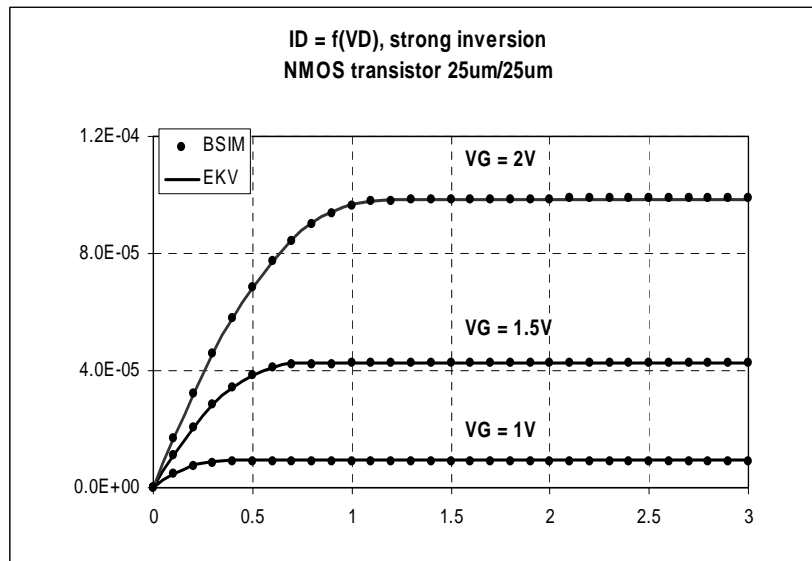
Conversion example (CMOS 0.5 μm technology)



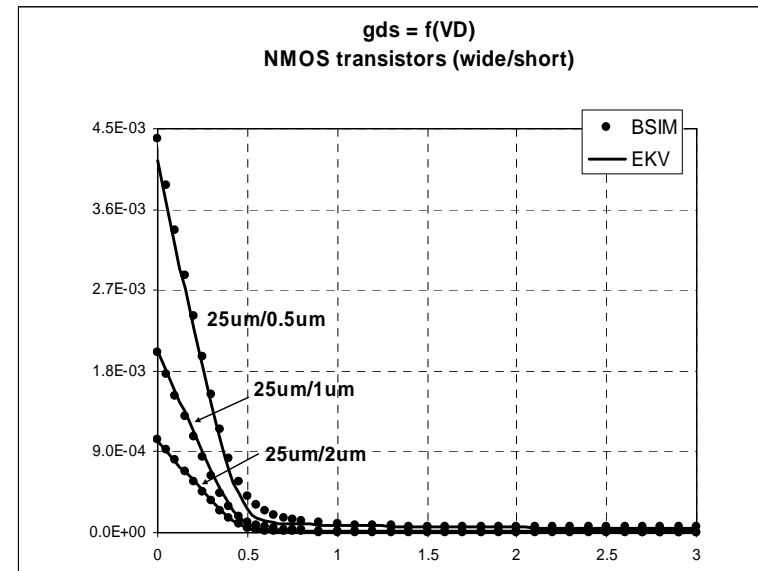
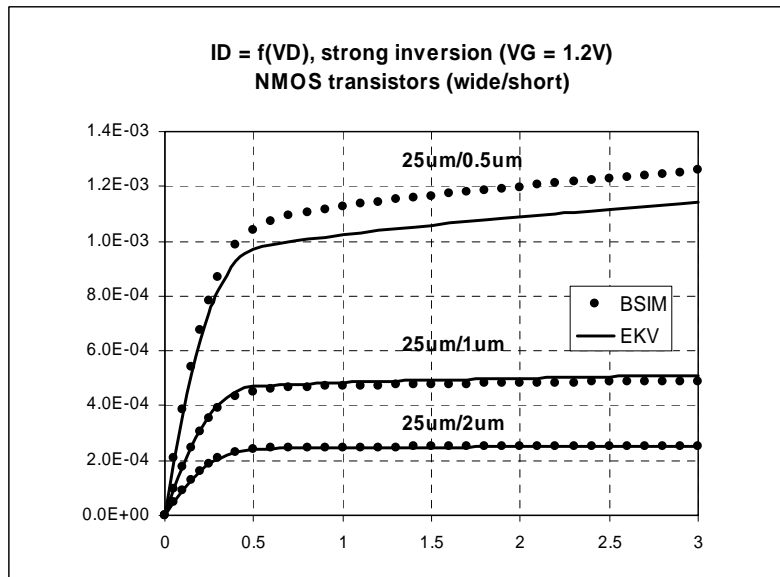
Conversion example (CMOS 0.5 μm technology)



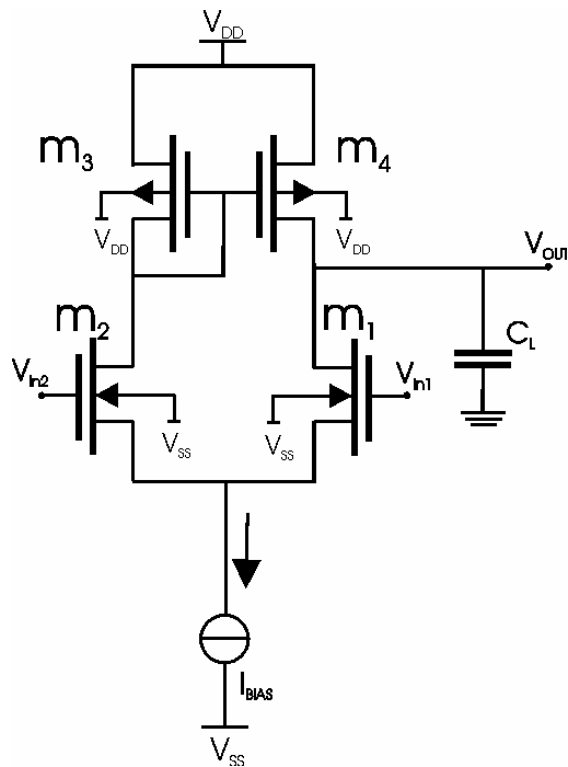
Conversion example (CMOS 0.5 μm technology)



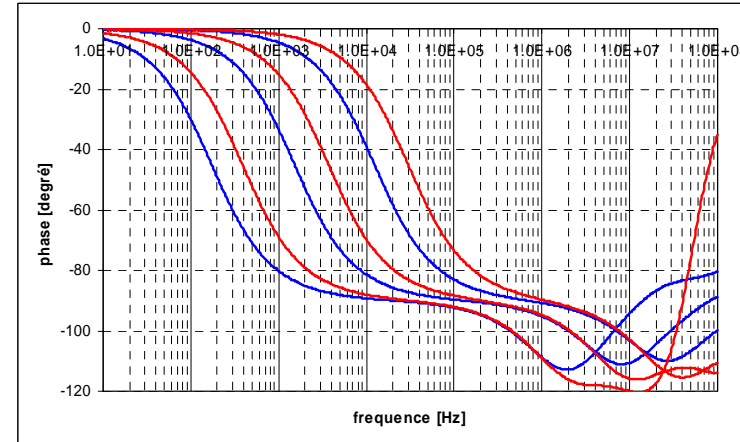
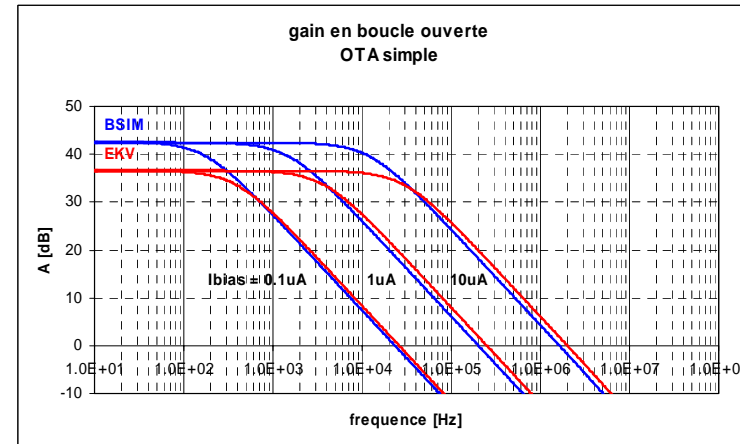
Conversion example (CMOS 0.5 μm technology)



Testbench: open-loop gain, simple OTA



$W_{1,2} = 100L_{min} / L_{1,2} = 2L_{min}$
 $W_{3,4} = 20L_{min} / L_{3,4} = 10L_{min}$
 $C_L = 10pF, I_{bias} = 0.1\mu A, 1\mu A, 10\mu A$



Conclusion

- EKV model – model dedicated to the design of analog circuits
- BSIM model – empirical model, widely used
- BSIM2EKV – enables to generate the EKV model parameters from BSIM model parameters (**within several minutes**) and opens new possibilities to use:
 - ✓ EKV model
 - ✓ PAD
 - ✓ gm/Id design methodology

