PAD:
Procedural Analog Design Tool

D. Stefanovic, M. Kayal, M. Pastre

Swiss Federal Institute of Technology, Electronic Labs, STI/IMM/LEG,
Lausanne, Switzerland

Procedural Analog Design Tool

- Interactive chart-based tool

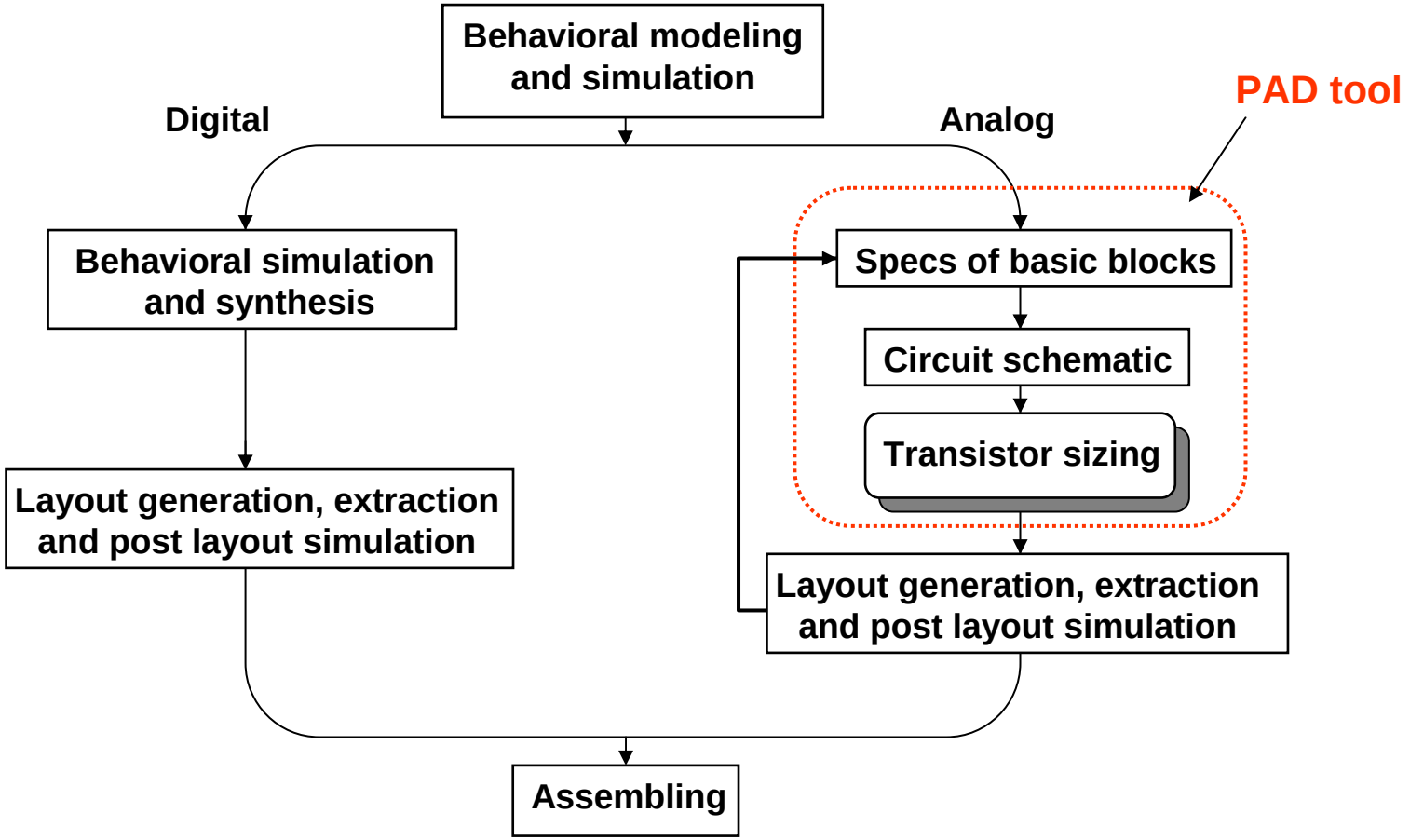
- Dedicated to step-by-step design of analog cells

The present version covers the design of:

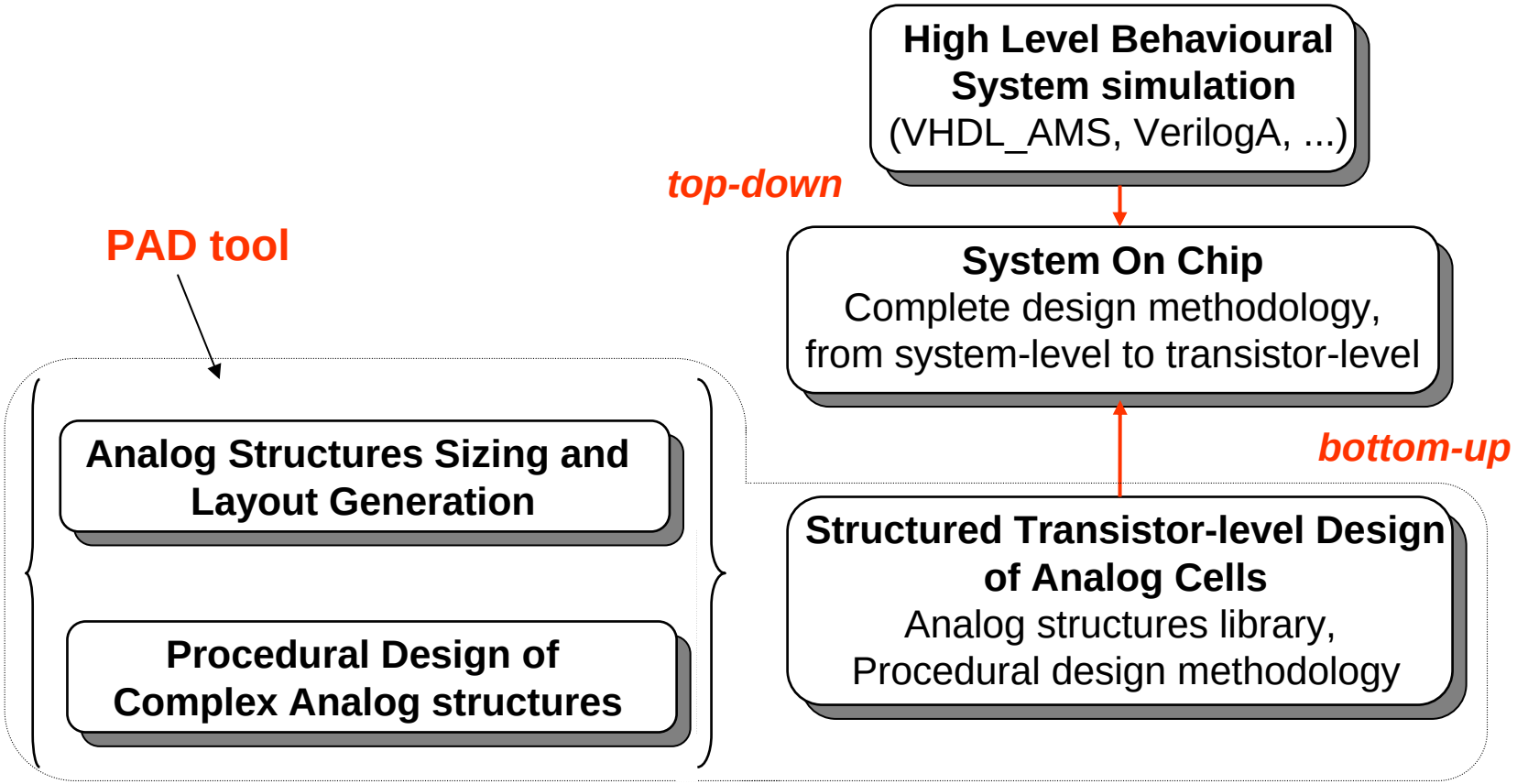
- basic analog structures
- procedural design of OTAs and different operational amplifiers topologies (complex analog structures)

- Transistor-level calculator embedded in PAD uses the complete set of equations of the EKV MOS model

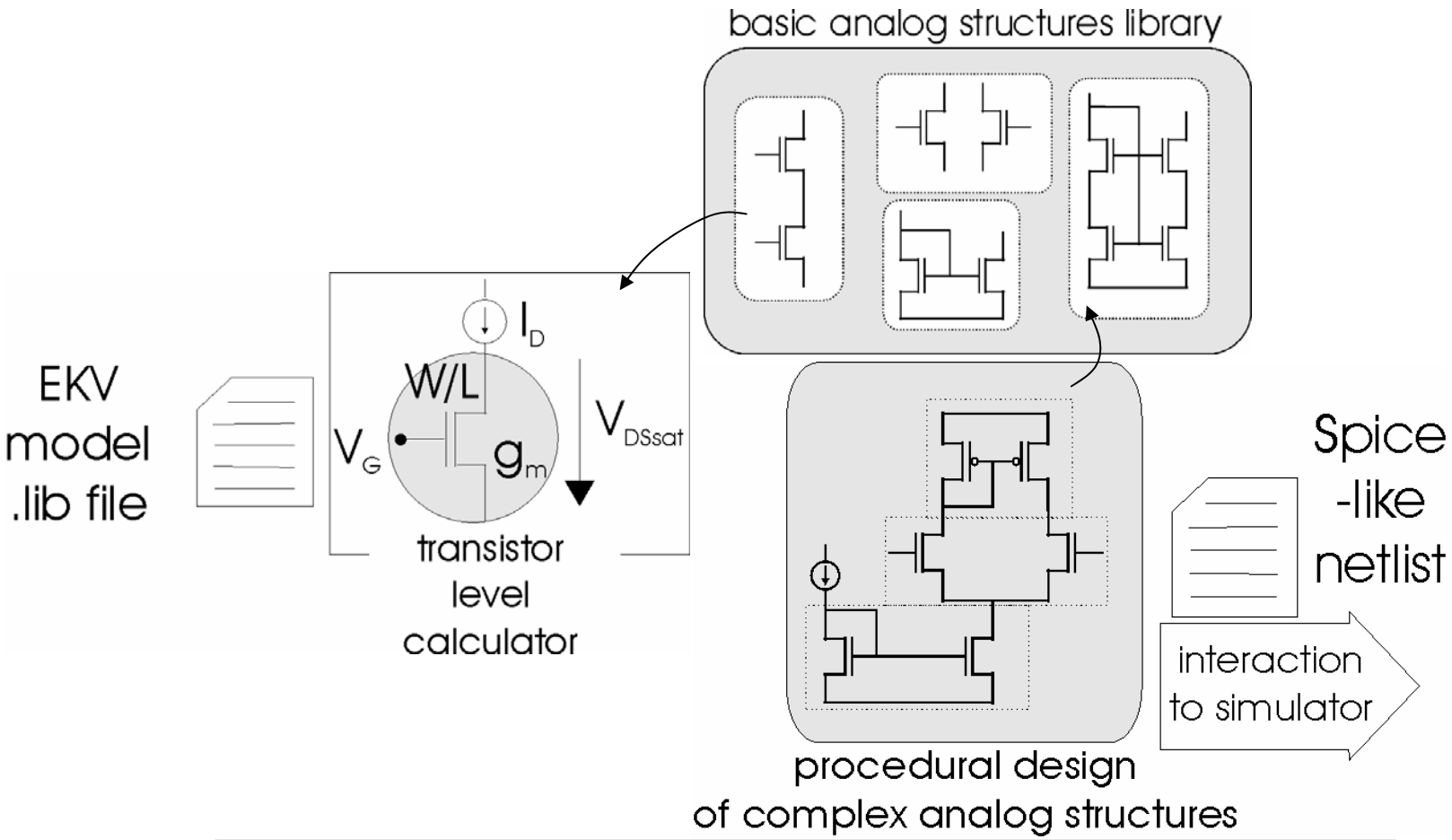
Top down system design approach



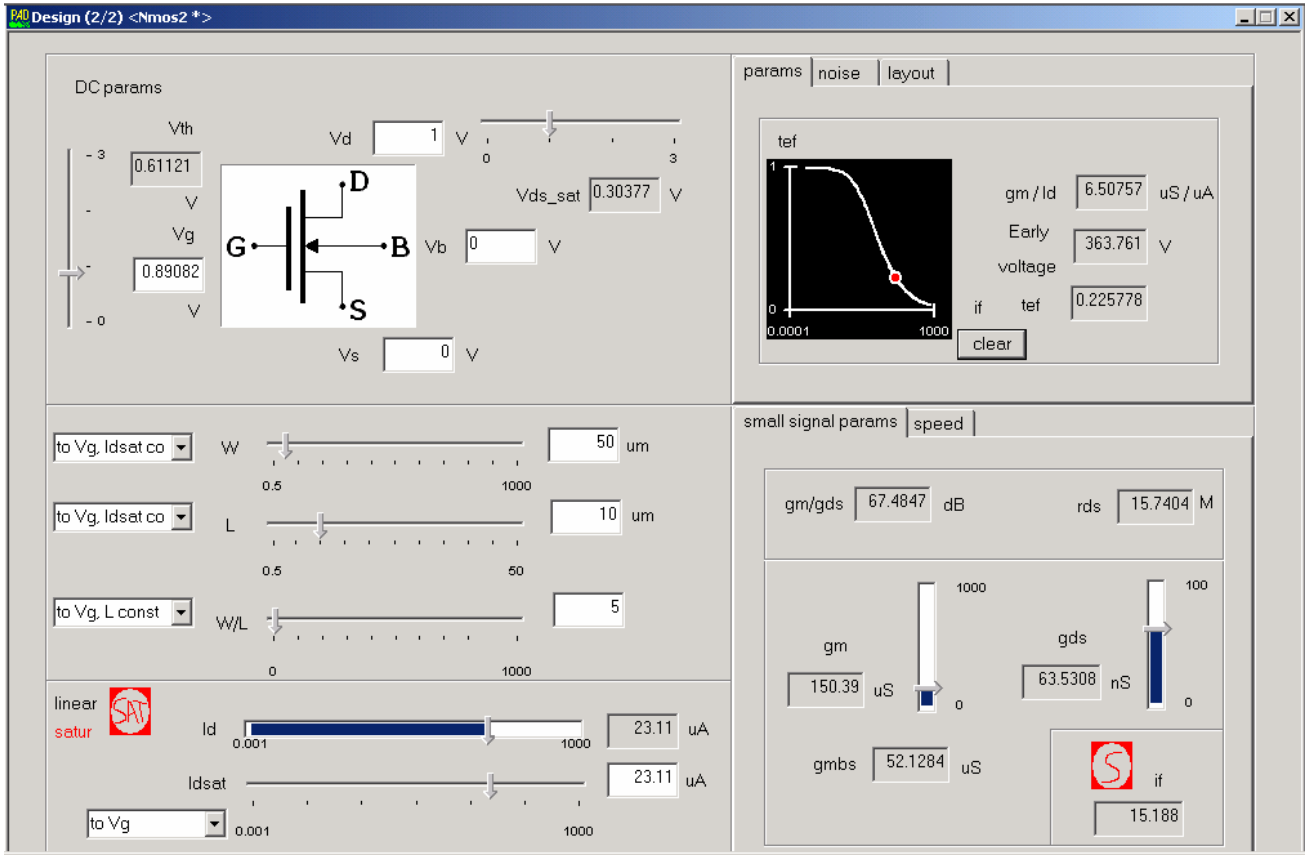
Combine approaches:



PAD structure



The charts !


Design (2/2) <Nmos2 *>
DC params
Vth
0.61121
V
Vg
0.89082
V
Vd
1
V
Vds_sat
0.30377
V
Vb
0
V
Vs
0
V
G
D
B
S
params
noise
layout
tef
gm / Id
6.50757
uS / uA
Early voltage
363.761
V
if tef
0.225778
clear
to Vg, Idsat co
W
50
um
to Vg, Idsat co
L
10
um
to Vg, L const
W/L
5
linear
satur
Id
23.11
uA
Idsat
23.11
uA
to Vg
small signal params
speed
gm/gds
67.4847
dB
rds
15.7404
M
gm
150.39
uS
gds
63.5308
nS
gmbs
52.1284
uS
if
15.188

Transistor level calculator

EKV MOS model

- dedicated to the design of analog circuits
- based on device physics
- links weak and strong inversion in a continuous way
- has small number of model parameters, but good accuracy

- solutions for different input parameter sets are found without using complex numerical methods

- large number of transistor parameters can be extracted

Analog structures library

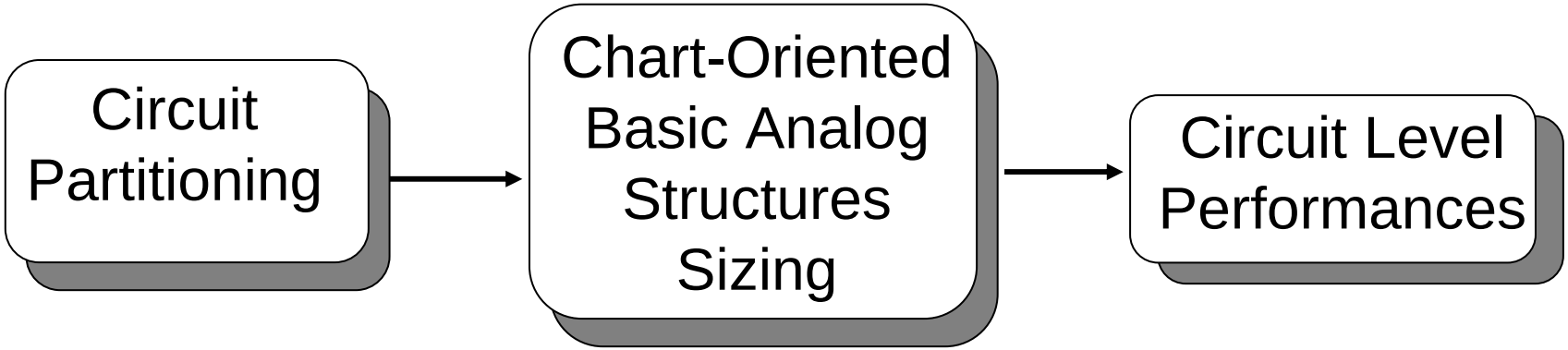
- single transistor
- current mirror
- cascode current mirror
- differential pair
- cascode stage
- folded cascode stage
- common source
- common drain

- general params
  - small signal params
  - DC biasing values
  - parasitic capas
  - transition frequency
- specific params
  - maximum DC offset
  - current mismatch
  - output resistance
  - gain

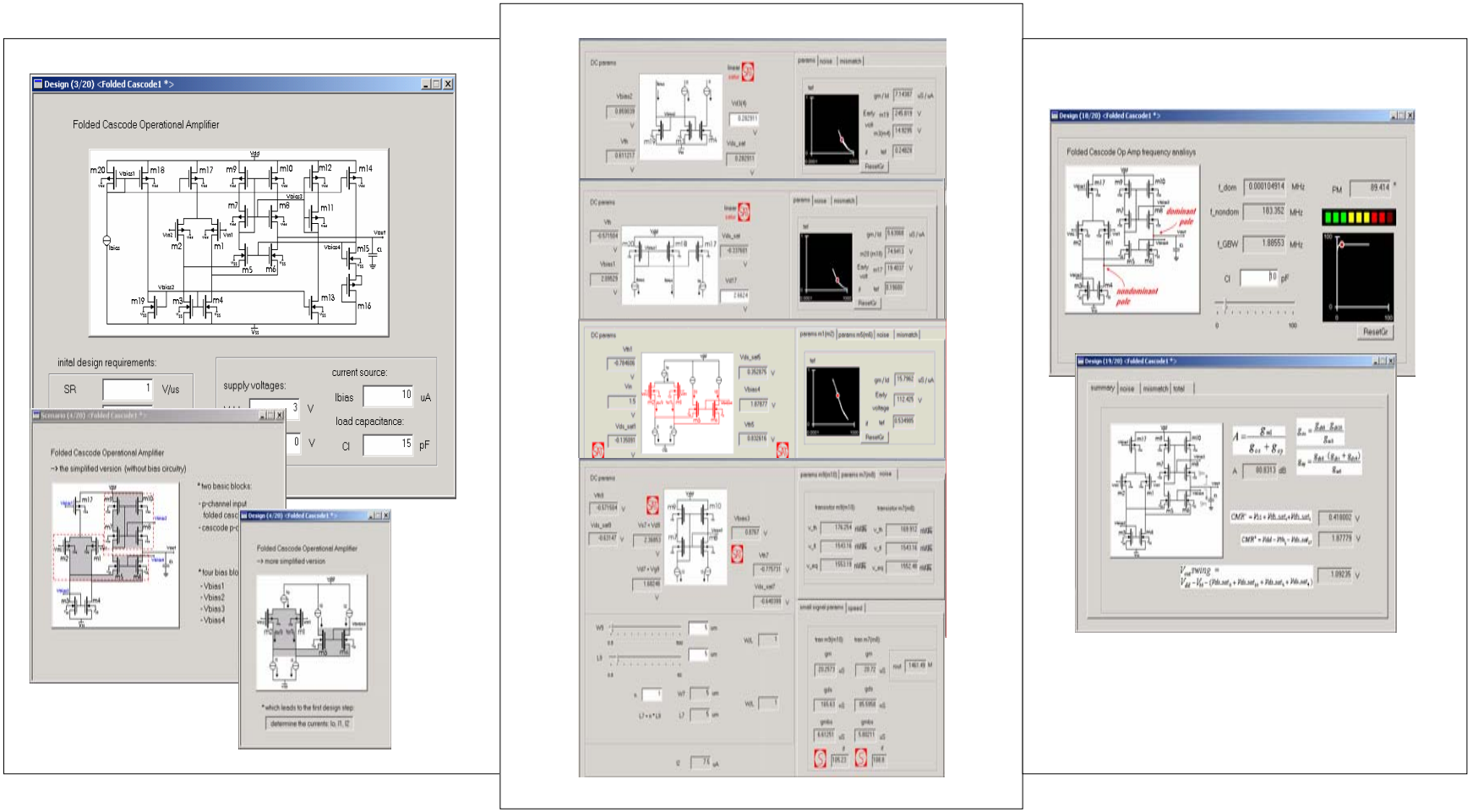
g_m/I_D design procedure

- set priority targets (gain, noise, speed…)
- choose bias current and accordingly gm/Id ratio
- change free variables (W, L)
- observe effects on other parameters

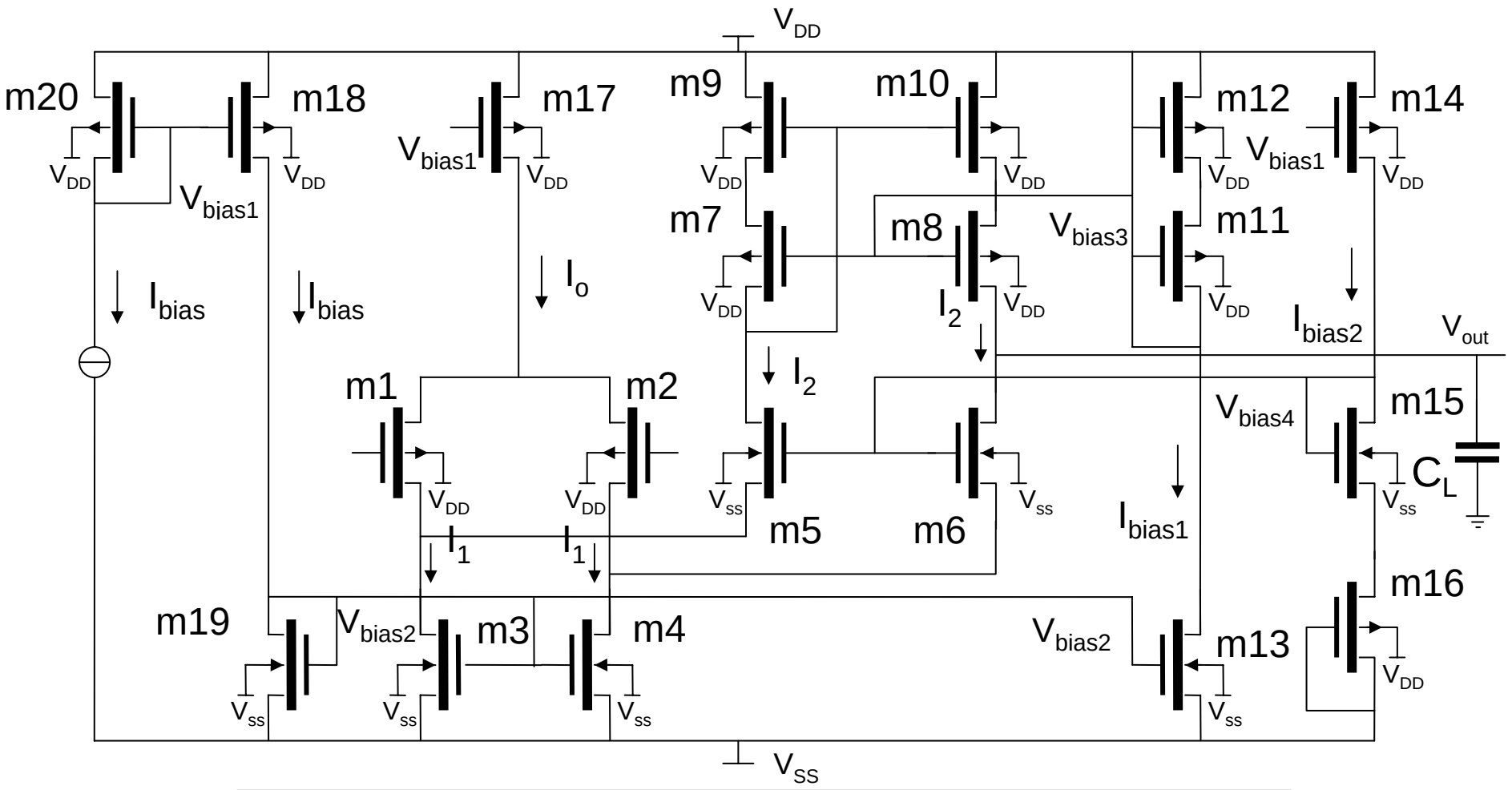
Procedural Design of Complex Structures



Procedural Design of Complex Structures

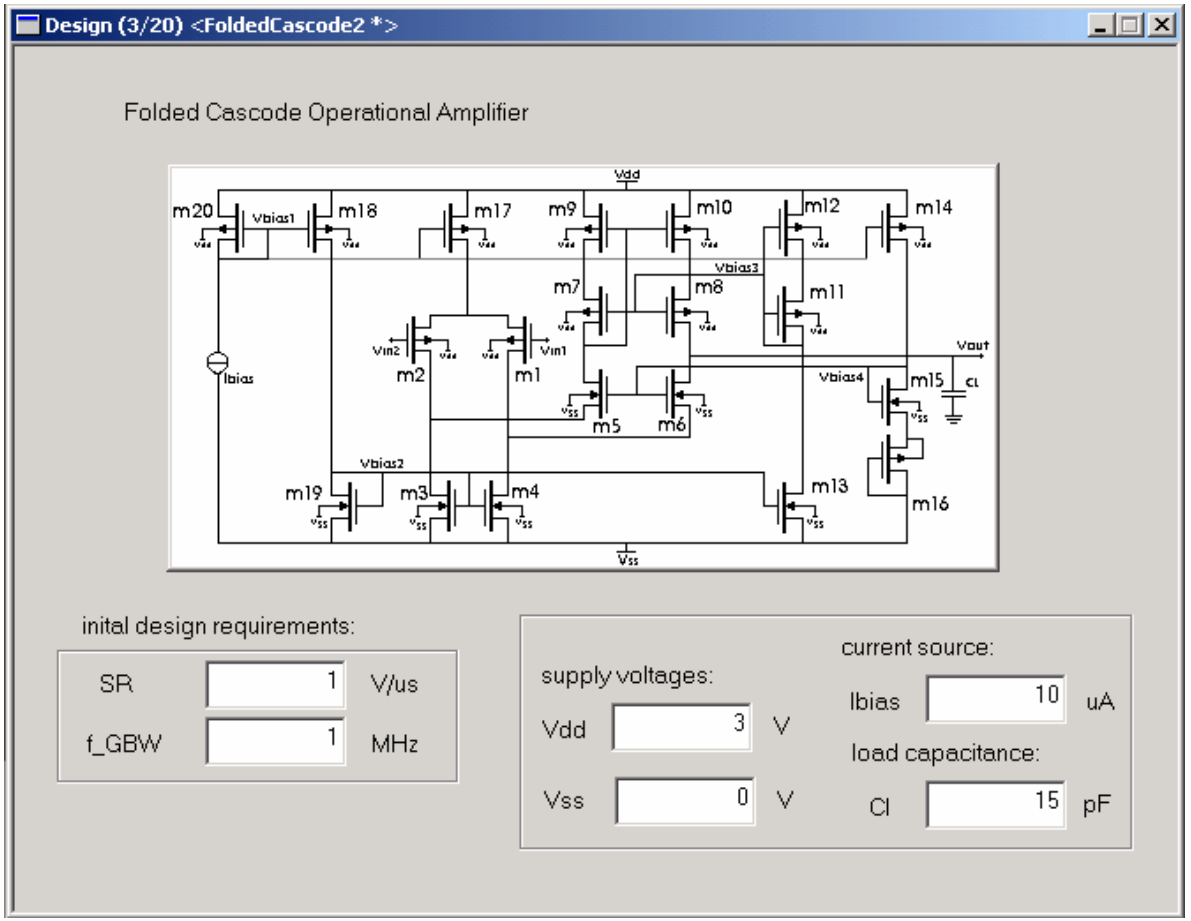


Procedural Design of Folded Cascode OTA



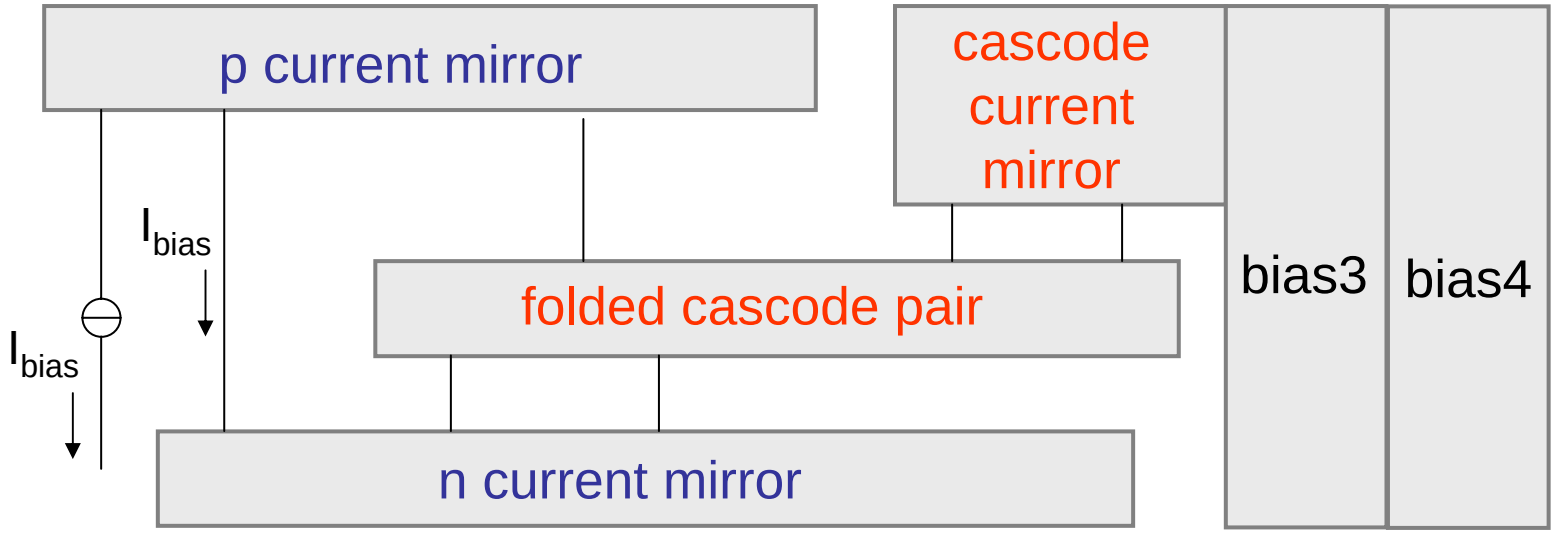
PAD Design Flow

Initialisation :



PAD Design Flow

Circuit partitioning :

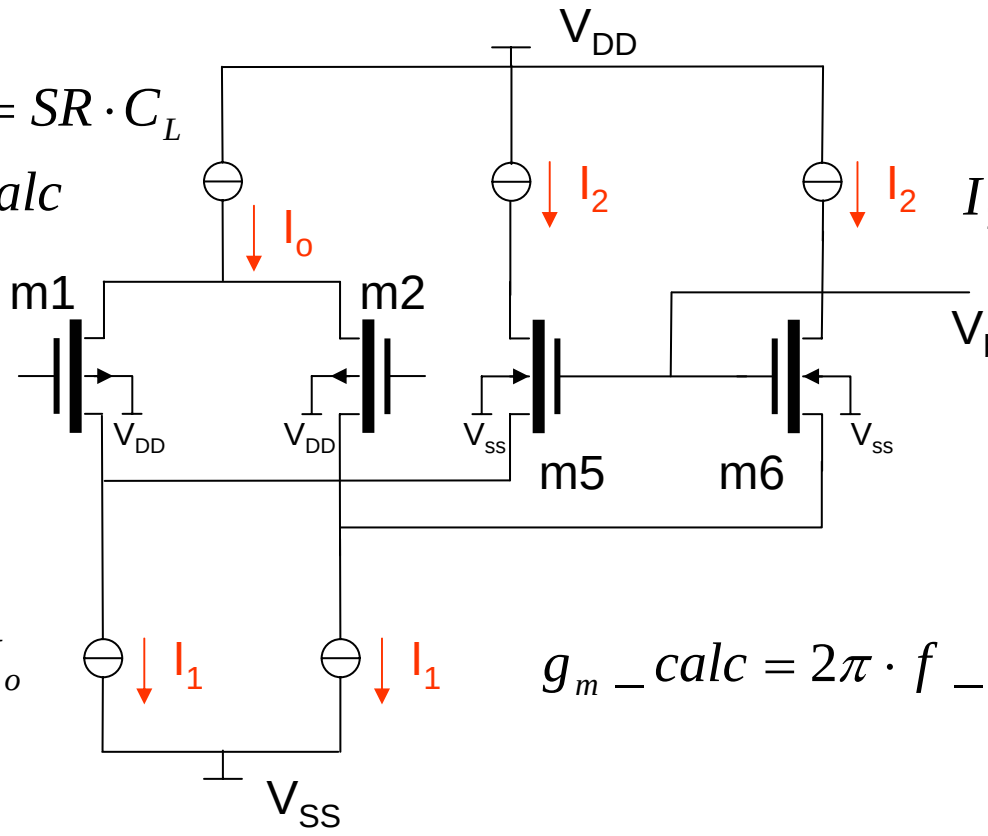


PAD Design Flow

Determination of circuit currents :

$$I_o\_calc = SR \cdot C_L$$

$$I_o \geq I_o\_calc$$



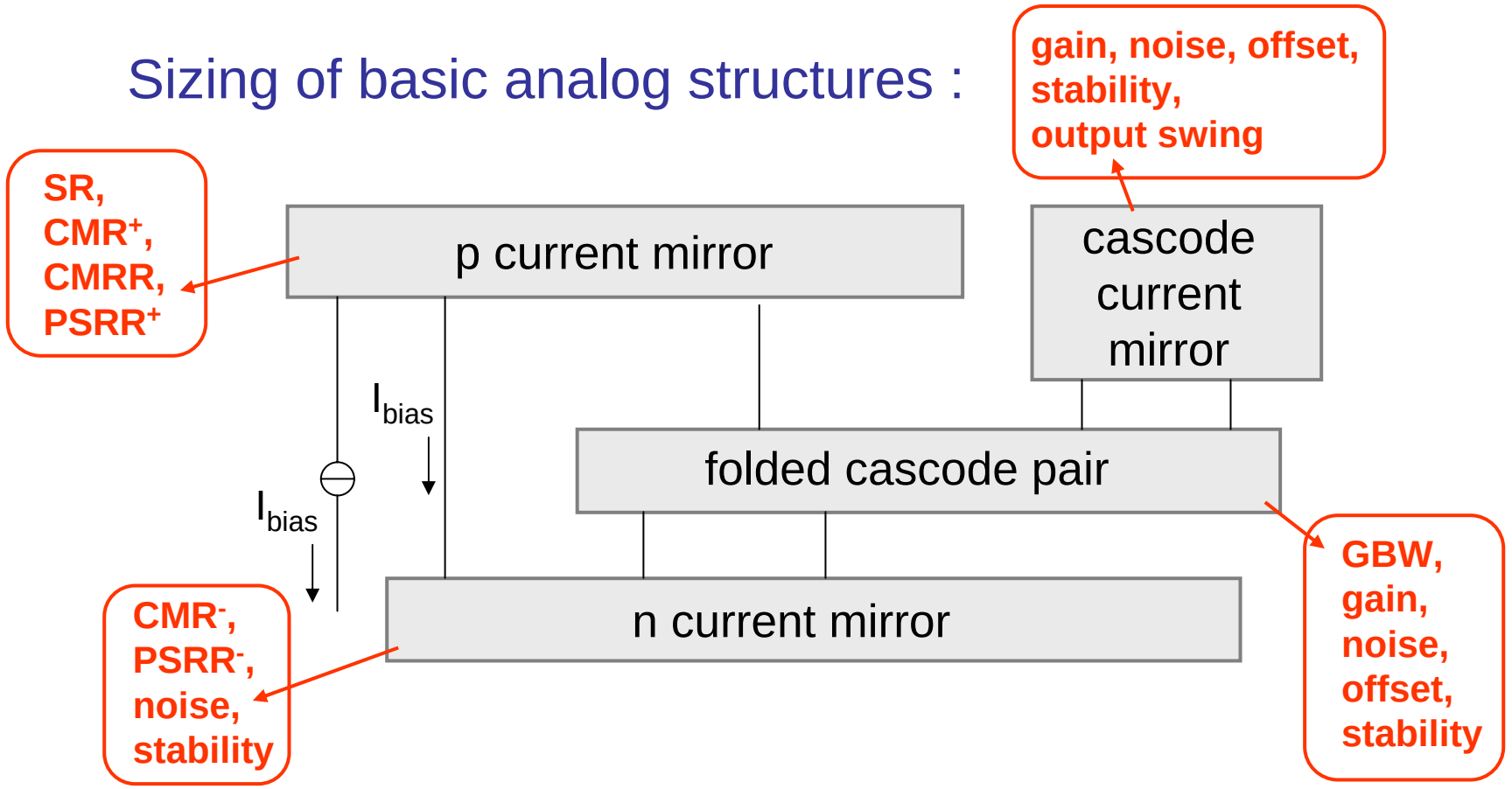
$$I_2 = I_1 - \frac{I_o}{2}$$

$$I_o \leq I_1 \leq n \cdot I_o$$

$$g_m\_calc = 2\pi \cdot f\_GBW \cdot C_L$$

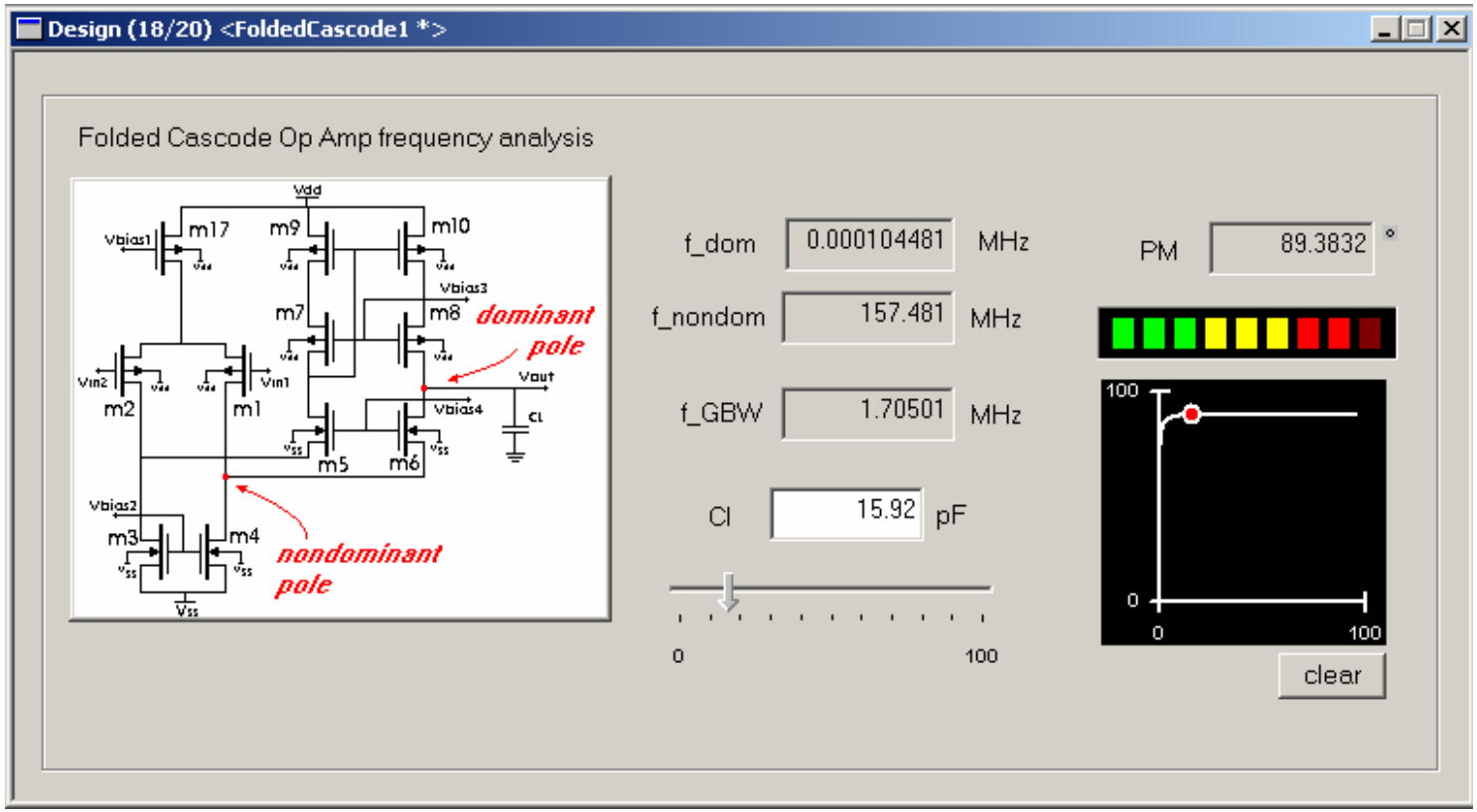
PAD Design Flow

Sizing of basic analog structures :



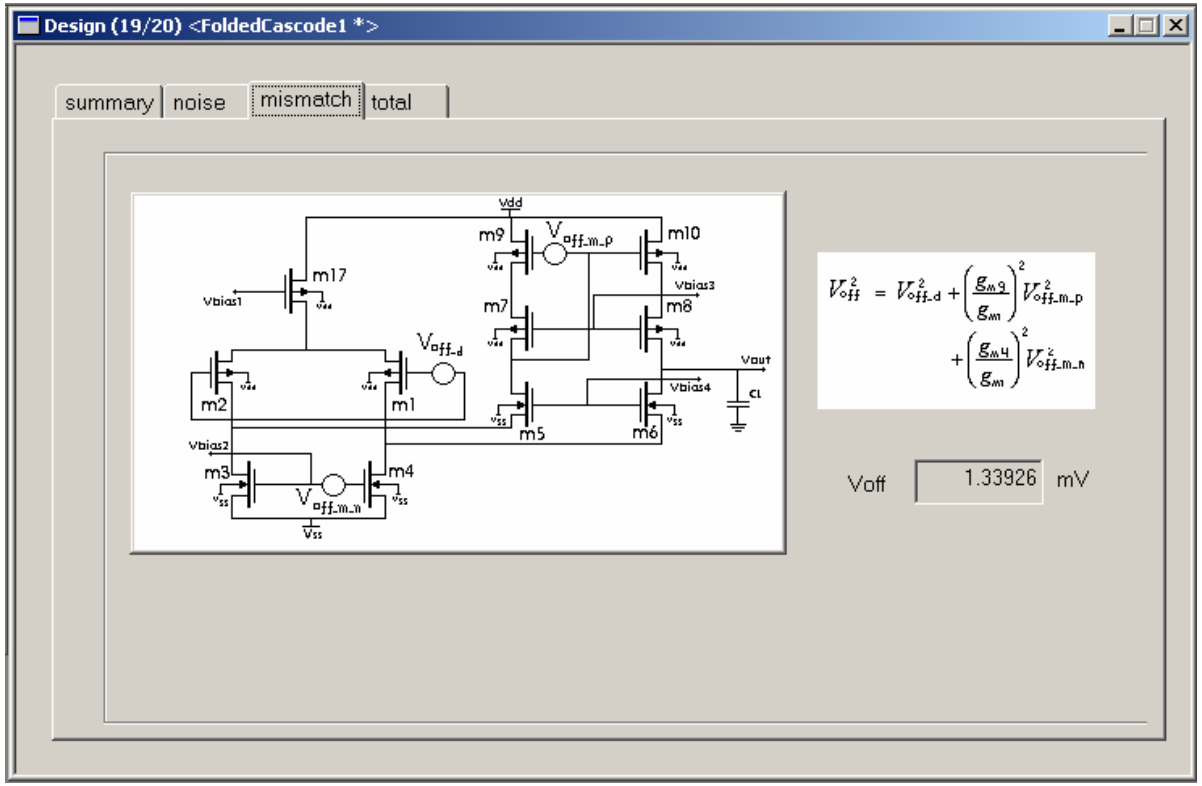
PAD Design Flow

Circuit level design :



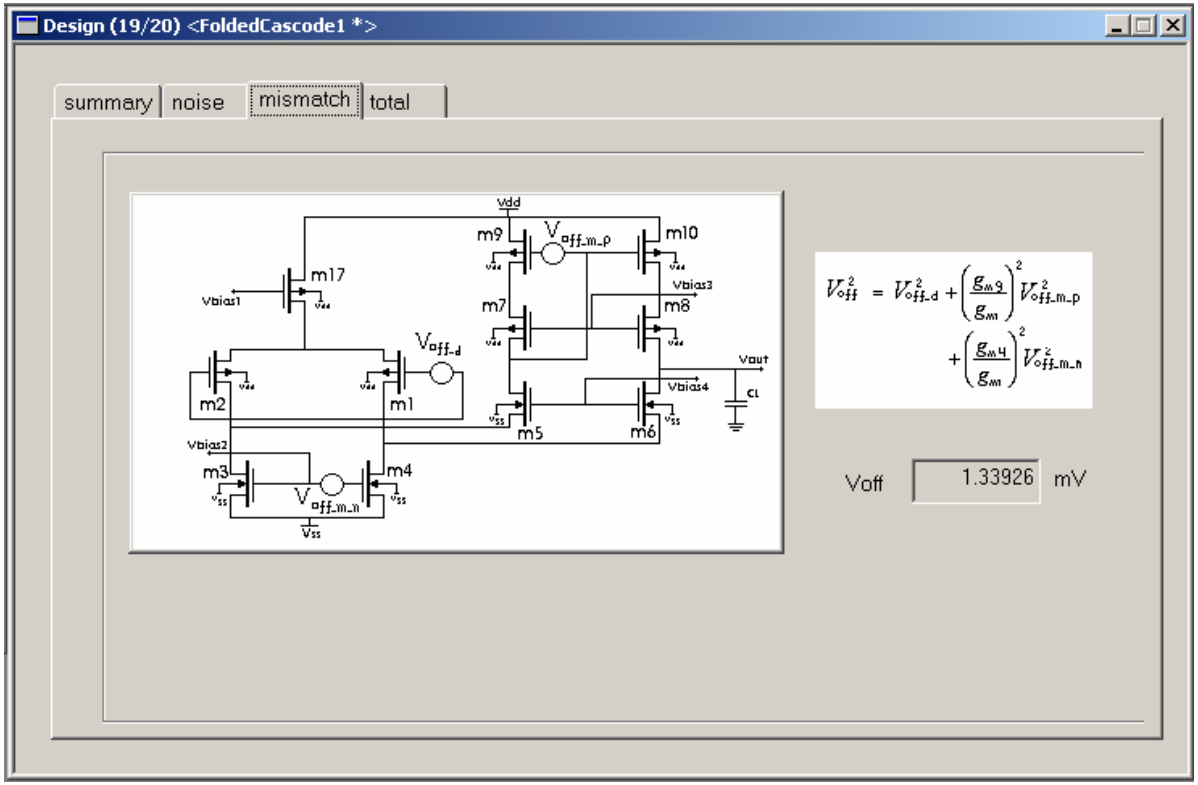
PAD Design Flow

Circuit level design :



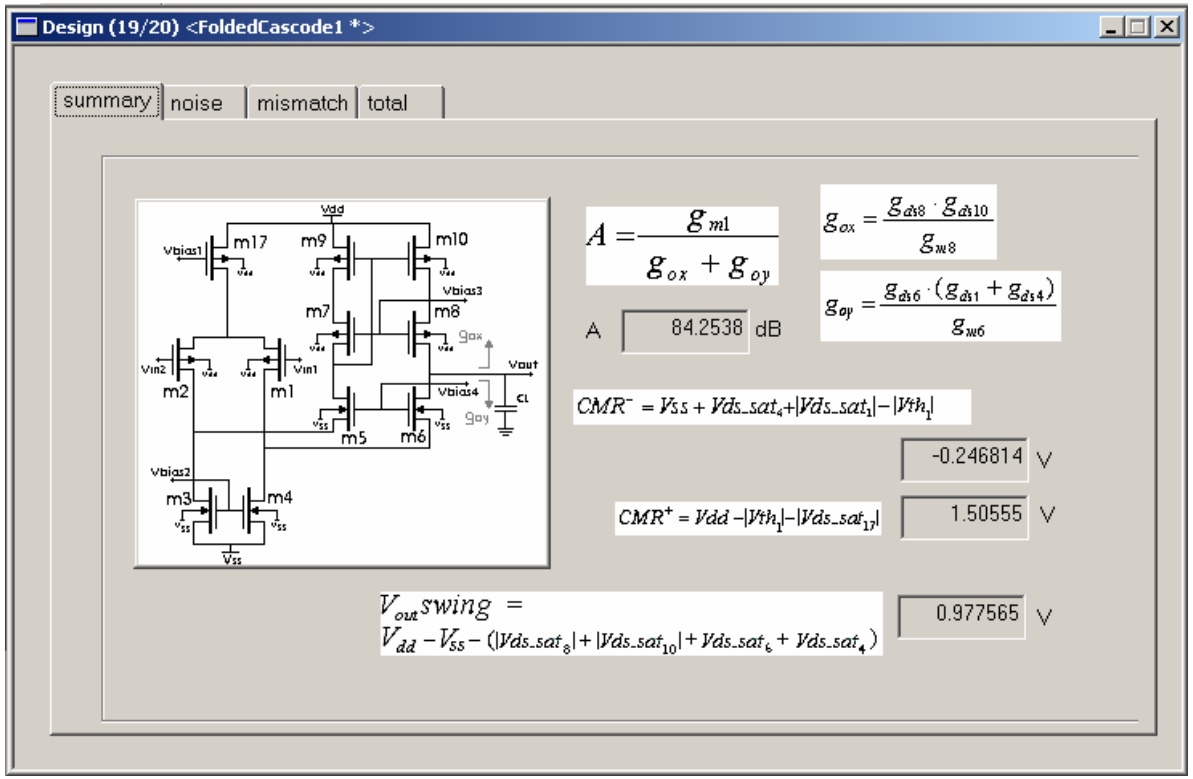
PAD Design Flow

Circuit level design :



PAD Design Flow

Circuit level design :



Conclusion

- new chart-based procedural analog design tool
- new knowledge-based analog design methodology

- design and re-design of wide range of circuits
- didactical tool that helps to hand analog knowledge towards non-expert designer

Download

http://legwww.epfl.ch/CSL

If you have any questions:

maher.kayal@epfl.ch
danica.stefanovic@epfl.ch