
PAD: **Procedural Analog Design Tool**

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Procedural Analog Design Tool

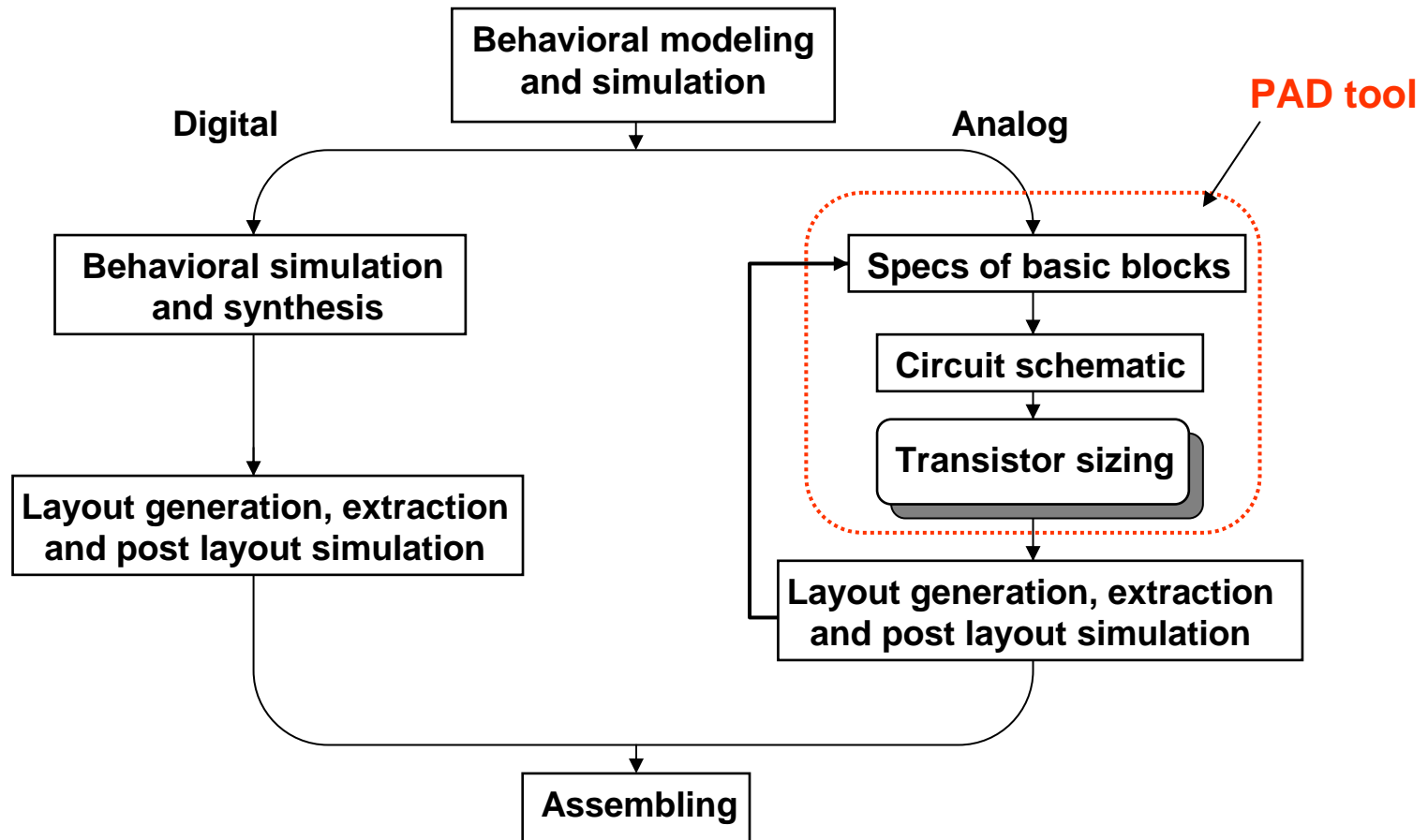
- Interactive chart-based tool
- Dedicated to step-by-step design of analog cells

The present version covers the design of:

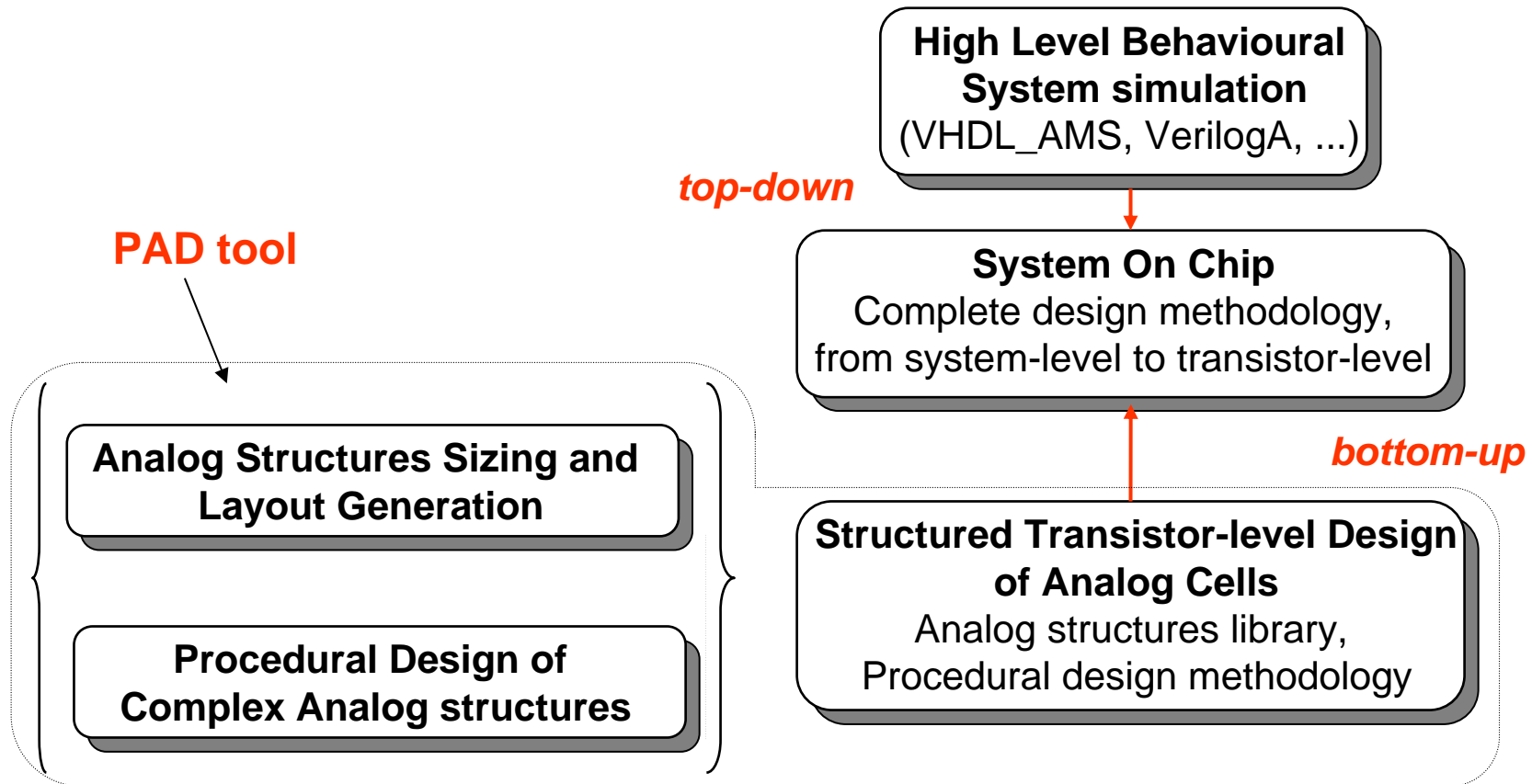
- basic analog structures
- procedural design of OTAs and different operational amplifiers topologies (complex analog structures)
- Transistor-level calculator embedded in PAD uses the complete set of equations of the EKV MOS model



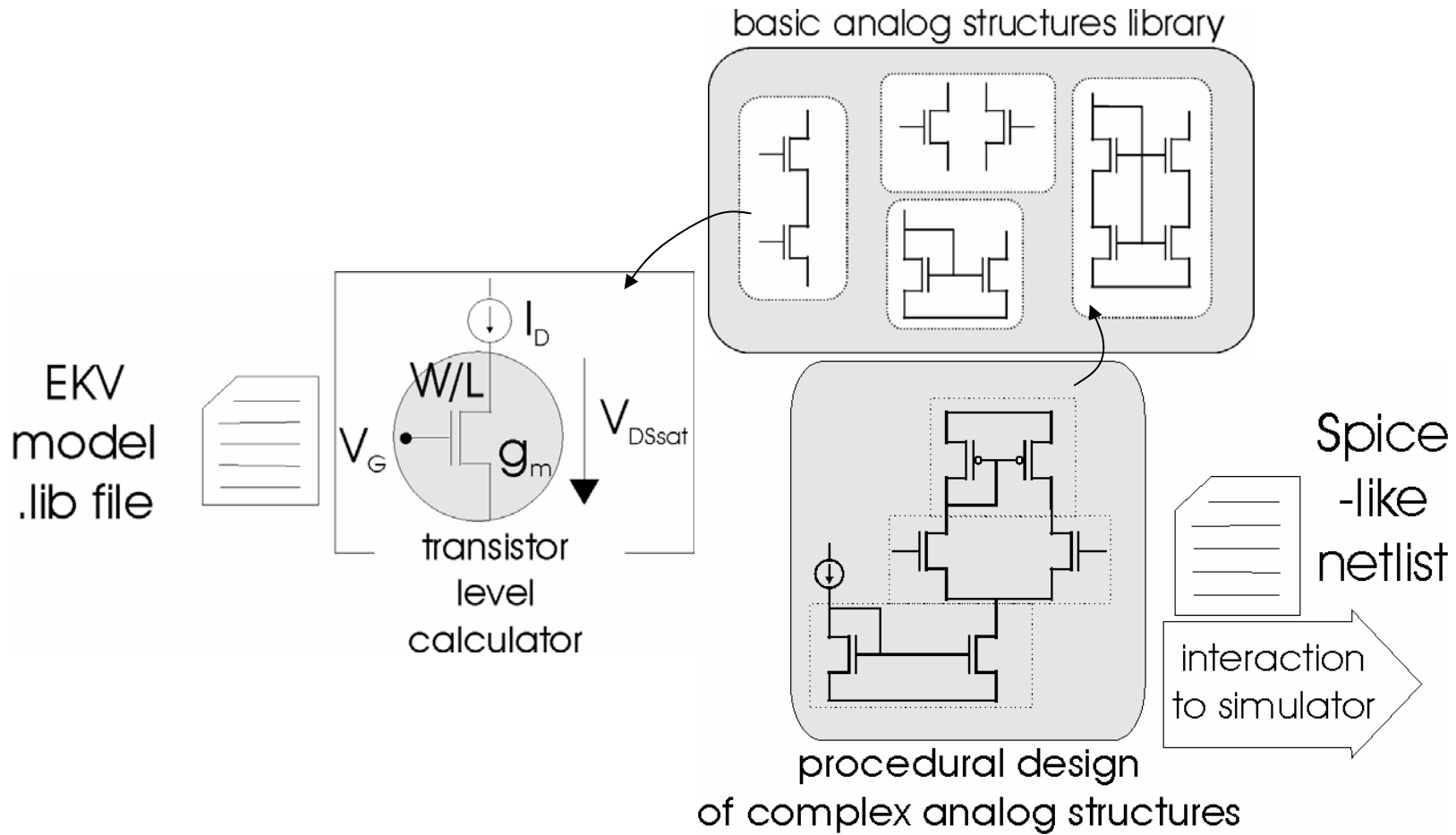
Top down system design approach



Combine approaches:



PAD structure



The charts !

The screenshot displays the PAD Design (2/2) <Nmos2 +> interface, which is used for configuring and simulating an Nmos2 transistor. The interface is divided into several sections:

- DC params:** This section includes a schematic diagram of an Nmos2 transistor with terminals G (Gate), D (Drain), B (Bulk), and S (Source). The parameters are: $V_{th} = 0.61121$ V, $V_g = 0.89082$ V, $V_d = 1$ V, $V_b = 0$ V, $V_s = 0$ V, and $V_{ds_sat} = 0.30377$ V.
- Small signal params:** This section shows various parameters: $gm/gds = 67.4847$ dB, $r_{ds} = 15.7404$ M, $gm = 150.39$ uS, $gds = 63.5308$ nS, $g_{mbs} = 52.1284$ uS, and $if = 15.188$.
- Physical parameters:** This section includes sliders for W (width) set to 50 um, L (length) set to 10 um, and W/L set to 5. There are also dropdown menus for "to Vg, Idsat co" and "to Vg, L const".
- Simulation mode:** The "linear" mode is selected, with a "SAT" icon indicating saturation.
- Currents:** I_d is set to 23.11 uA and I_{dsat} is also set to 23.11 uA.
- Chart:** A "tef" chart is displayed, showing a curve that starts at 1 and decreases towards 0 as frequency increases from 0.0001 to 1000. A red dot is placed on the curve at approximately 1000.

Transistor level calculator

EKV MOS model

- dedicated to the design of analog circuits
- based on device physics
- links weak and strong inversion in a continuous way
- has small number of model parameters, but good accuracy
- solutions for different input parameter sets are found without using complex numerical methods
- large number of transistor parameters can be extracted



Analog structures library

- single transistor
- current mirror
- cascode current mirror
- differential pair
- cascode stage
- folded cascode stage
- common source
- common drain

■ general params

- small signal params
- DC biasing values
- parasitic capas
- transition frequency

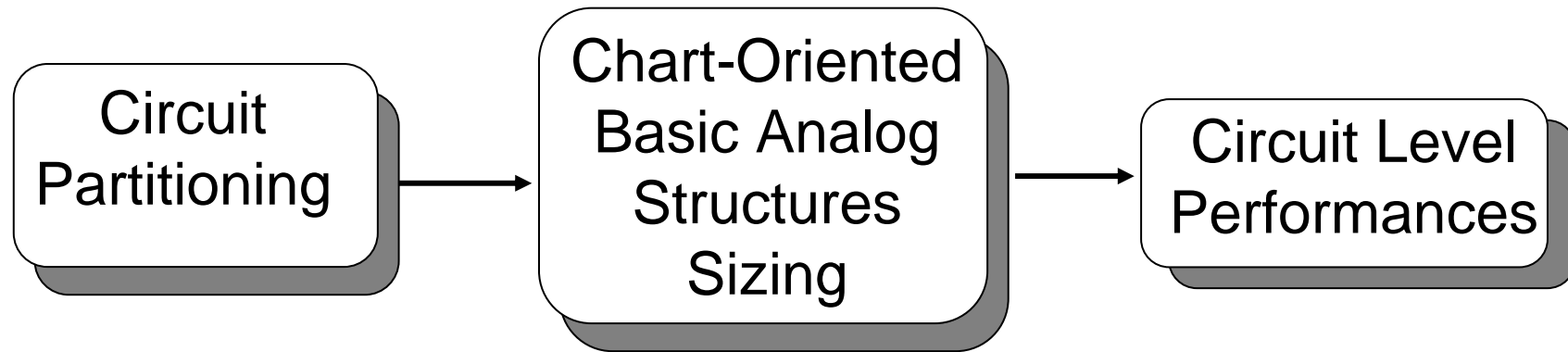
■ specific params

- maximum DC offset
- current mismatch
- output resistance
- gain

g_m/I_D design procedure

- set priority targets (gain, noise, speed...)
- choose bias current and accordingly g_m/I_D ratio
- change free variables (W , L)
- observe effects on other parameters

Procedural Design of Complex Structures



Procedural Design of Complex Structures

The image displays a series of screenshots from a circuit design software, illustrating the procedural design of a complex structure, specifically a folded cascode operational amplifier.

Design (3/20) - Folded Cascode1 *

Folded Cascode Operational Amplifier

intel design requirements:

- SR: 1 V/us
- supply voltages: 3 V
- current source: 10 uA
- load capacitance: 15 pF

Design (4/20) - Folded Cascode1 *

Folded Cascode Operational Amplifier

→ the simplified version (without bias circuitry)

- * two basic blocks:
 - p-channel input folded cascode
 - cascode p-cs
- * four bias b/c:
 - Vbias1
 - Vbias2
 - Vbias3
 - Vbias4

→ more simplified version

* which leads to the first design step: determine the currents to I1, I2

Design (5/20) - Folded Cascode1 *

DC param:

Vbias2	0.85000 V
Vbias1	0.85000 V
Vbias4	0.85000 V
Vbias3	0.85000 V

Design (6/20) - Folded Cascode1 *

DC param:

Vbias2	-0.57500 V
Vbias1	1.88000 V
Vbias4	-0.32000 V
Vbias3	1.88000 V

Design (7/20) - Folded Cascode1 *

DC param:

Vbias2	-0.79400 V
Vbias1	1.5 V
Vbias4	-0.13000 V
Vbias3	1.5 V

Design (8/20) - Folded Cascode1 *

DC param:

Vbias2	-0.57500 V
Vbias1	1.88000 V
Vbias4	-0.32000 V
Vbias3	1.88000 V

Design (9/20) - Folded Cascode1 *

DC param:

Vbias2	-0.57500 V
Vbias1	1.88000 V
Vbias4	-0.32000 V
Vbias3	1.88000 V

Design (10/20) - Folded Cascode1 *

Folded Cascode Op Amp frequency analysis

L_dom	0.00010414 MHz	PM	89.414 °
L_random	103.352 MHz		
L_GBW	1.88553 MHz		
C1	0 pF		

Design (11/20) - Folded Cascode1 *

summary | noise | mismatch | total

$A = \frac{g_m}{g_{cs} + g_{c2}}$

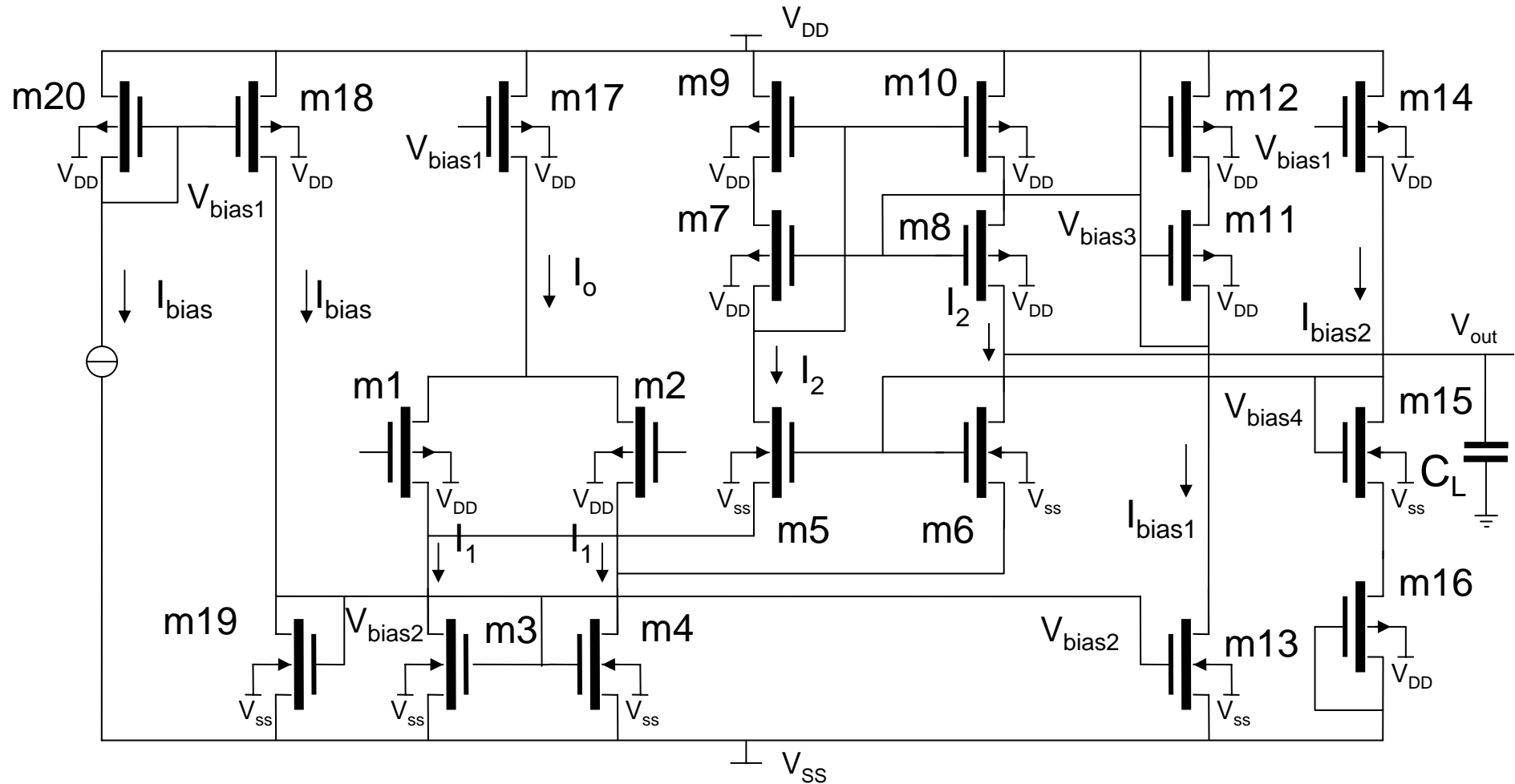
$A_{dom} = \frac{g_m}{g_{cs} + g_{c2}}$

$A_{rand} = \frac{g_m}{g_{cs} + g_{c2}}$

$CMR^* = PM - PM_{dom} + PM_{rand}$

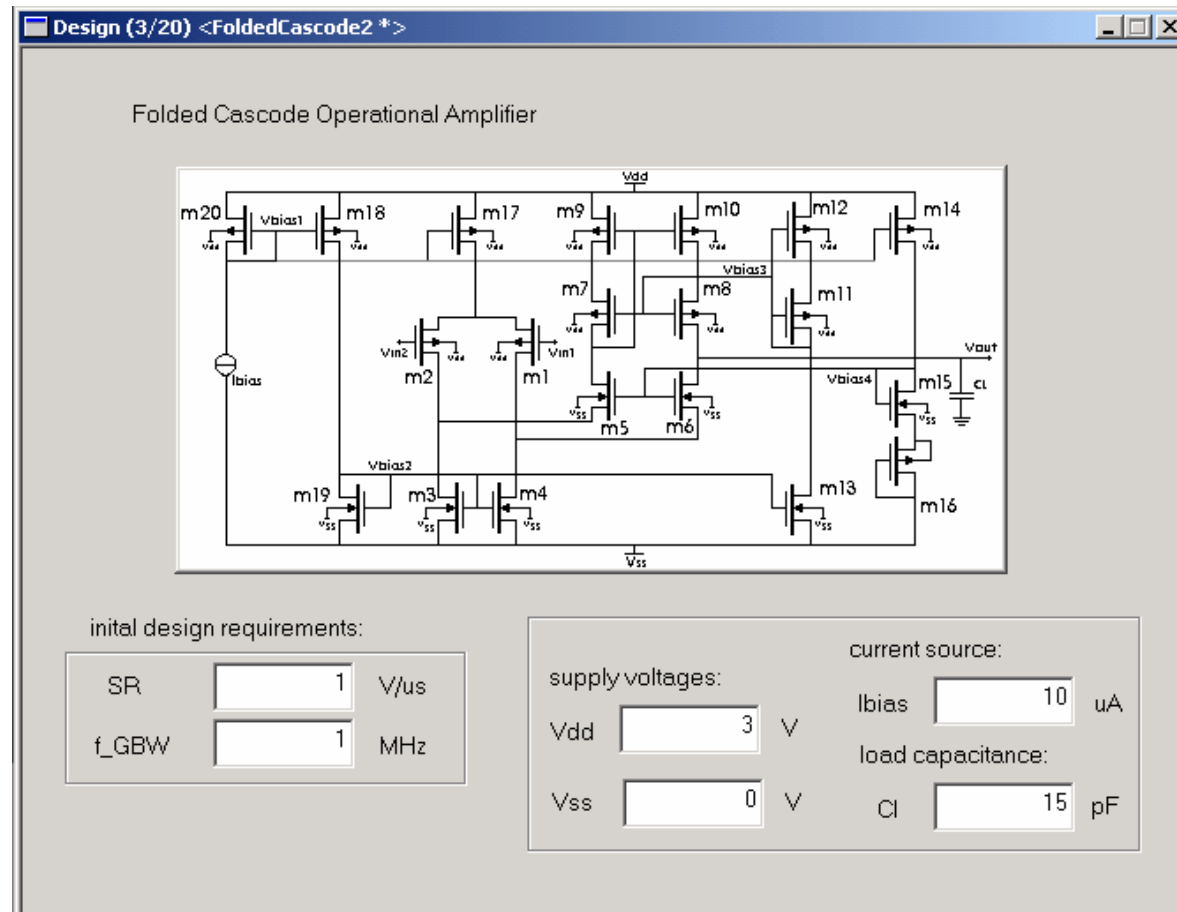
$V_{sw}^{FWTDR} = V_{DD} - V_{L1} - (I_{D1,sw} + I_{D2,sw} + I_{D3,sw} + I_{D4,sw})$

Procedural Design of Folded Cascode OTA



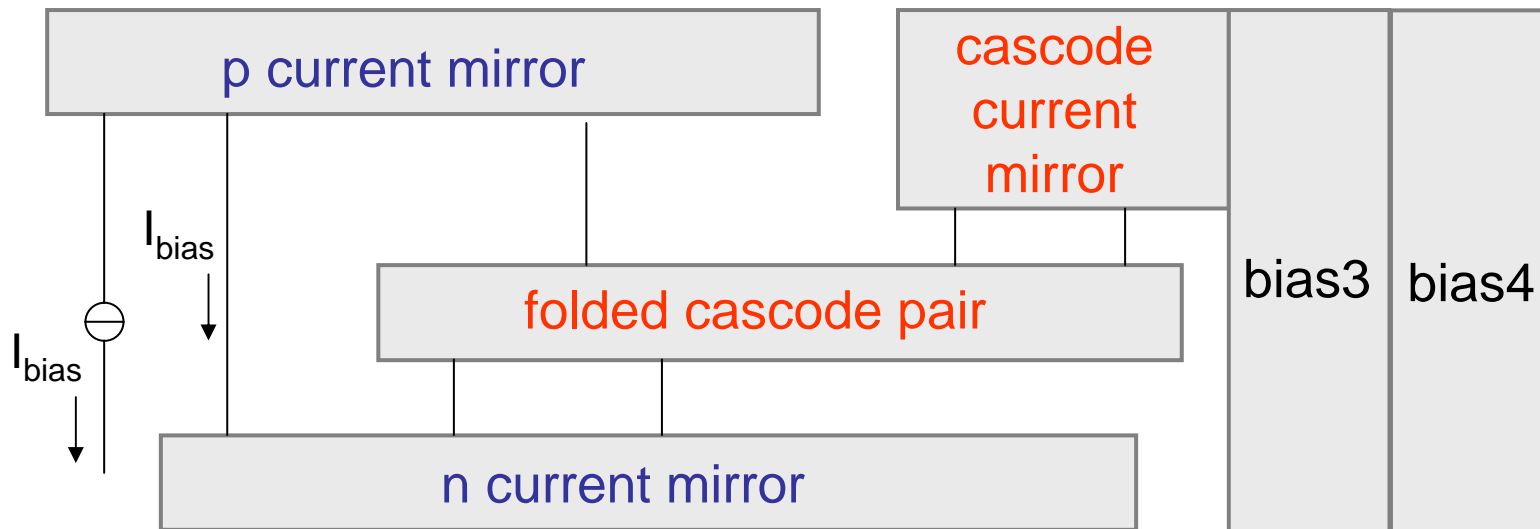
PAD Design Flow

Initialisation :



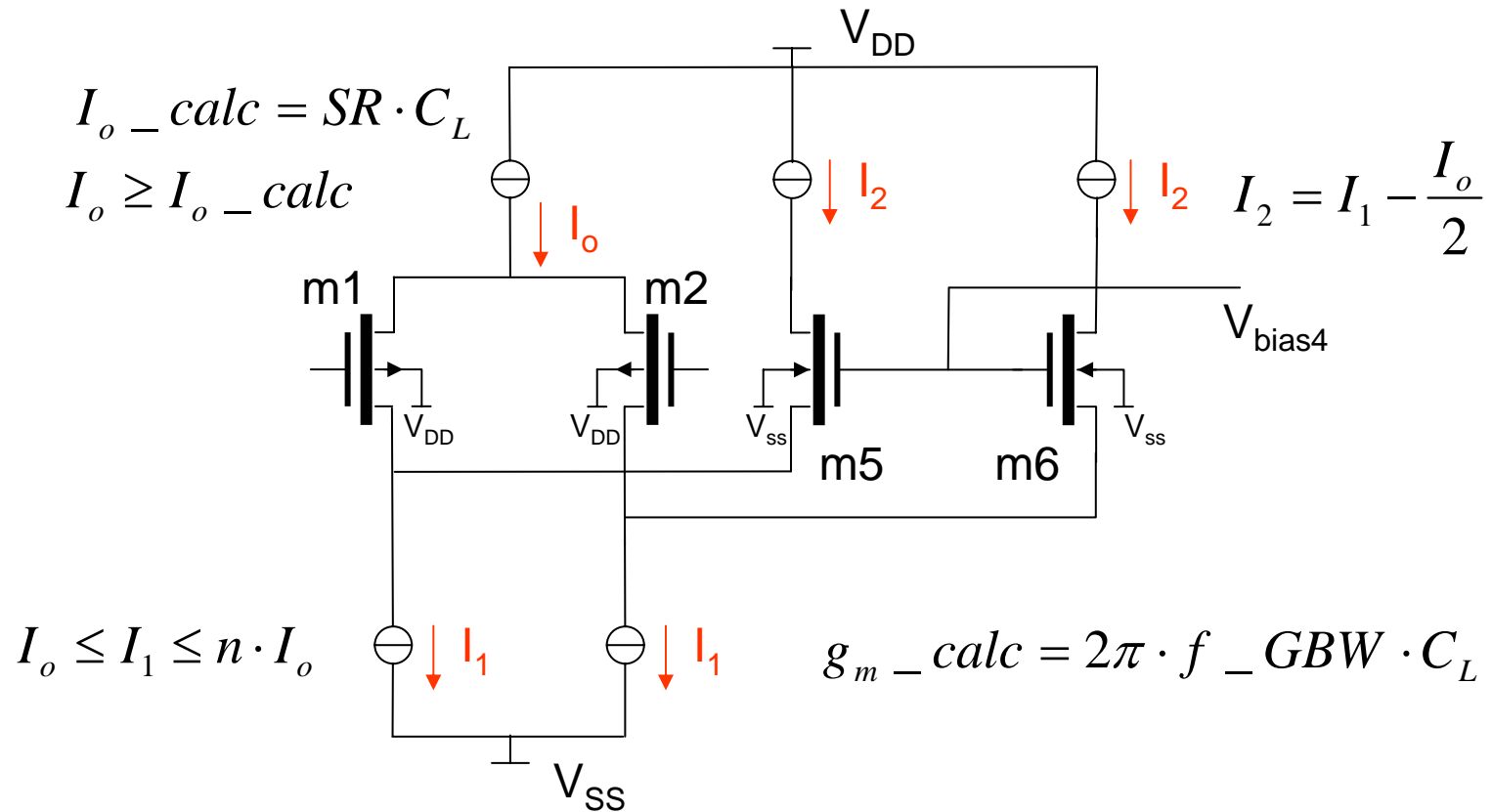
PAD Design Flow

Circuit partitioning :



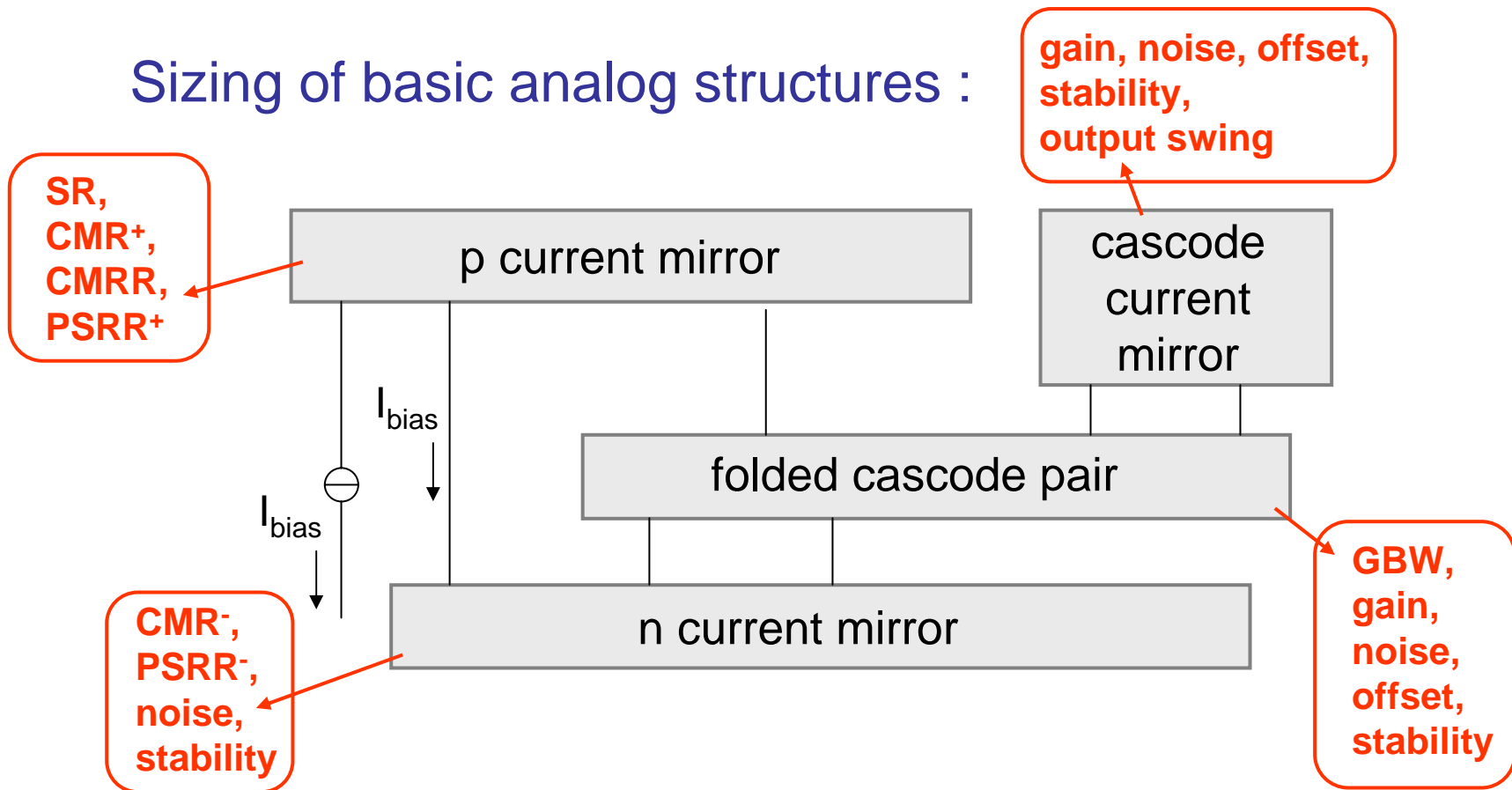
PAD Design Flow

Determination of circuit currents :



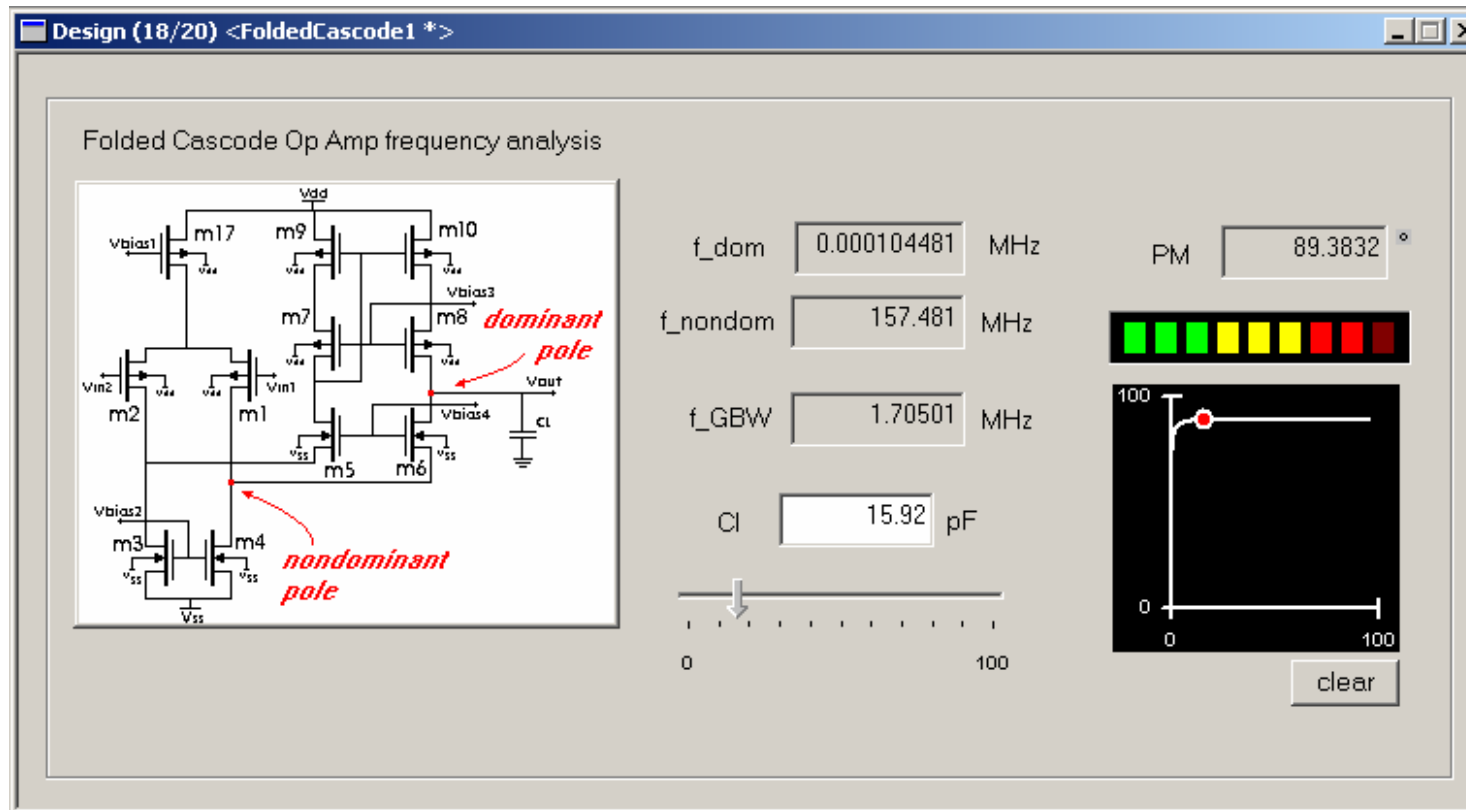
PAD Design Flow

Sizing of basic analog structures :



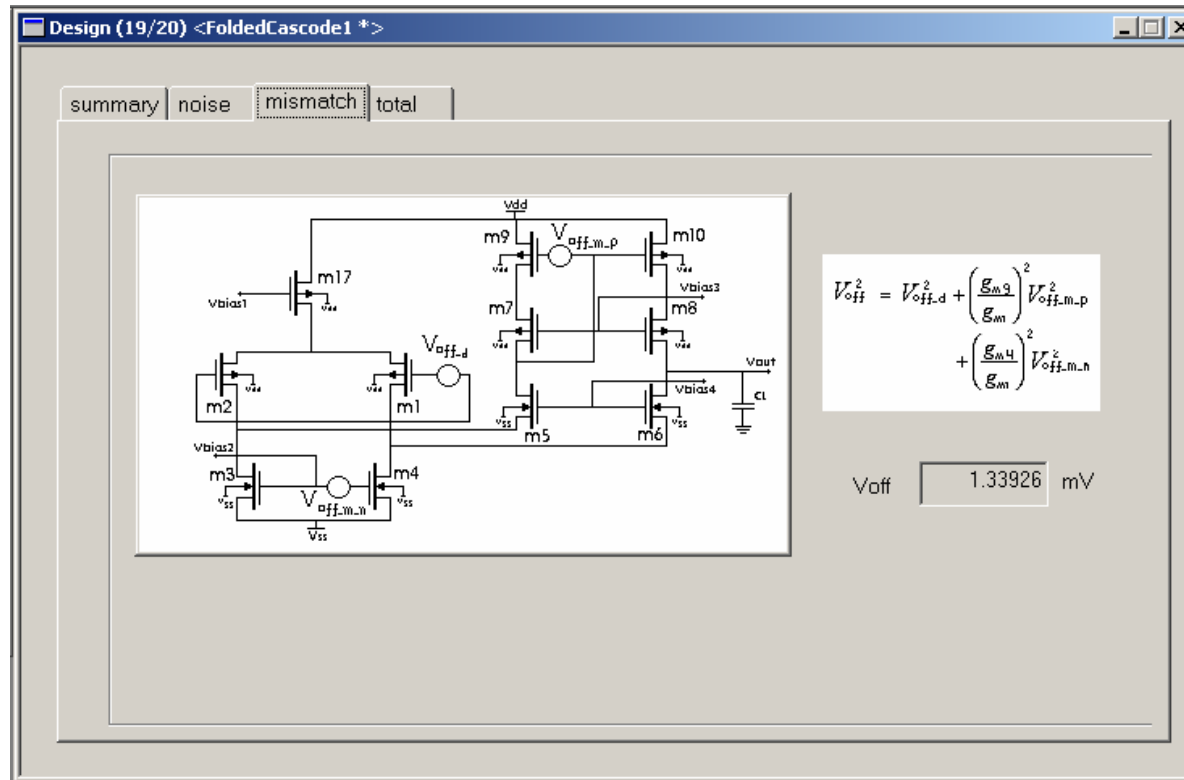
PAD Design Flow

Circuit level design :



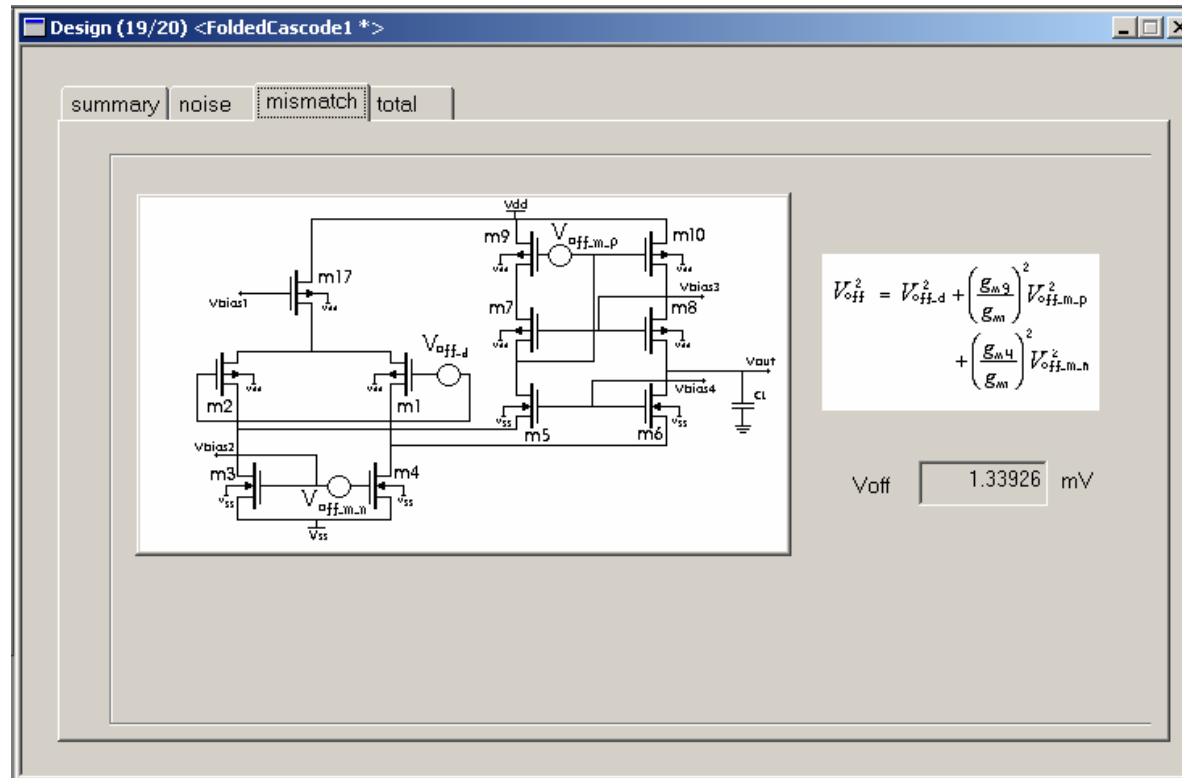
PAD Design Flow

Circuit level design :



PAD Design Flow

Circuit level design :



PAD Design Flow

Circuit level design :

The screenshot shows a circuit design tool window titled "Design (19/20) <FoldedCascode1 *>". It features a schematic of a folded cascode circuit with transistors labeled m1 through m17, biasing nodes (vbiass1-vbiass4), and input/output nodes (vin1, vin2, vout). The tool displays several performance metrics:

- Gain: $A = \frac{g_{m1}}{g_{ox} + g_{oy}}$ with a value of 84.2538 dB.
- Output conductance: $g_{ox} = \frac{g_{ds8} \cdot g_{ds10}}{g_{m8}}$
- Input conductance: $g_{oy} = \frac{g_{ds6} \cdot (g_{ds1} + g_{ds4})}{g_{m6}}$
- Common-mode range (CMR⁻): $CMR^- = V_{ss} + |V_{ds,sat4}| + |V_{ds,sat1}| - |V_{th1}|$ with a value of -0.246814 V.
- Common-mode range (CMR⁺): $CMR^+ = V_{dd} - |V_{th1}| - |V_{ds,sat17}|$ with a value of 1.50555 V.
- Output swing: $V_{out\ swing} = V_{dd} - V_{ss} - (|V_{ds,sat8}| + |V_{ds,sat10}| + |V_{ds,sat6}| + |V_{ds,sat4}|)$ with a value of 0.977565 V.

Conclusion

- new chart-based procedural analog design tool
- new knowledge-based analog design methodology
- design and re-design of wide range of circuits
- didactical tool that helps to hand analog knowledge towards non-expert designer



Download

<http://legwww.epfl.ch/CSL>

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