

Introduction to Reliability Simulation with EKV Device Model

Benoît Mongellaz

Laboratoire IXL

ENSEIRB - Université Bordeaux 1 - UMR CNRS 5818

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Motivation & Goal

- Introduced new activities to EKV modelling development
- Implemented Ageing/Reliability model into EKV
- Developed future experiments on advanced process to Design In Reliability
- Discussed technical needs to R&D works interfacing with industrial partners

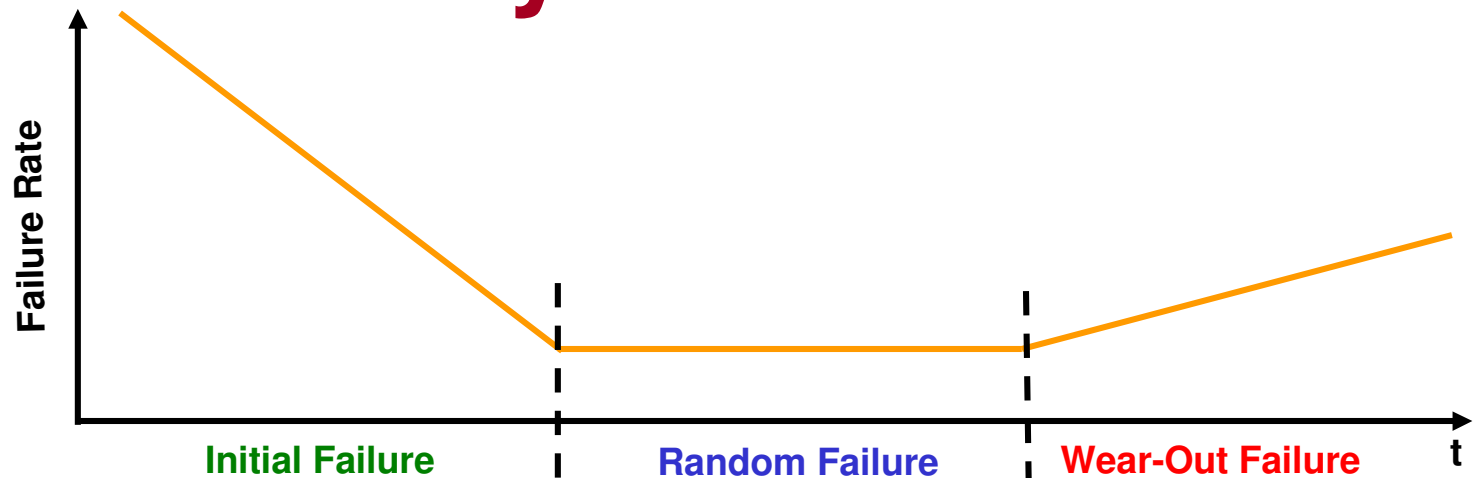
Context

- Reliability requirements are more and more important for advanced process (CMOS, HVMOS...)
- Shrunked devices are most sensitive to stresses induce loss of performance
- Reliability prediction from process qualification
- What are the method to take into account physic failure mode on IC performances and reliability?

Outline

- IC Reliability Prediction
- Reliability Simulation Tools
- EKV Reliability Model
- R&D Works

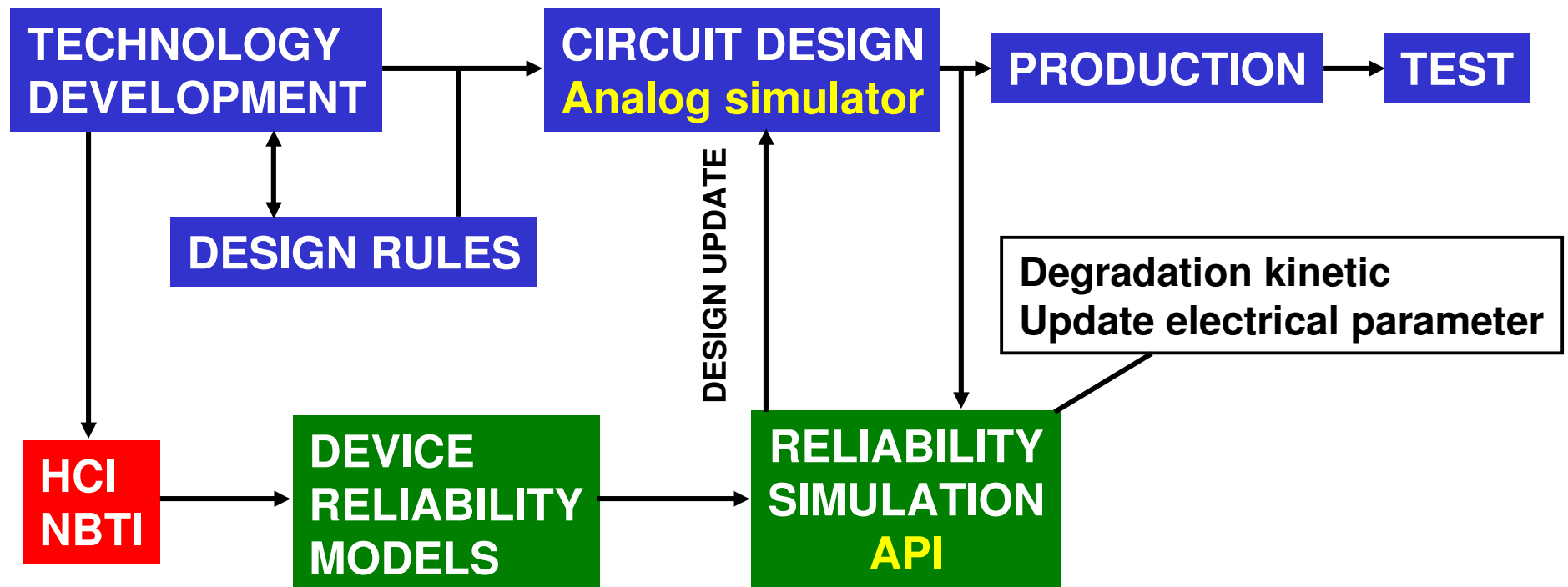
IC Reliability Prediction



Failure mechanism	Manufacturer	Customer	Market (end user)
ESD, Latch-up	←————→		
Oxide Film Destruction	←————→		
Electromigration			←————→
NBTI			←————→
HCI			←————→

- How to predict **NBTI** and **HCI** wear-out failures effects on IC performances?

IC Reliability Prediction



- Included external interface to take into account EKV reliability models

Outline

- Reliability Prediction
- Reliability Simulation Tools
 - Functionalities
- EKV Reliability Model
- R&D Works

Reliability Simulation Tools

Tool	Owner	Model	Simulator
BERT	UC Berkeley	HCIM , HCIB, TDDDB, EM, ESD, SEU,TDRE	SPICE
HOTRON	Texas Instrument	HCIM , EM, MS	SPICE
PRESS	Philips/MESA	HCIM , EM, ESD	PSTAR

HCIM = Hot-Carrier injection MOS ,

TDDDB = Time Dependent Dielectric Breakdown,

ESD = Electro-Static Discharge,

TDRE = Totale-Dose Radiation Effects,

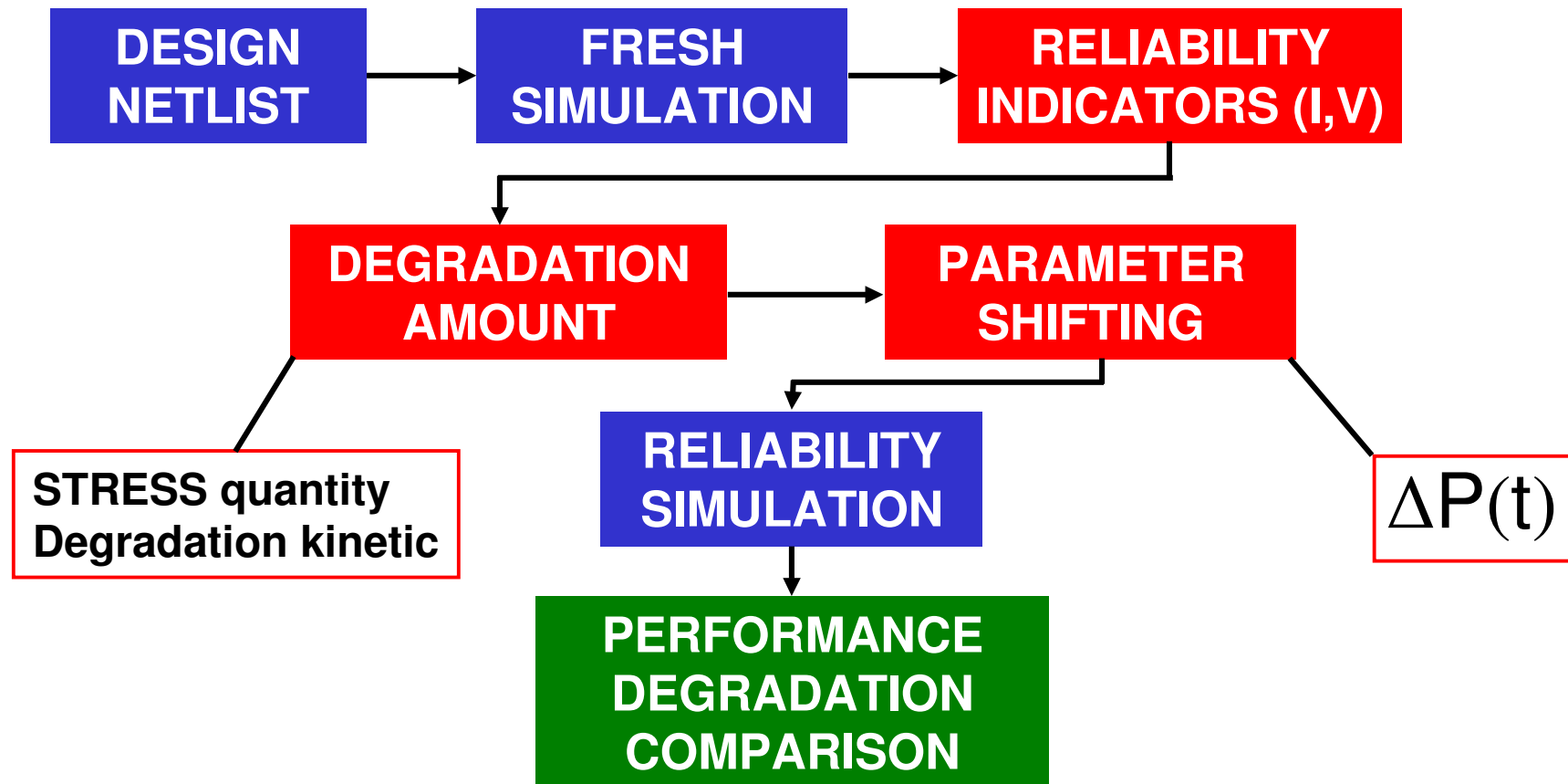
HCIB = Hot-Carrier injection Bipolar,

EM = Electromigration,

SEU = Single Event Upset,

MS = Mechanical Stress

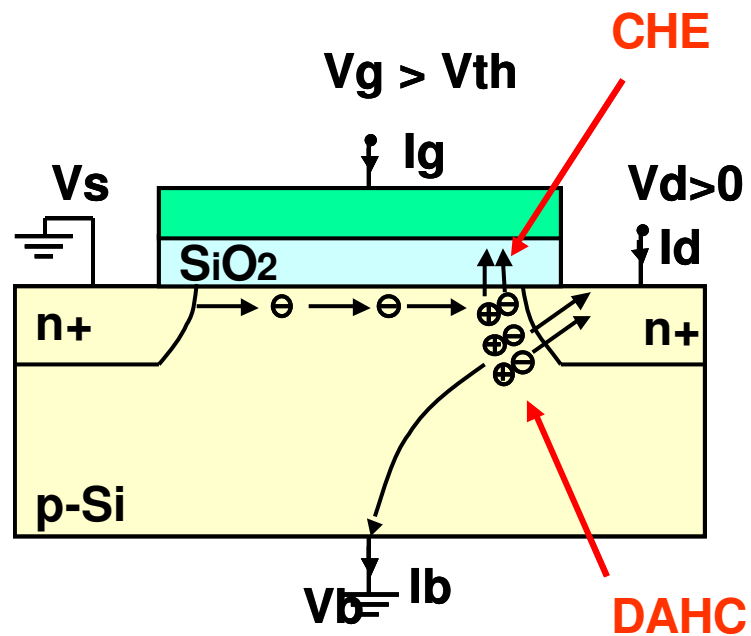
Reliability Simulation Tools



Outline

- Reliability Prediction
- Reliability Simulation Tools
- EKV Reliability Model
 - A Wear-Out Failure : Hot-Carrier Injection
- R&D Works

Hot-Carrier Injection



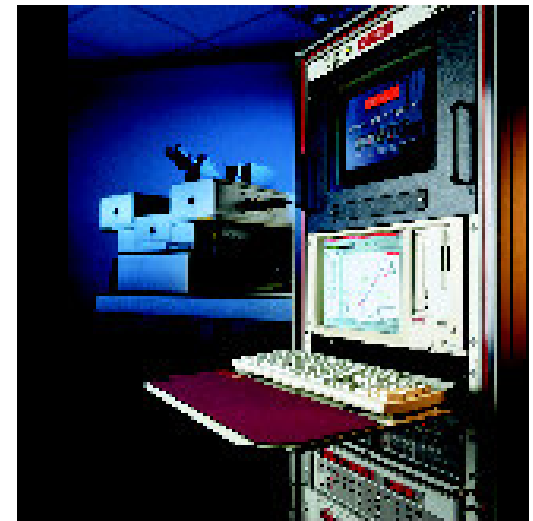
- Injection mechanism
 - **CHE** : Channel Hot Electron
 - **DAHC** : Drain Avalanche Hot Carrier
- Effects :
 - Electrical parameter shifting
 - Reduce device lifetime
 - Loss of performance
- Reliability indicators :
 - Substrate current I_b
 - Gate current I_g
 - Drain-source voltage V_d

Outline

- Reliability Prediction
- Reliability Simulation Tools
- EKV Reliability Model
 - Operational device lifetime
 - Electrical parameter shifting
- R&D Works

EKV Reliability Models

- JEDEC standard method [1]
 - I-V characterization
- Taken into account degradation criteria :
 - 100 mV threshold voltage shift
 - 10 % gm variation
 - 5 % linear or saturation current
- Used indicators to device lifetime :
 - V_{ds} , I_b , I_g
- Extracted parameter shifting model versus ageing time



Operational Device Lifetime

- Takeda model [2]
 - drain-source voltage method

$$\tau = t_0 \exp\left(\frac{B}{V_{DS}}\right)$$

- Hu model [3]
 - substrate current method
 - gate current method

$$\tau = \frac{HW}{I_{DS}} \left(\frac{I_B}{I_{DS}}\right)^m$$

$$\tau = k \left(\frac{I_G}{W}\right)^m$$

Electrical Parameter Shifting

- Evaluated device performance degradation
- Depend on the stress applied to device
- Taken into account effects of gradually changing bias condition

- The amount of degradation : $\text{stress}(T) = \frac{1}{T} \int_0^T \tau(t) dt$

Electrical Parameter Shifting

- The parameter time evolution : $P(t)=P_0(0)+\Delta P(t)$
- The parameter shifting models :
 - Power law [2] : $\Delta P(t)=A(\text{stress}(t))^n$
 - Logarithmic law [4] : $\Delta P(t)=B(\ln(1+C\text{stress}(t)))^n$
 - Exponential law [5] : $\Delta P(t)=D\exp(E\text{stress}(t)^n)$

What are the needs?

- Use EKV 3.0 release
 - Substrate, gate currents are defined
- Do I-V and reliability experiments
 - Calibrate EKV electrical model
 - Define the degradation trend of each electrical parameter (V_{T0} , KP , $LAMBDA$...) to build reliability models
- Use EKV device model is a key point thanks to a minimum set of parameters

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R&D Future Works

- Collaboration with industrial partners
- Target process : CMOS, HVMOS...
- Access to device samples and IC demonstrators
 - Digital blocks and analog blocks
- Develop WLR process qualification experiments at LEG/EPFL Laboratory
- Build EKV reliability models
- Include EKV model in a reliability simulation tool

Reference

- [1] JEDEC standard JESD-28, "*A procedure for measuring N-Channel MOSFET hot carrier induced degradation at maximum substrate current*", June 1995.
- [2] E. Takeda, N. Suzuki, "*An Empirical Model for Device Degradation Due to Hot-Carrier Injection*", IEEE Electron Device Letters, vol. EDL-4, n°4, pp. 111-113, April 1983.
- [3] C. Hu and als, "*Hot-Electron Induced MOSFET Degradation Model, Monitor and Improvement*", IEEE J. Of Solid-State Circuits, vol. SC-20, pp. 295-305, February 1985.
- [4] D. R. Wolters and als « *Trapping of Hot Electrons* ", Proc. 6th INFOS, 1989.
- [5] B. Marchand and als, « *A New Hot Carrier Degradation law for MOSFET Lifetime Prediction* ", Microelectronics Reliability, 1998, 1103-1107.