EKV Users’ Meeting/Workshop

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EKV3.0 model code & parameter extraction

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Outline

- EKV3.0 Verilog-A code
- Phenomena covered
- Parameter extraction methodology
- Illustration of model characteristics
- Summary

The Verilog-A code at a glance

- The Verilog-A code of EKV3.0
  - Contained in one file “ekv3.va”
  - ~1400 lines (46KB)
  - ~50 intrinsic model parameters
  - BSIM4-like junction diode models & effects
  - Optional source/drain, gate, substrate resistors
  - Developed using ELDO and SPECTRE
  - Used as the reference code for all model implementations
  - ADMS is being used in order to obtain “standard” C code versions for various simulators.

Verilog-A code vs. C code

- Verilog-A code of EKV3.0 has a brother in C code (ELDO)
    - Hand-coded for comparison with ADMS-created C code
    - C code allows implementation of advanced aspects (NQS, NQS noise)
    - Verilog-A and C codes otherwise have the same functionality
    - Writing Verilog-A code is simpler but code is less efficient (2-3 times slower than C).

Few, brief excerpts of the Verilog-A code of EKV3.0

1/2

```
module ekv3(d,g,s,b);
inout d,g,b,s;
electrical d,g,s,b;
electrical di,si,gi,bi;
```

Defining external and internal nodes of the module

```
parameter real p_cox = 0.012 from (0.0:inf);
parameter real p_xj = 20.0E-09 from (0.0:inf);
parameter real p_vto = 0.3 from (-inf:inf);
parameter real p_phi_f = 0.45 from [0.1:inf);
parameter real p_gamma_b = 0.3 from (0.0:inf);
parameter real p_gamma_g = 4.1 from (0.0:inf);
```

Defining parameters, default and acceptable values

```
if (f_x_res==1) begin
     VS=V(si,b); VD=V(di,b);
end
else begin
     VS=V(s,b);  VD=V(d,b);
end
```

Choosing to use the internal nodes or not

Few, brief excerpts of the Verilog-A code of EKV3.0

2/2

```
//RSCE
  Leff_o_LR = Leff/p_lr;
  one_lr = 1.0 - exp(-Leff_o_LR*Leff_o_LR);
  dvtrsce = 2.0*p_qlr*one_lr/(cox*Leff_o_LR*UT);
```

Calculating the ΔVT_{RSCE}

```
if (f_x_res==1) begin
     V(d ,di) <+ I(d,di)*rlx;
     V(s ,si) <+ I(s,si)*rlx;
     I(di,si) <+ IDS;
end else begin
     I(d ,s ) <+ IDS;
     V(di,b ) <+ 0.0; V(si,b) <+ 0.0;
end
```

Describing the external resistors. In case they are not used the internal nodes are grounded to bulk node.

```
I(b,g) <+ ddt(QB);
```

Describing the AC behaviour of the transistor. *QB is the charge related to the substrate node.*

Phenomena covered by EKV3.0 -- Associated parameters

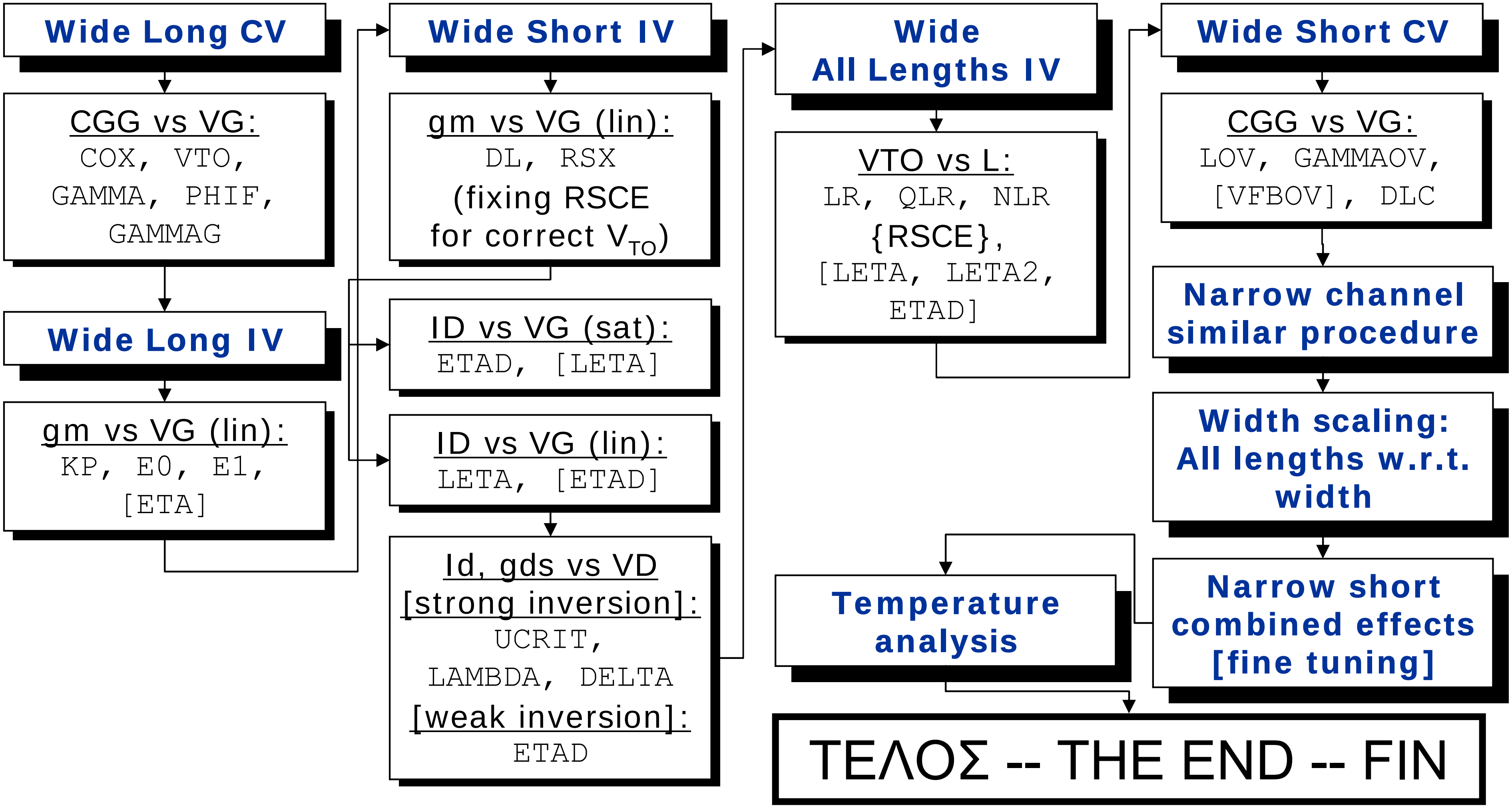
1/2

Modelled effect	Related parameters
Physical Modelling of Charges Including Accumulation Region Covering Polysilicon Depletion and Quantum mechanical effects	`COX(TOX), PHIF, GAMMA(NSUB), VTO(VFB), GAMMAG(NGATE)`
Bias-dependent Overlap Capacitances	`LOV, GAMMAOV(NOV), VFBOV`
Non-Uniform Vertical Doping	`GAMMA2, VR, DVR`
NQS (AC, noise)	`--`
Mobility (reduction due to vertical field effect) Covering: Surface Roughness, Phonon Scattering, Coulomb Scattering	`KP(U0), E0, E1, ETA` `ZC, THC`
Impact ionization current	`IBA, IBB, IBN`
Gate currents (IGS, IGD, IGB)	`KG, XB, UB`

Phenomena covered by EKV3.0 -- Associated parameters 2/2

Modelled effect	Related parameters
Longitudinal Field Effect Velocity Saturation, Channel Length Modulation	`UCRIT(VSAT), LAMBDA, DELTA`
Reverse Short Channel Effect	`LR, QLR, NLR`
Inverse Narrow Width Effect	`WR, QWR, NWR`
Drain Induced Barrier Lowering	`ETAD, SIGMAD`
Source and Drain Charge Sharing	`LETA, {LETA2}, WETA`
Geometrical effects, Width scaling	Various parameters (`DL, WQLR,` …)
Noise (Flicker / Thermal)	`AF, KF`
Temperature Effects	various parameters (7)
TOTAL	~60

Basic parameter extraction methodology



Wide Long CV

CGG vs VG:
COX, VTO,
GAMMA, PHIF,
GAMMAG

Wide Long IV

gm vs VG (lin):
KP, E0, E1,
[ETA]

Wide Short IV

gm vs VG (lin):
DL, RSX
(fixing RSCE
for correct V_{TO})

ID vs VG (sat):
ETAD, [LETA]

ID vs VG (lin):
LETA, [ETAD]

Id, gds vs VD
[strong inversion]:
UCRIT,
LAMBDA, DELTA
[weak inversion]:
ETAD

Wide
All Lengths IV

VTO vs L:
LR, QLR, NLR
{RSCE},
[LETA, LETA2,
ETAD]

Wide Short CV

CGG vs VG:
LOV, GAMMAOV,
[VFBOV], DLC

Narrow channel
similar procedure

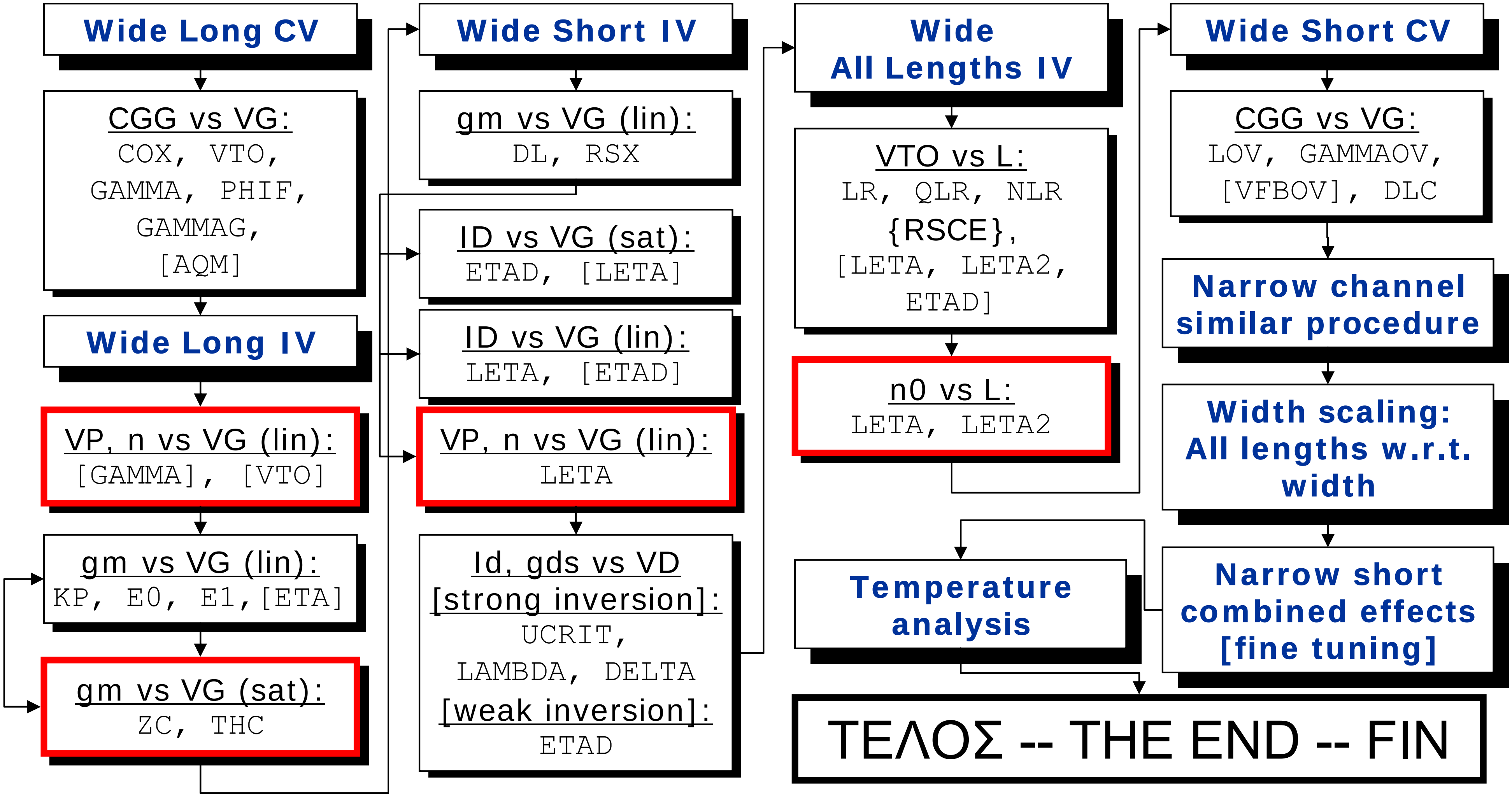
Width scaling:
All lengths w.r.t.
width

Narrow short
combined effects
[fine tuning]

Temperature
analysis

ΤΕΛΟΣ -- THE END -- FIN

Refined parameter extraction methodology



Wide Long CV

CGG vs VG:
COX, VTO,
GAMMA, PHIF,
GAMMAG,
[AQM]

Wide Long IV

VP, n vs VG (lin):
[GAMMA], [VTO]

gm vs VG (lin):
KP, E0, E1,[ETA]

gm vs VG (sat):
ZC, THC

Wide Short IV

gm vs VG (lin):
DL, RSX

ID vs VG (sat):
ETAD, [LETA]

ID vs VG (lin):
LETA, [ETAD]

VP, n vs VG (lin):
LETA

Id, gds vs VD
[strong inversion]:
UCRIT,
LAMBDA, DELTA
[weak inversion]:
ETAD

Wide All Lengths IV

VTO vs L:
LR, QLR, NLR
{RSCE},
[LETA, LETA2,
ETAD]

n0 vs L:
LETA, LETA2

Temperature analysis

Wide Short CV

CGG vs VG:
LOV, GAMMAOV,
[VFBOV], DLC

Narrow channel similar procedure

Width scaling: All lengths w.r.t. width

Narrow short combined effects [fine tuning]

ΤΕΛΟΣ -- THE END -- FIN

Example parameter set for 0.12µm CMOS

```
***General
+ COX = 12.25m
+ XJ = 20.0n
+ VTO = 225m
+ PHIF = 0.5
+ GAMMA = 0.25
+ GAMMAG = 14
+ N0 = 1.04
```

```
***QM [fine tuning]
+ AQM = 0.5
```

```
*** Mobility
+ KP = 524u
+ E0 = 10.0G
+ E1 = 380.0MEG
+ ETA = 1.8
+ ZC = 1.0
+ THC = 0
```

```
*** VSAT / CLM
+ UCRIT = 3.6MEG
+ LAMBDA = 0.2
+ DELTA = 1.65
```

```
*** Geometrical
+ DL = -23n
+ DW = -32n
+ WDL = 0
+ LDW = 1.5n
```

```
*** RSCE
+ LR = 55n
+ QLR = 2.8m
+ NLR = 150m
```

```
*** INWE
+ WR = 80n
+ QWR = 470u
+ NWR = 5.5m
```

```
*** Charge Sharing
+ LETA = 385m
+ LETA2 = 0
+ WETA = 450m
```

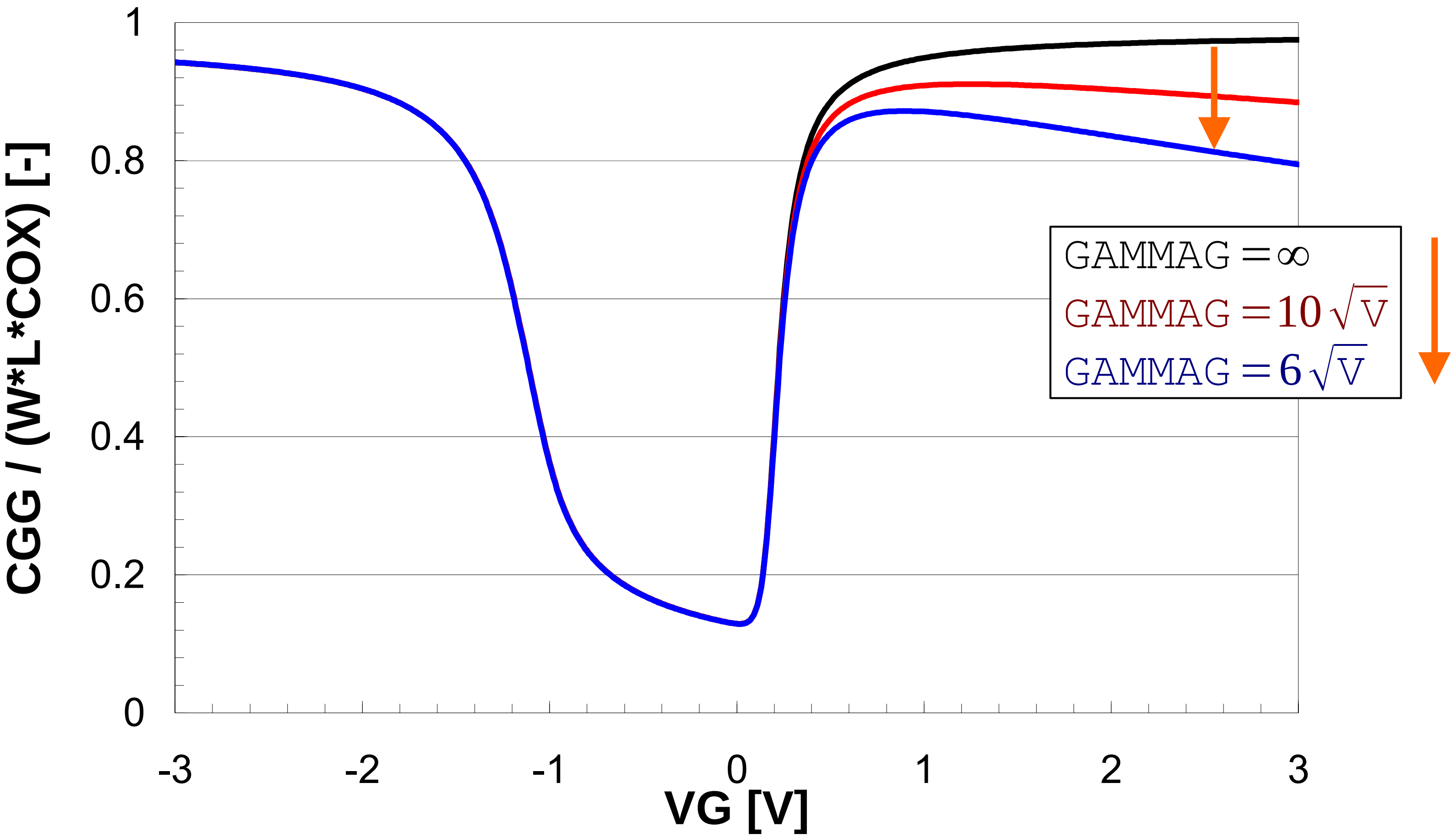
```
*** DIBL
+ ETAD  = 0.41
+ SIGMAD = 1
```

```
*** Temp params
+ TCV = 579u
+ BEX = -1.8
+ TETA = 6.25m
+ UCEX = 0.8
+ TLAMBDA = 0
+ TE0EX = -15
+ TE1EX = 1.5
```

```
*** Overlap Caps
+ LOV = 30.0n
+ GAMMAOV = 2.5
+ VFBOV = 250m
```

Polysilicon depletion effect

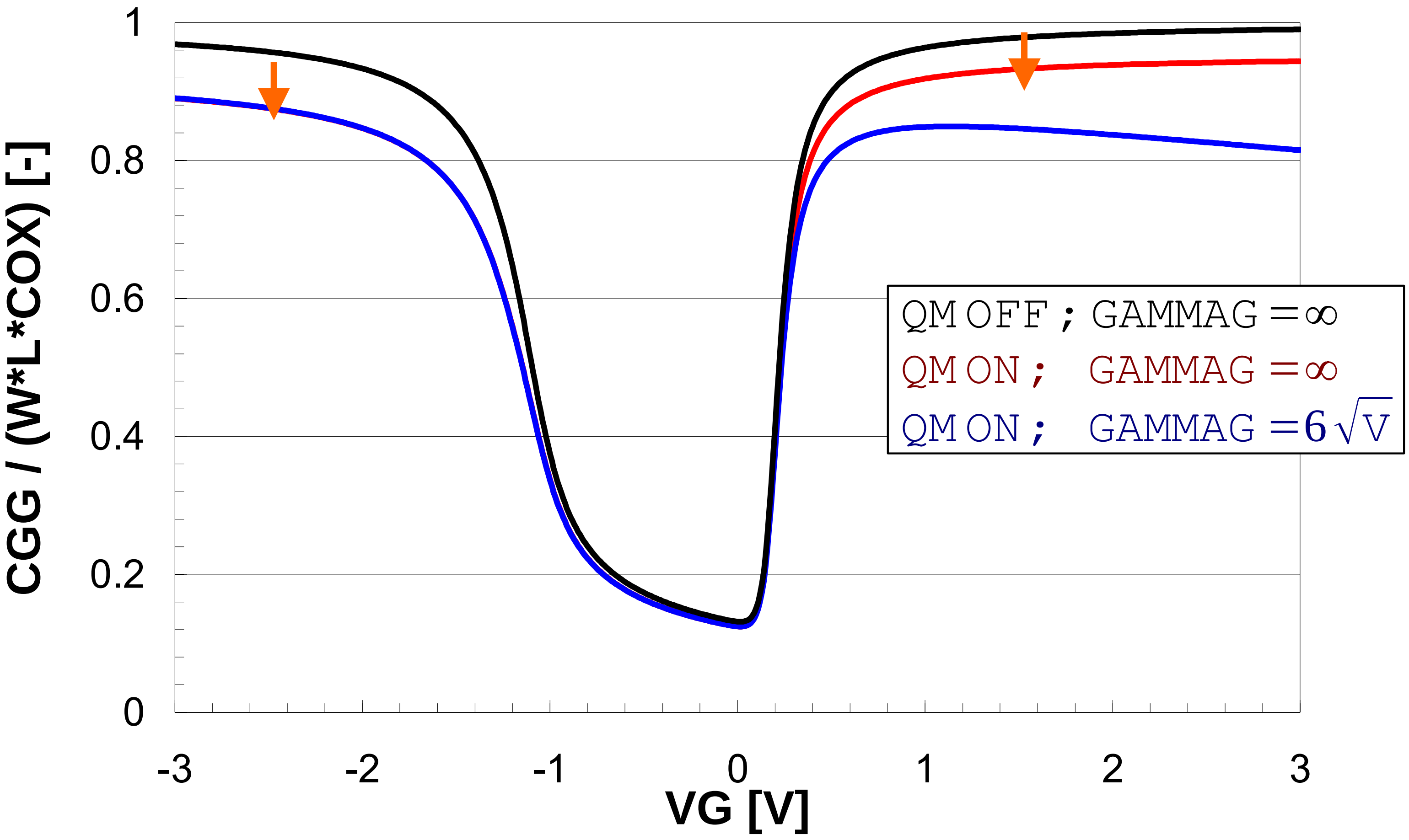
GAMMAG



nmos
W=10u
L=10u

Quantum mechanical effect

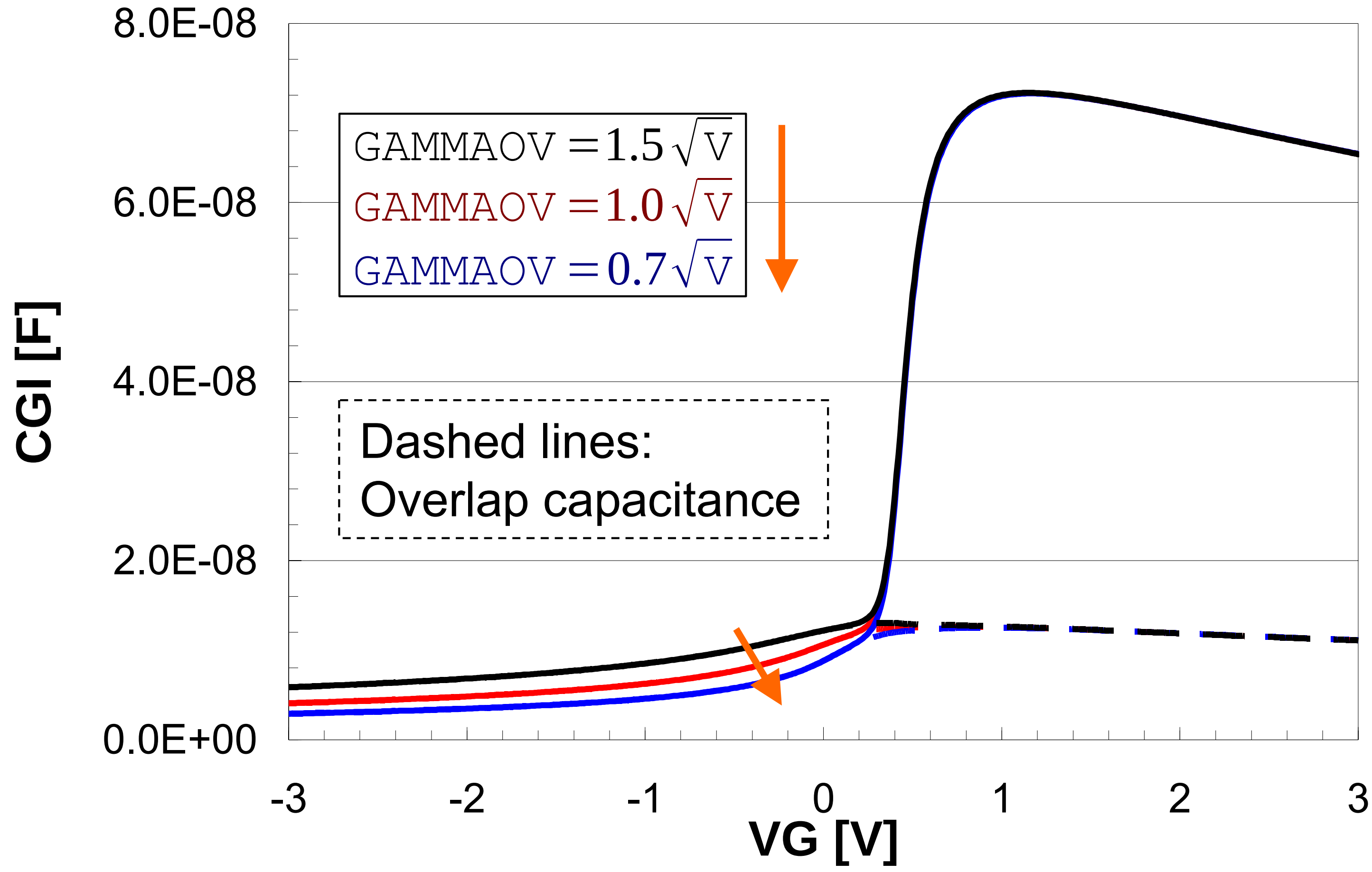
AQM



nmos
W=10u
L=10u

Overlap Capacitance

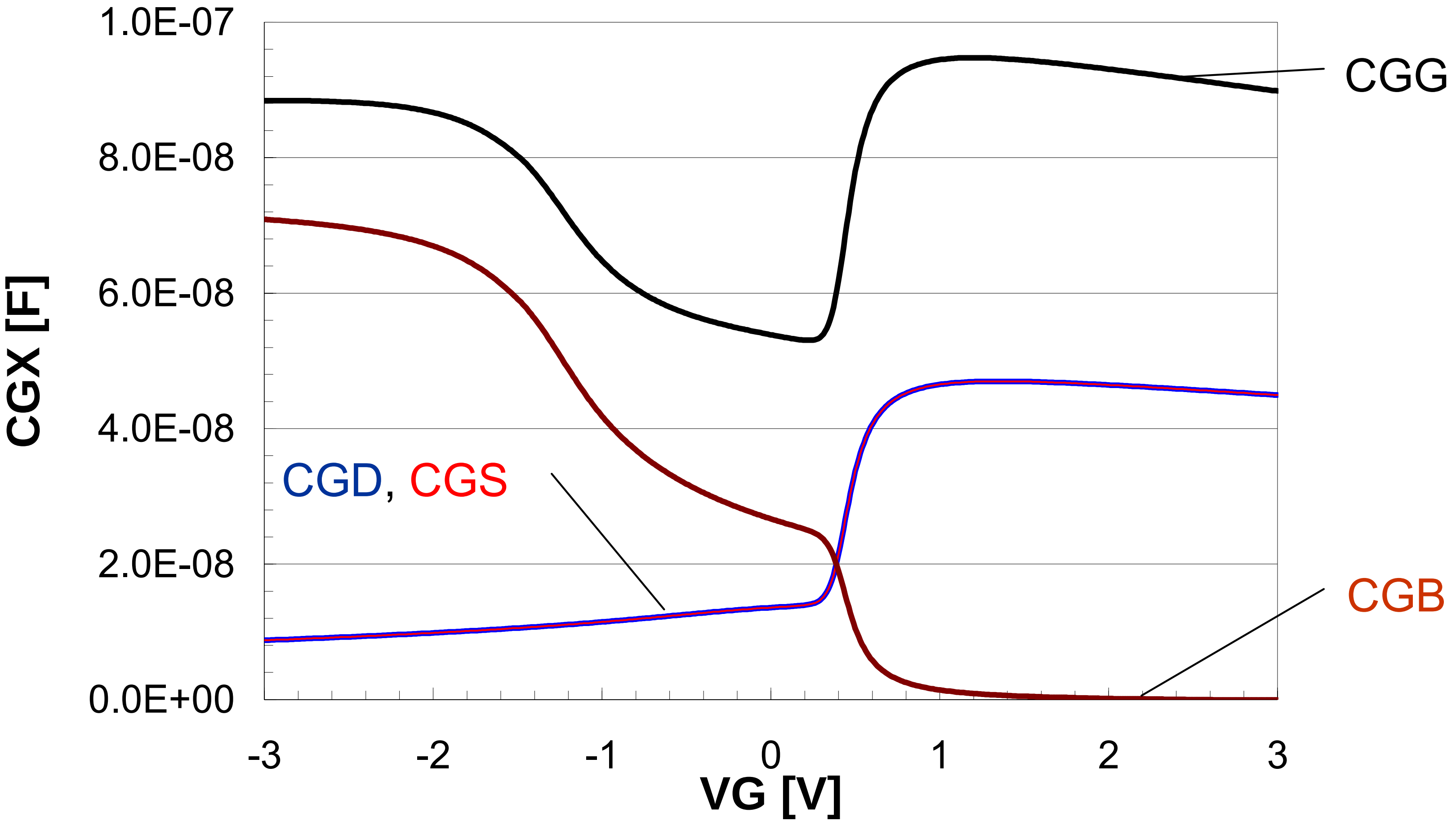
GAMMAOV



Dashed lines:
Overlap capacitance

nmos
W=10u
L=120n

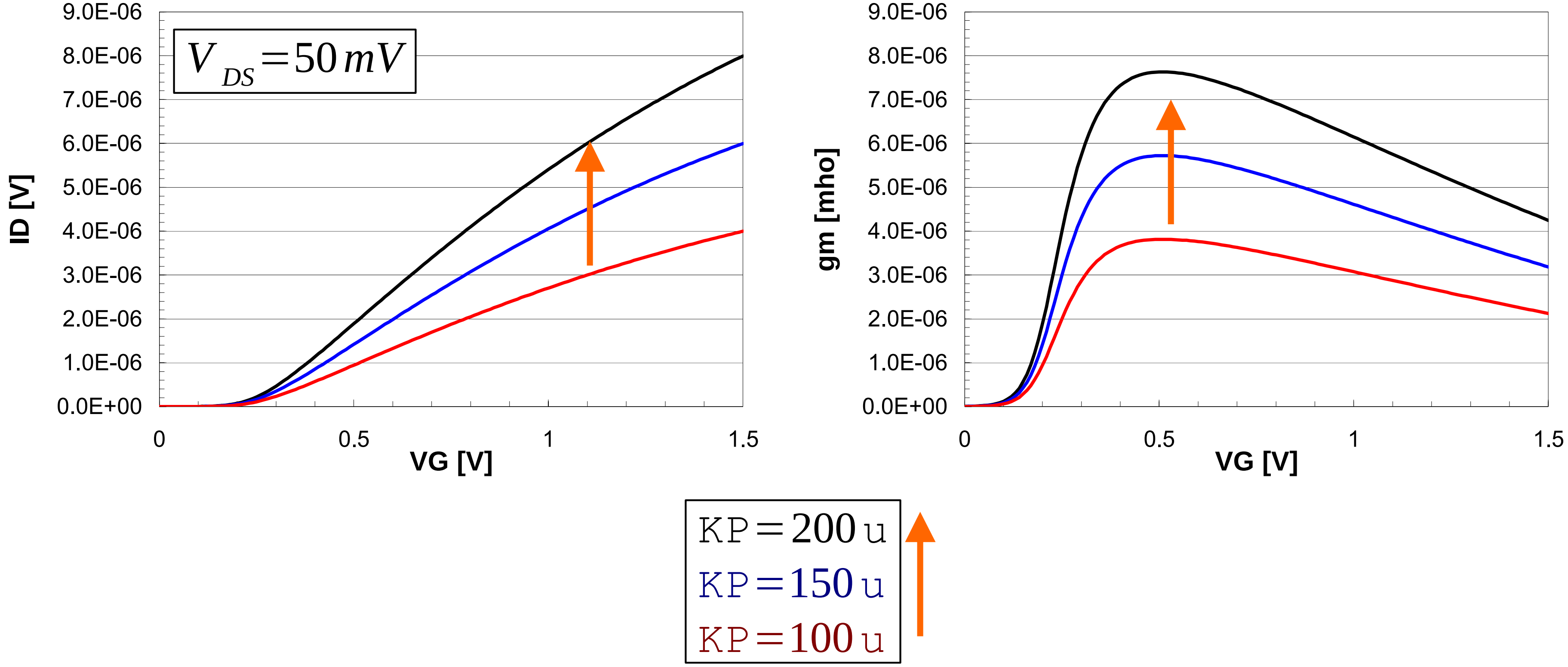
Short-channel CV



nmos
W=10u
L=120n

Transconductance factor

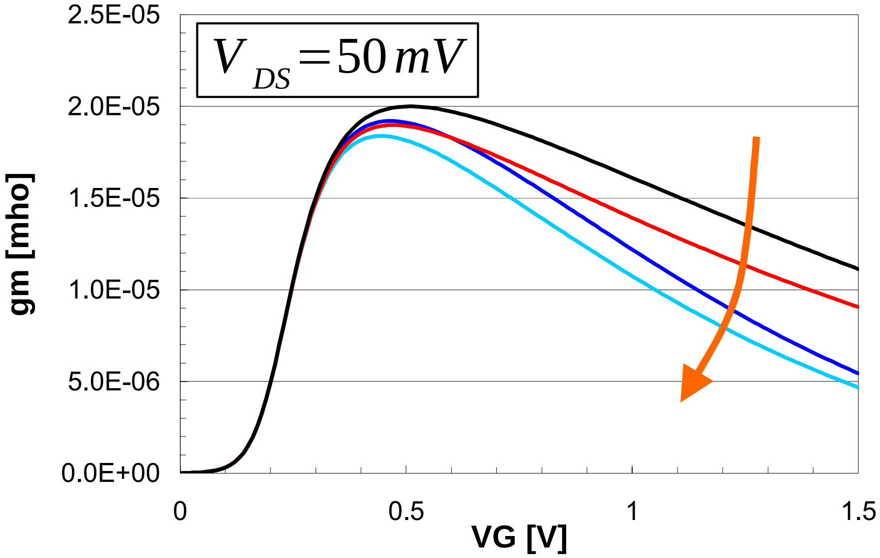
KP

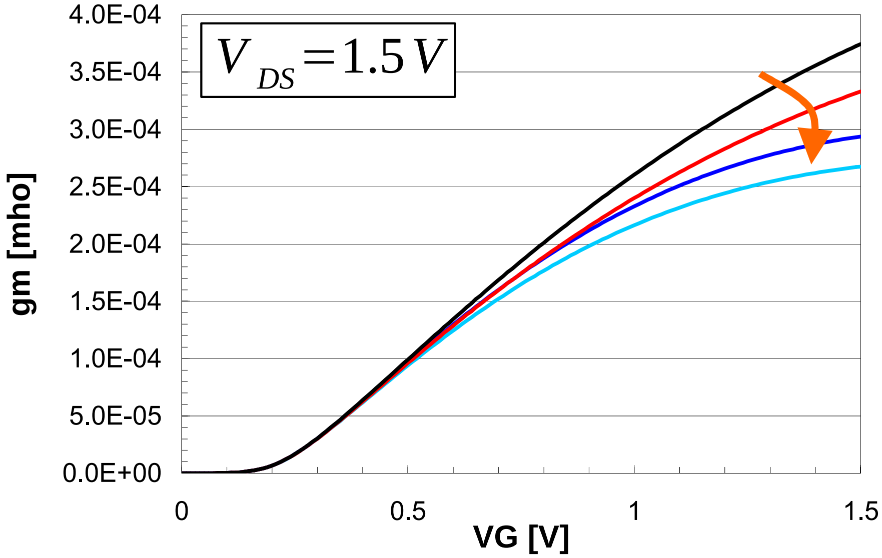


nmos
W=10u
L=10u

Mobility reduction due to vertical field

E0, E1, [ETA]





E0=1G; E1=600M
E0=600M; E1=600M
E0=1G; E1=400M
E0=600M; E1=400M

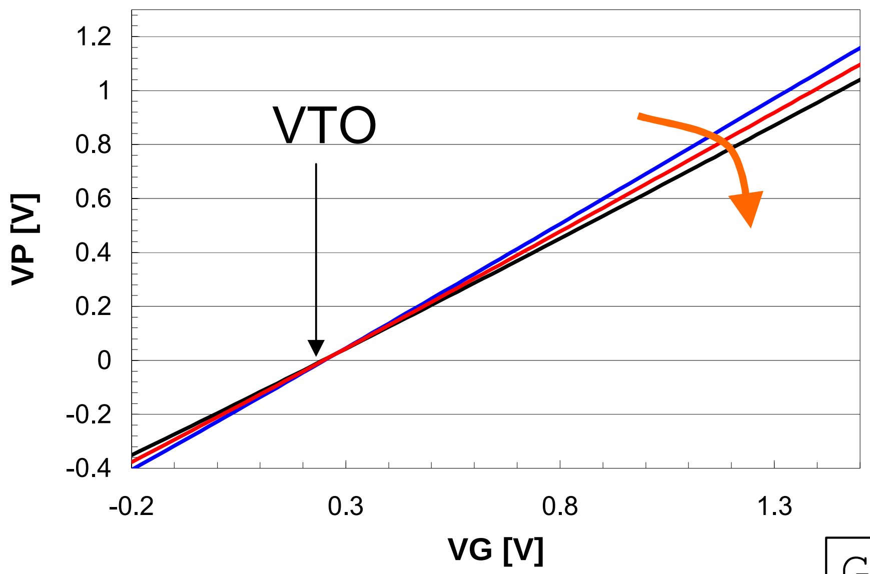
$$\mu = \frac{\mu_0}{1 + \frac{E_\perp}{E_0} + \left(\frac{E_\perp}{E_1}\right)^2}$$

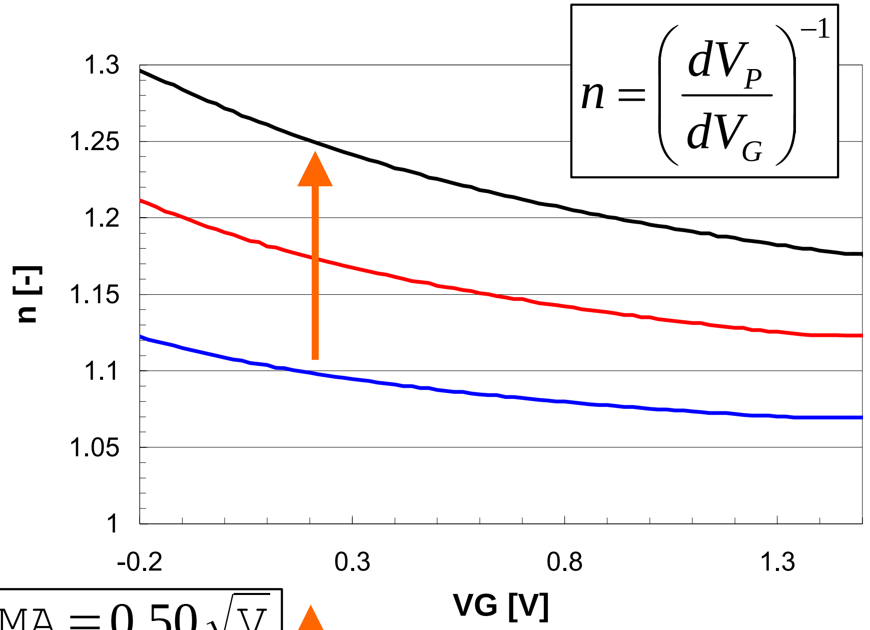
$$E_\perp = \frac{Q_i + \eta Q_b}{C_{OX}}$$

nmos
W=10u
L=10u

Pinch-off voltage & slope factor

GAMMA



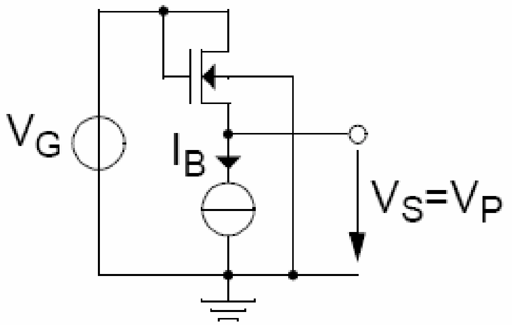


$$n = \left(\frac{dV_P}{dV_G} \right)^{-1}$$

$\mathrm{GAMMA} = 0.50\sqrt{\mathrm{V}}$

$\mathrm{GAMMA} = 0.35\sqrt{\mathrm{V}}$

$\mathrm{GAMMA} = 0.20\sqrt{\mathrm{V}}$



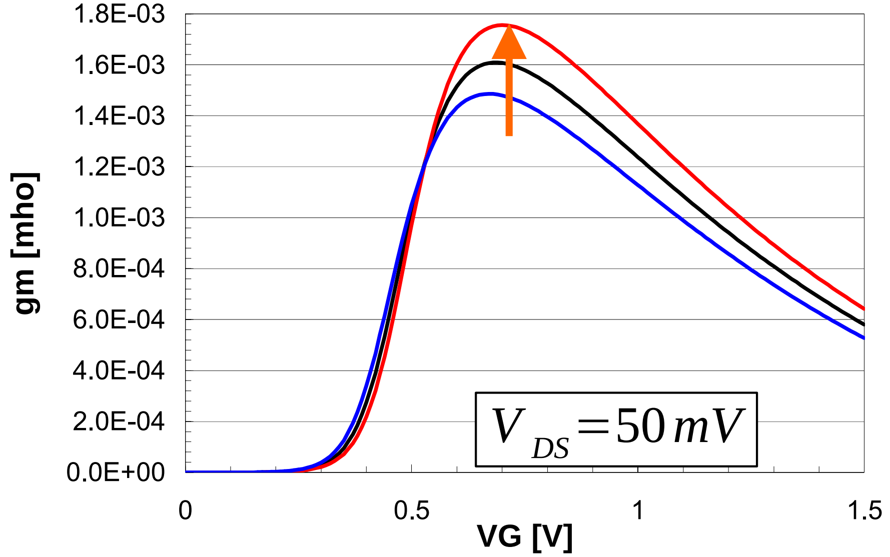
nmos
W=10u
L=10u

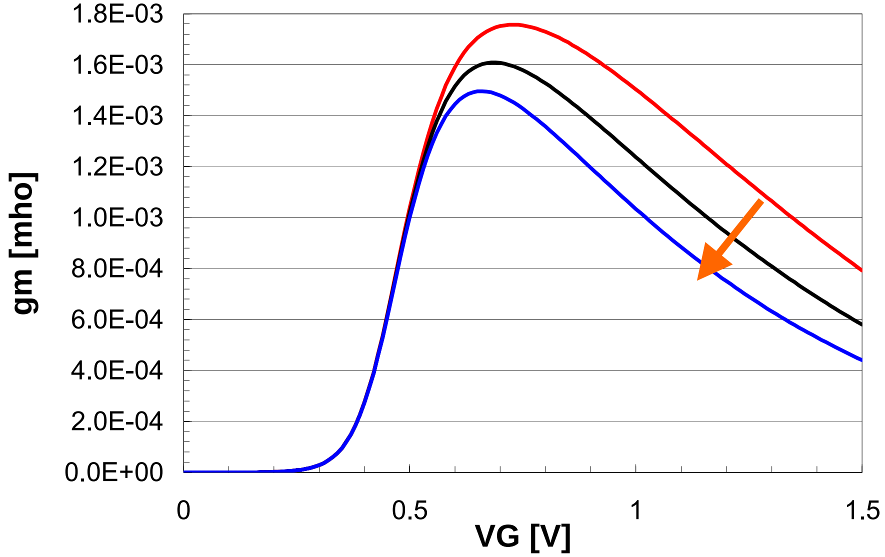
VP vs VG measurement setup.

**IB biases the device to moderate inversion*

Leff & series resistance effects

`DL, RS`





$$L_{eff} = L_{Drawn} + DL$$

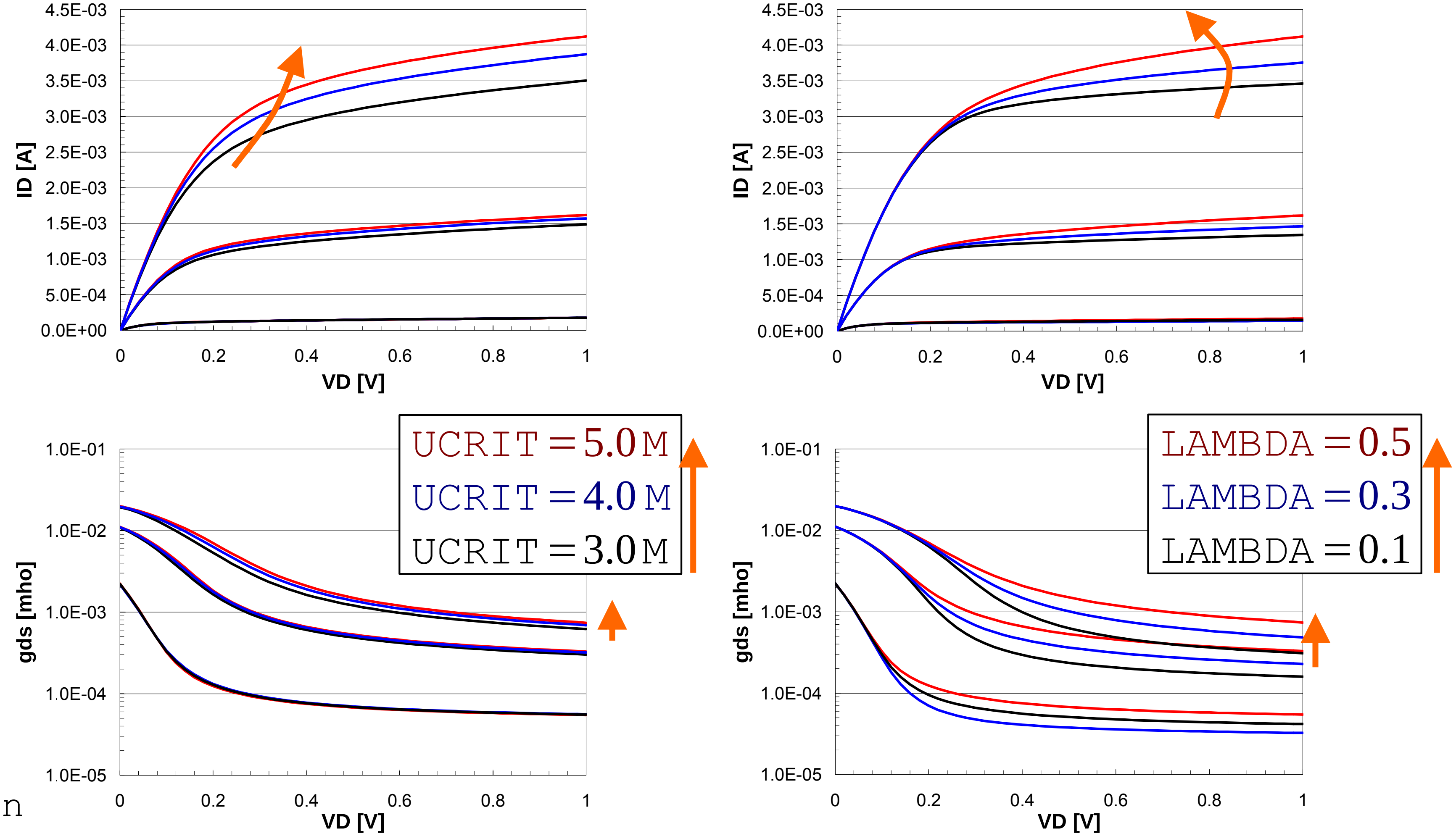
$\mathrm{DL} = -30\,\mathrm{n}$ ↑
$\mathrm{DL} = -20\,\mathrm{n}$
$\mathrm{DL} = -10\,\mathrm{n}$

$\mathrm{RS} = 00.0\,\mu\Omega\mathrm{m}$ ↓
$\mathrm{RS} = 30.0\,\mu\Omega\mathrm{m}$
$\mathrm{RS} = 60.0\,\mu\Omega\mathrm{m}$

```
nmos
W=10u
L=120n
```

Velocity saturation & CLM effects

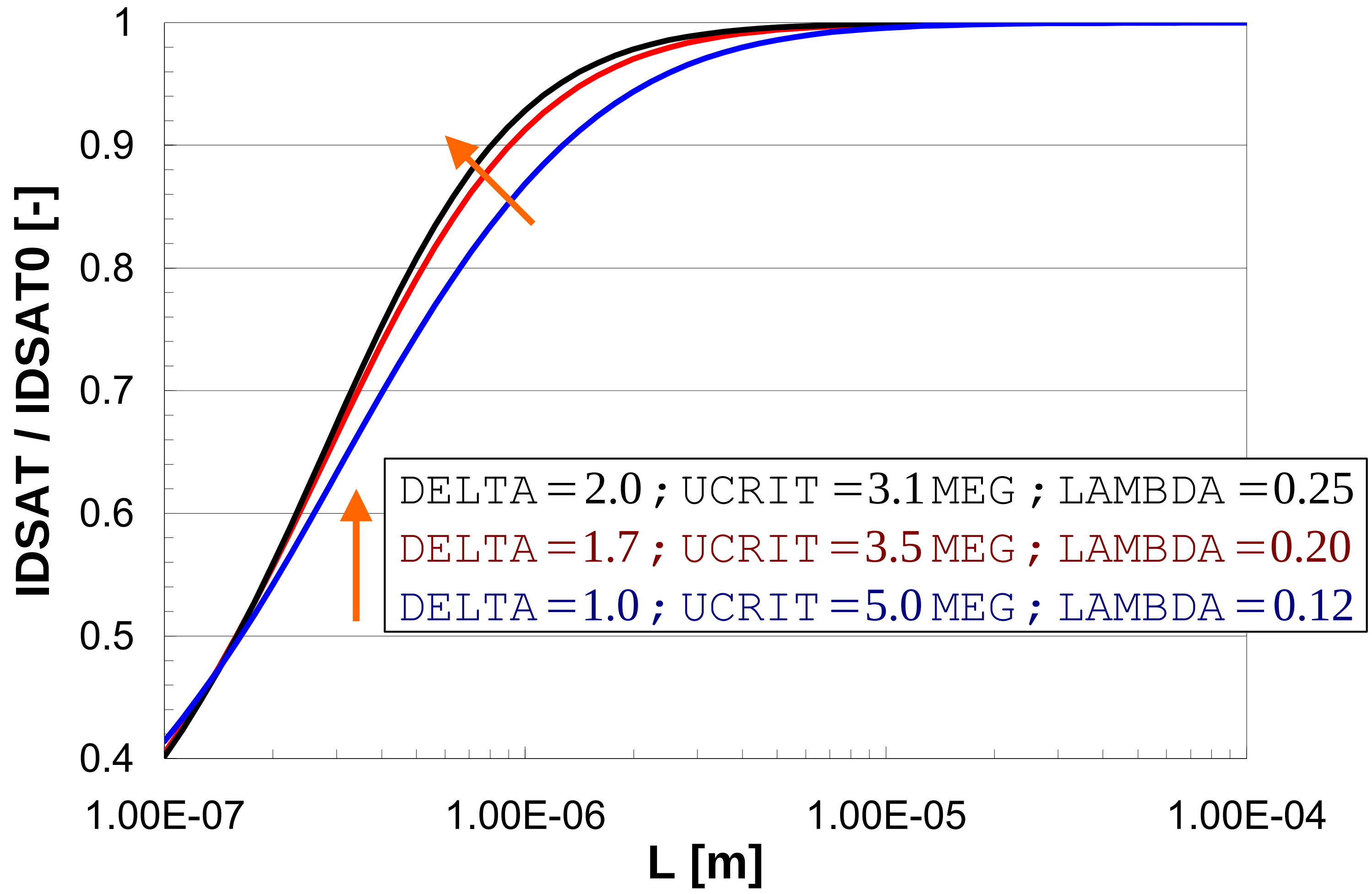
`LAMBDA, UCRIT`



nmos
W=10u
L=120n

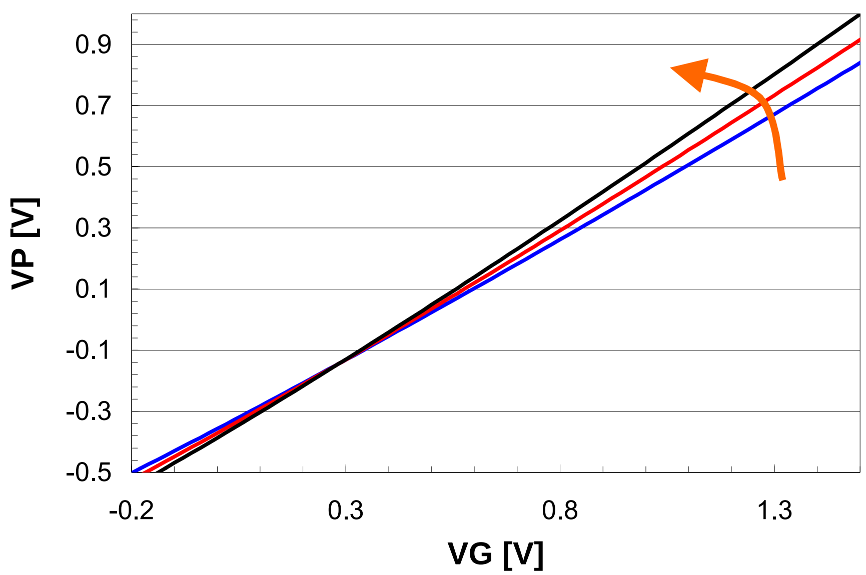
Scaling due velocity saturation

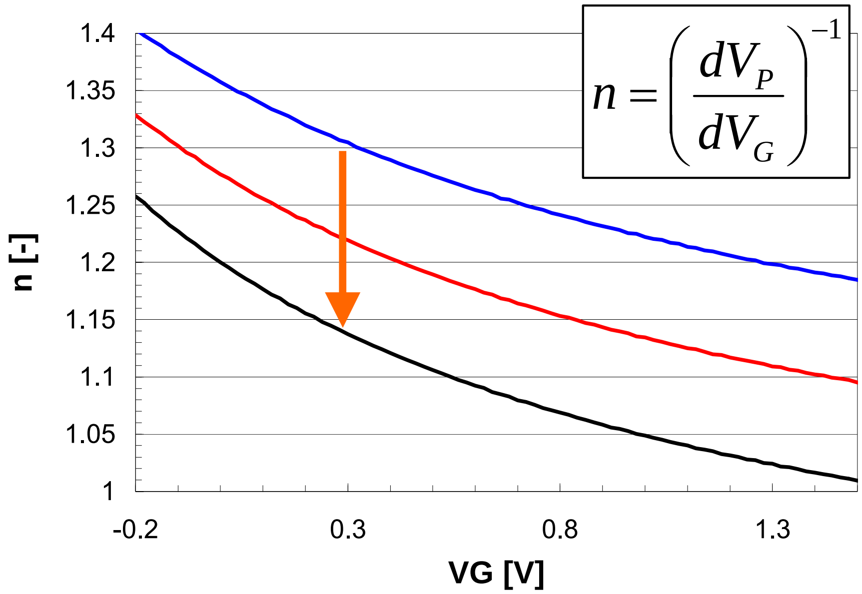
DELTA, UCRIT, LAMBDA



Pinch-off voltage & slope factor

`LETA`





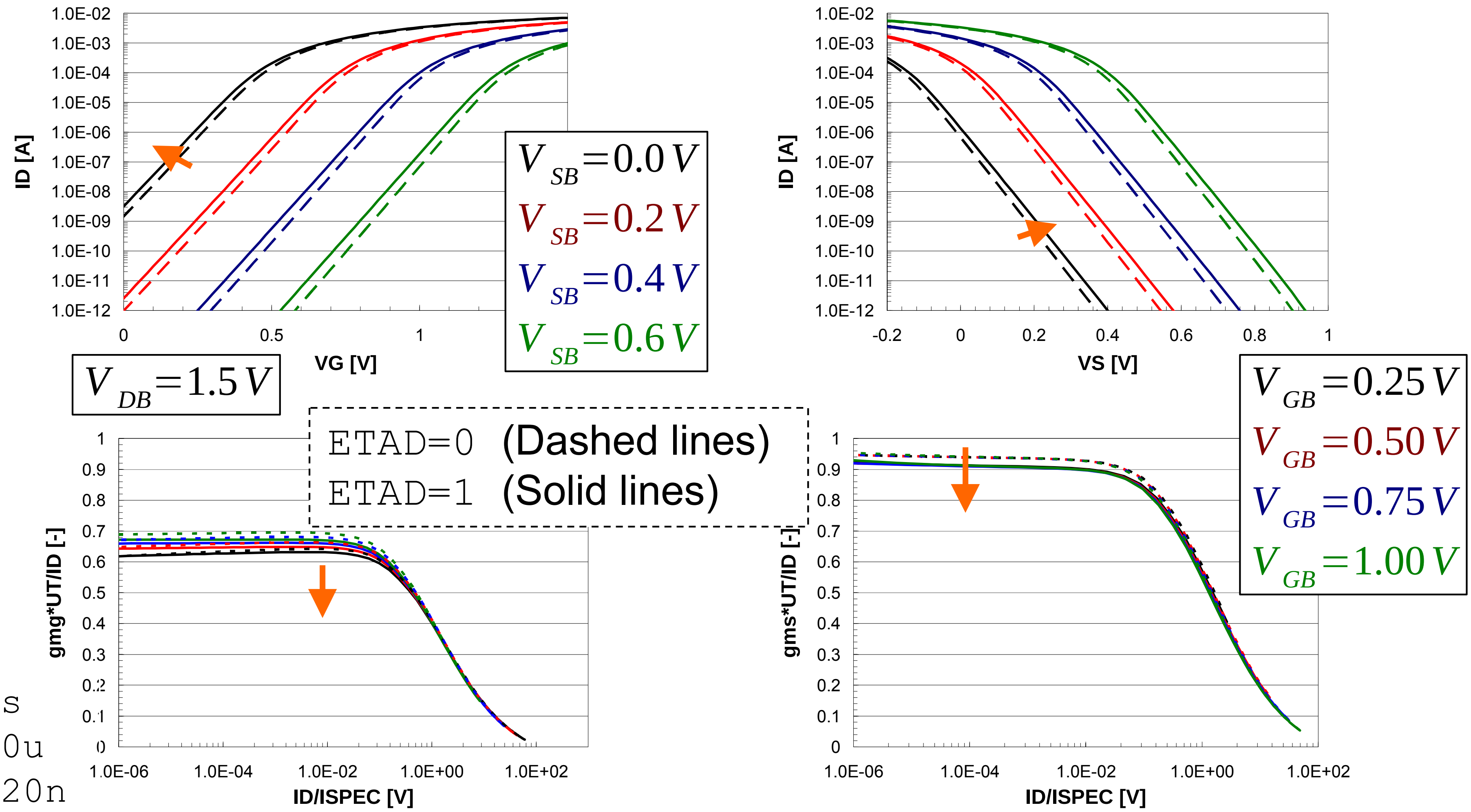
$$n = \left(\frac{dV_P}{dV_G} \right)^{-1}$$

$\mathtt{LETA} = 0.0$
$\mathtt{LETA} = 0.5$
$\mathtt{LETA} = 1.0$

```
nmos
W=10u
L=120n
```

DIBL effect

ETAD, [SIGMAD]

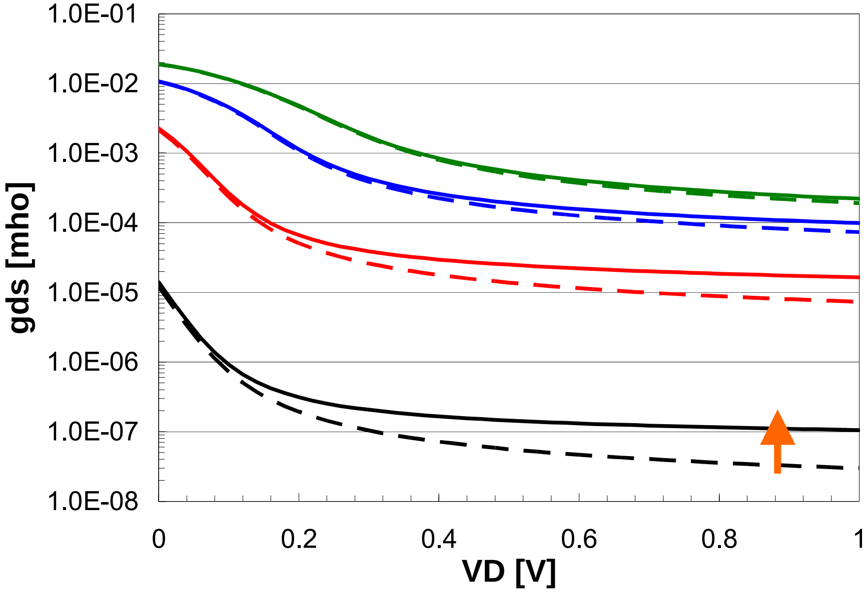


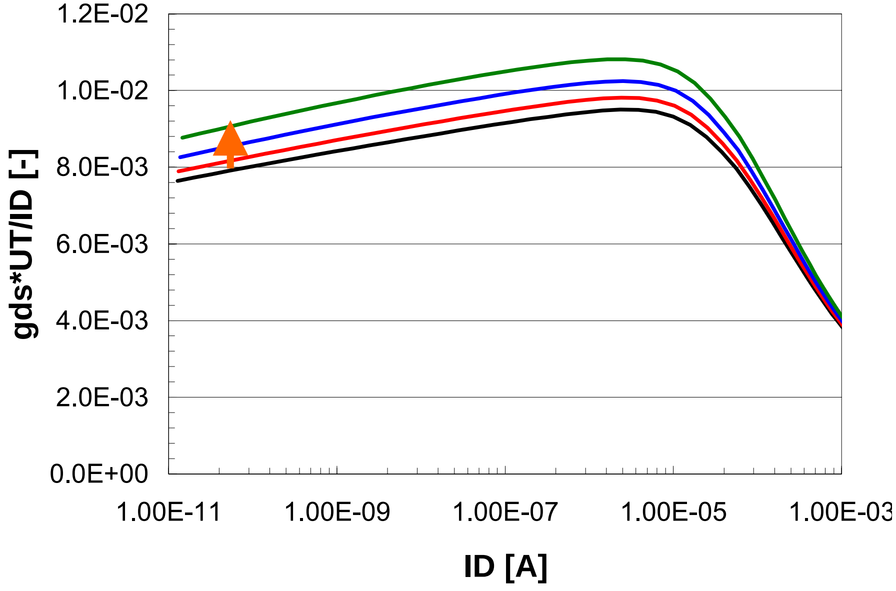
ETAD=0 (Dashed lines)
ETAD=1 (Solid lines)

nmos
W=10u
L=120n

DIBL effect on gds

ETAD, [SIGMAD]





$V_{GB}=1.00\,V$

$V_{GB}=0.75\,V$

$V_{GB}=0.50\,V$

$V_{GB}=0.25\,V$

ETAD=0 (Dashed lines)

ETAD=1 (Solid lines)

$\mathrm{ETAD}=0.75$

$\mathrm{ETAD}=0.70$

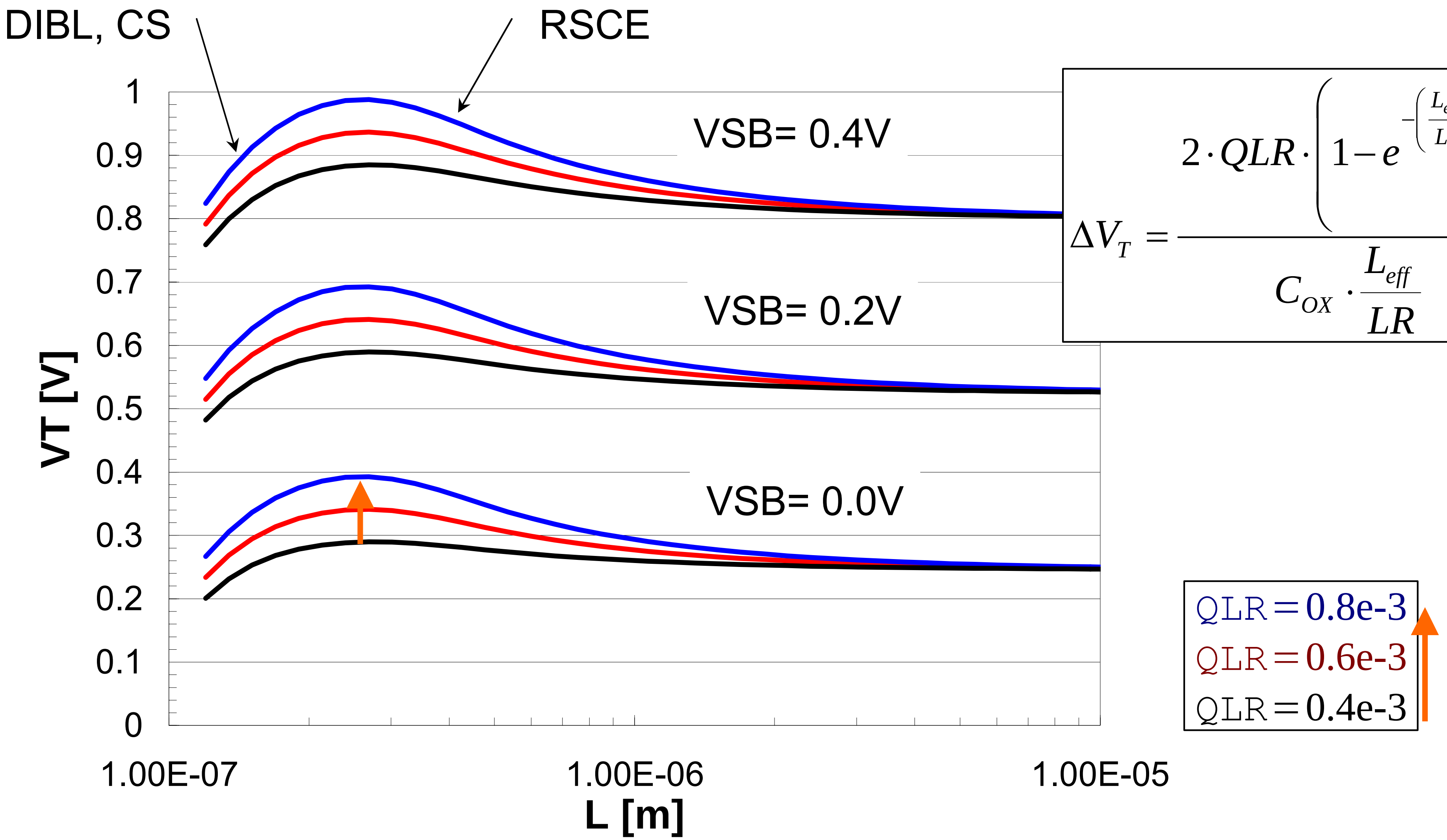
$\mathrm{ETAD}=0.65$

$\mathrm{ETAD}=0.60$

nmos
W=10u
L=120n

Reverse short channel effect

QLR

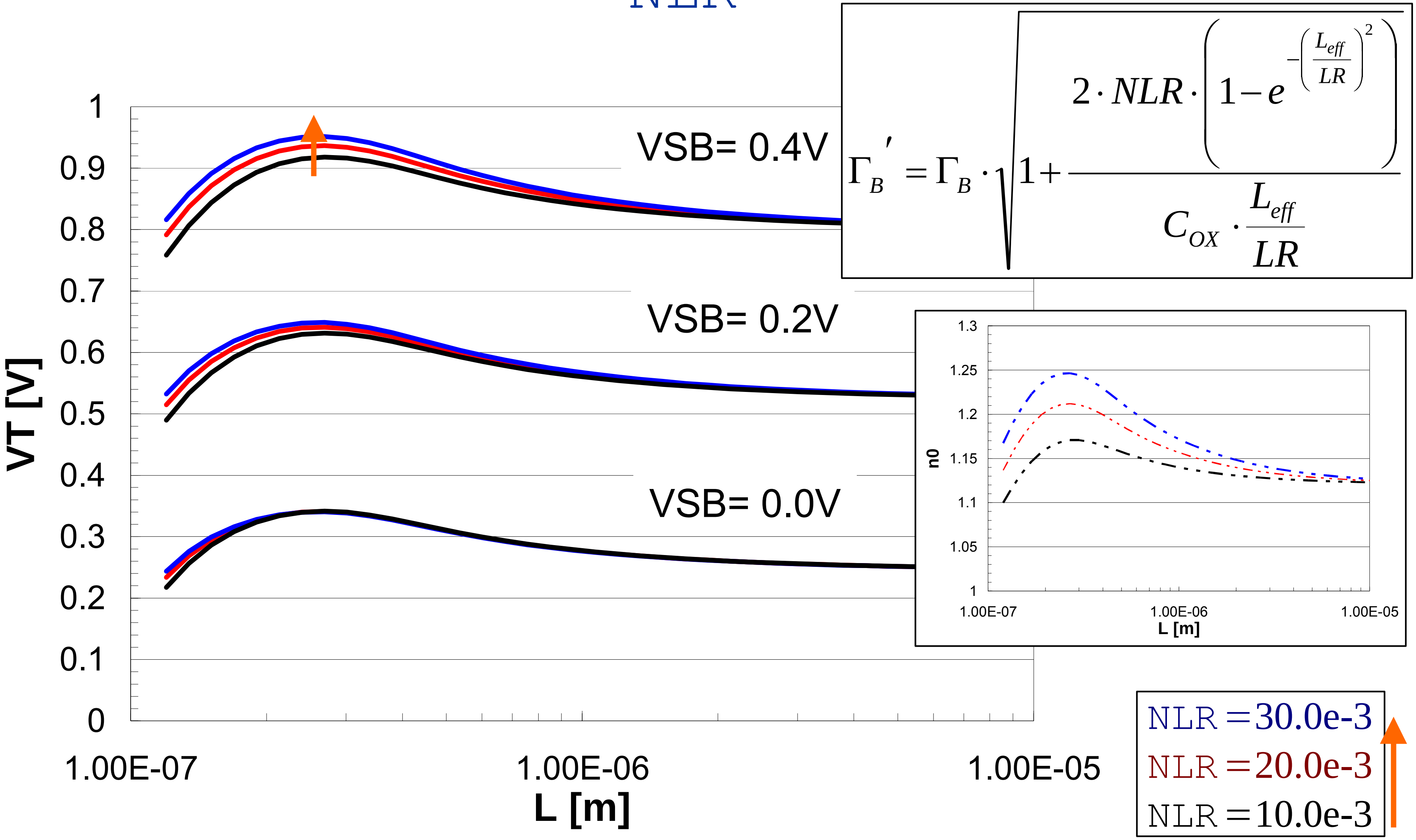


$$\Delta V_T = \frac{2\cdot QLR\cdot\left(1-e^{-\left(\frac{L_{eff}}{LR}\right)^2}\right)}{C_{OX}\cdot\frac{L_{eff}}{LR}}$$

Reverse short channel effect

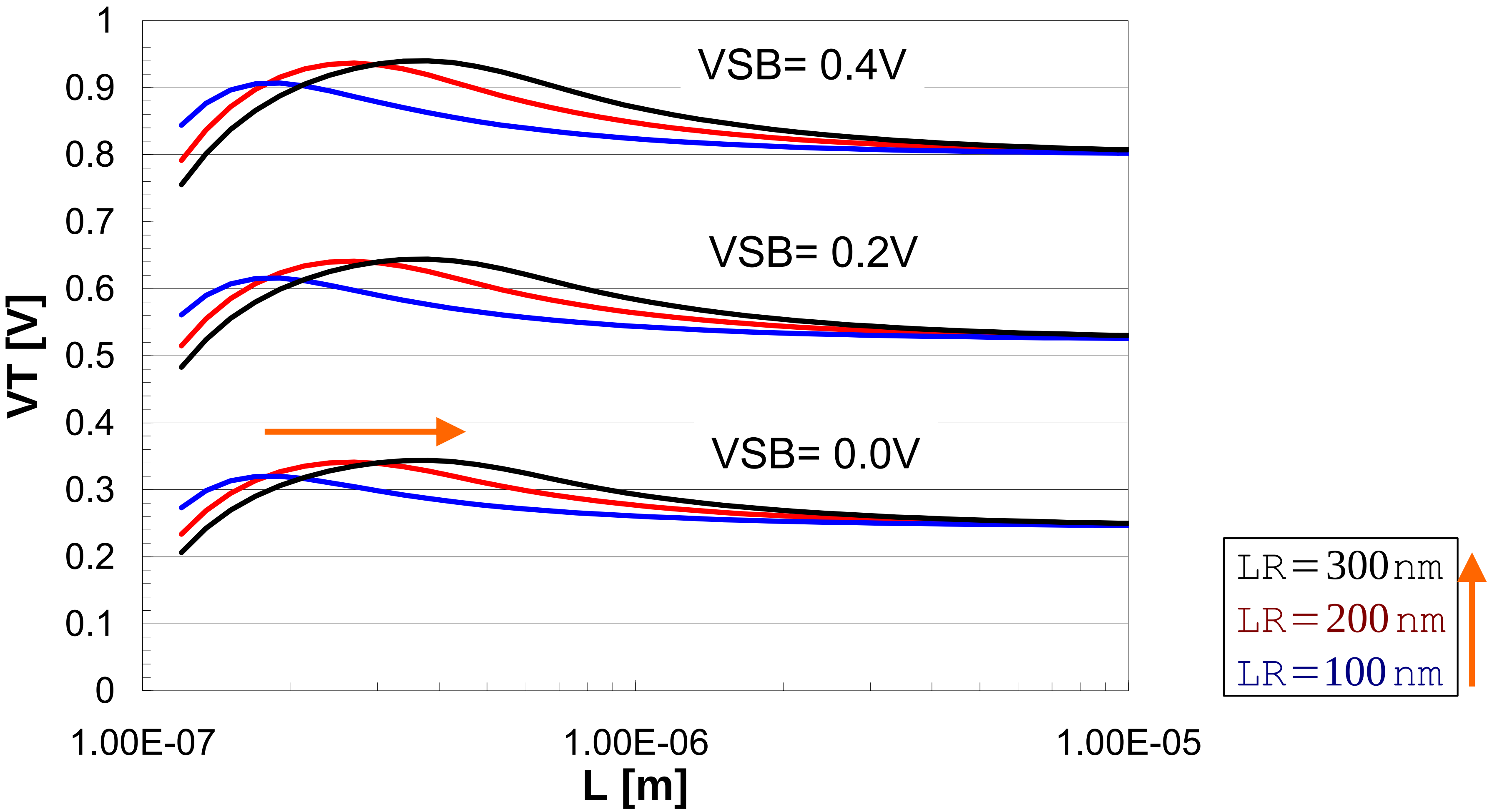
NLR

$$\Gamma_B{}' = \Gamma_B \cdot \sqrt{1 + \frac{2 \cdot NLR \cdot \left(1 - e^{-\left(\frac{L_{eff}}{LR}\right)^2}\right)}{C_{OX} \cdot \frac{L_{eff}}{LR}}}$$



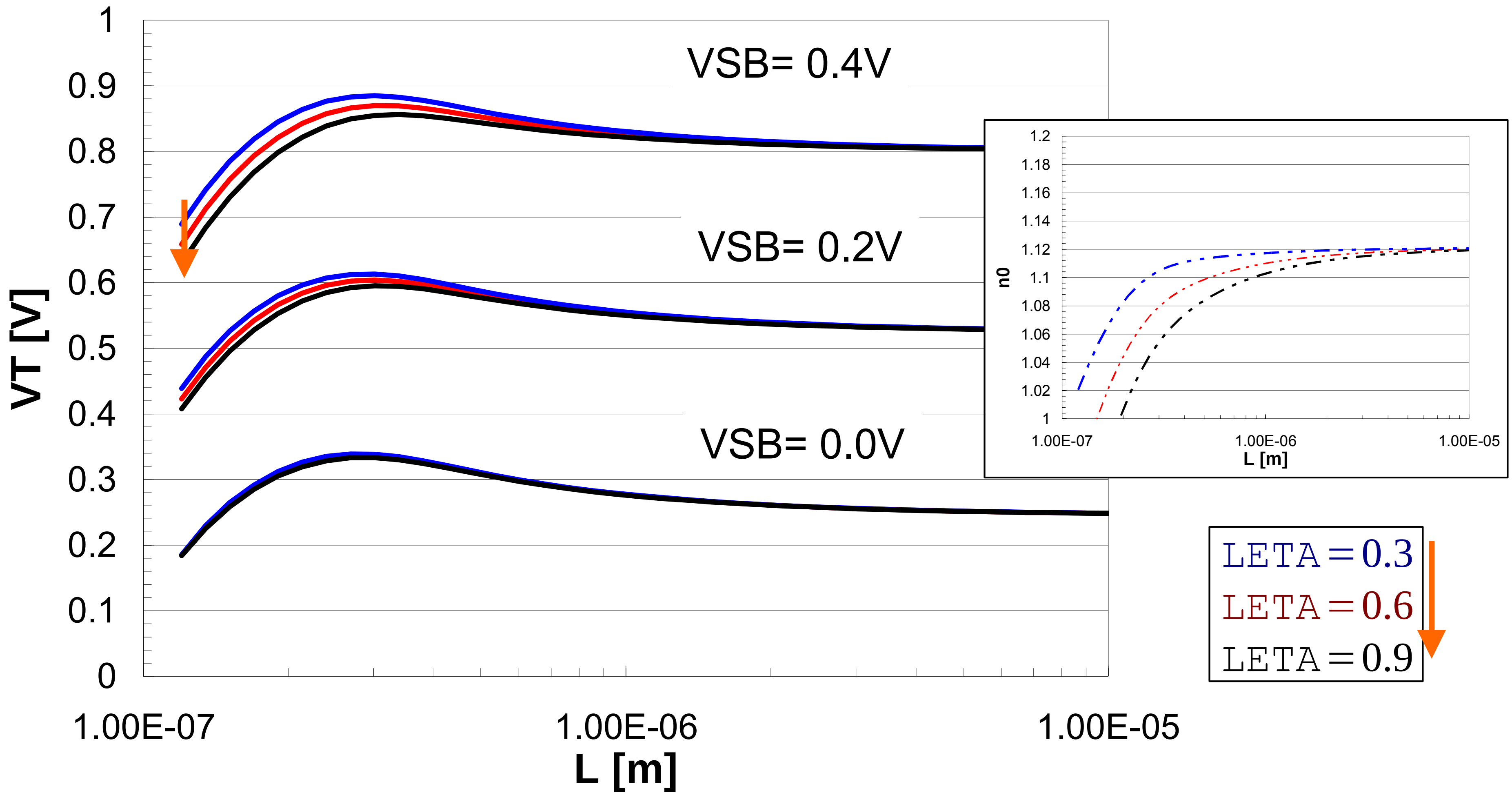
Reverse short channel effect

LR

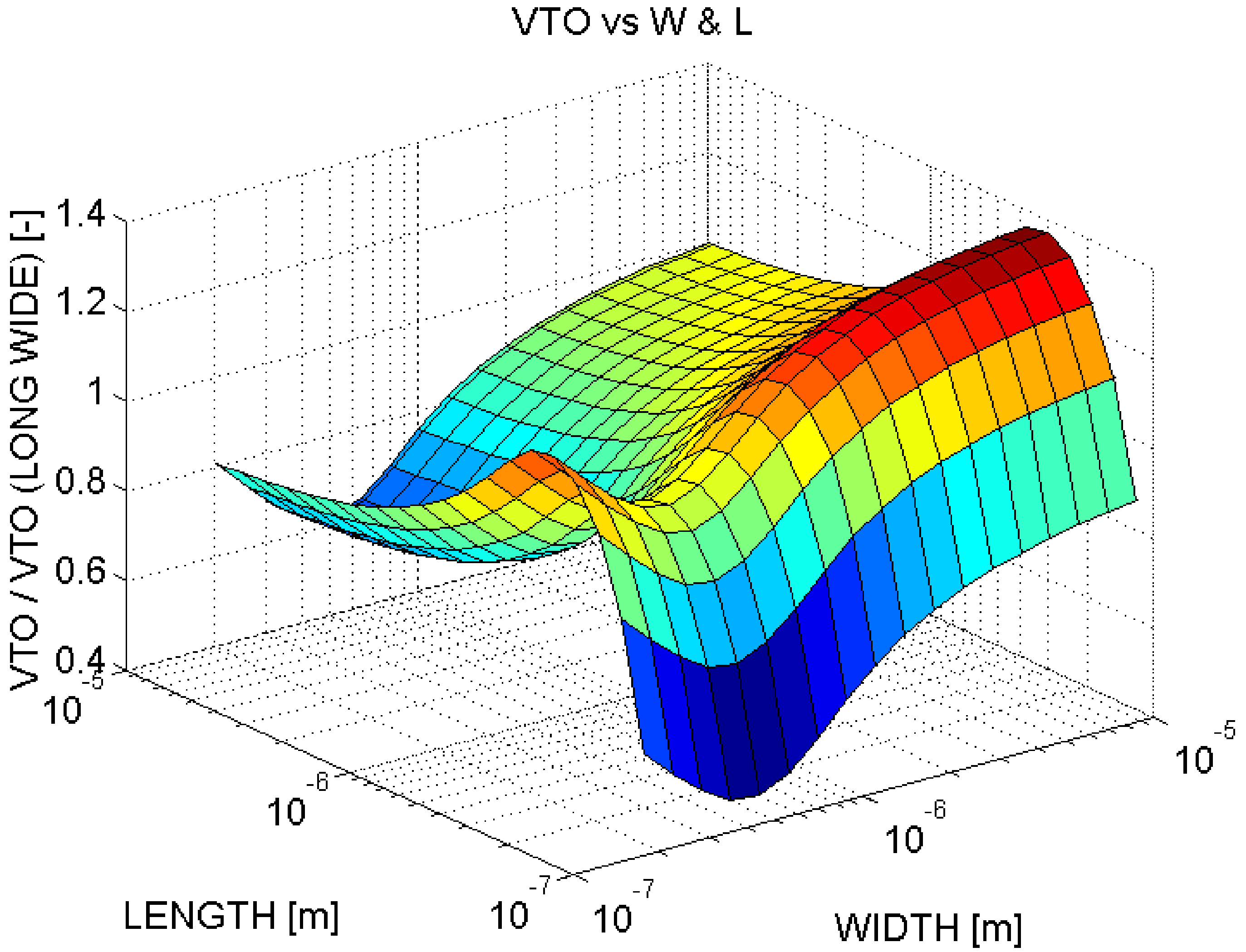


Charge sharing

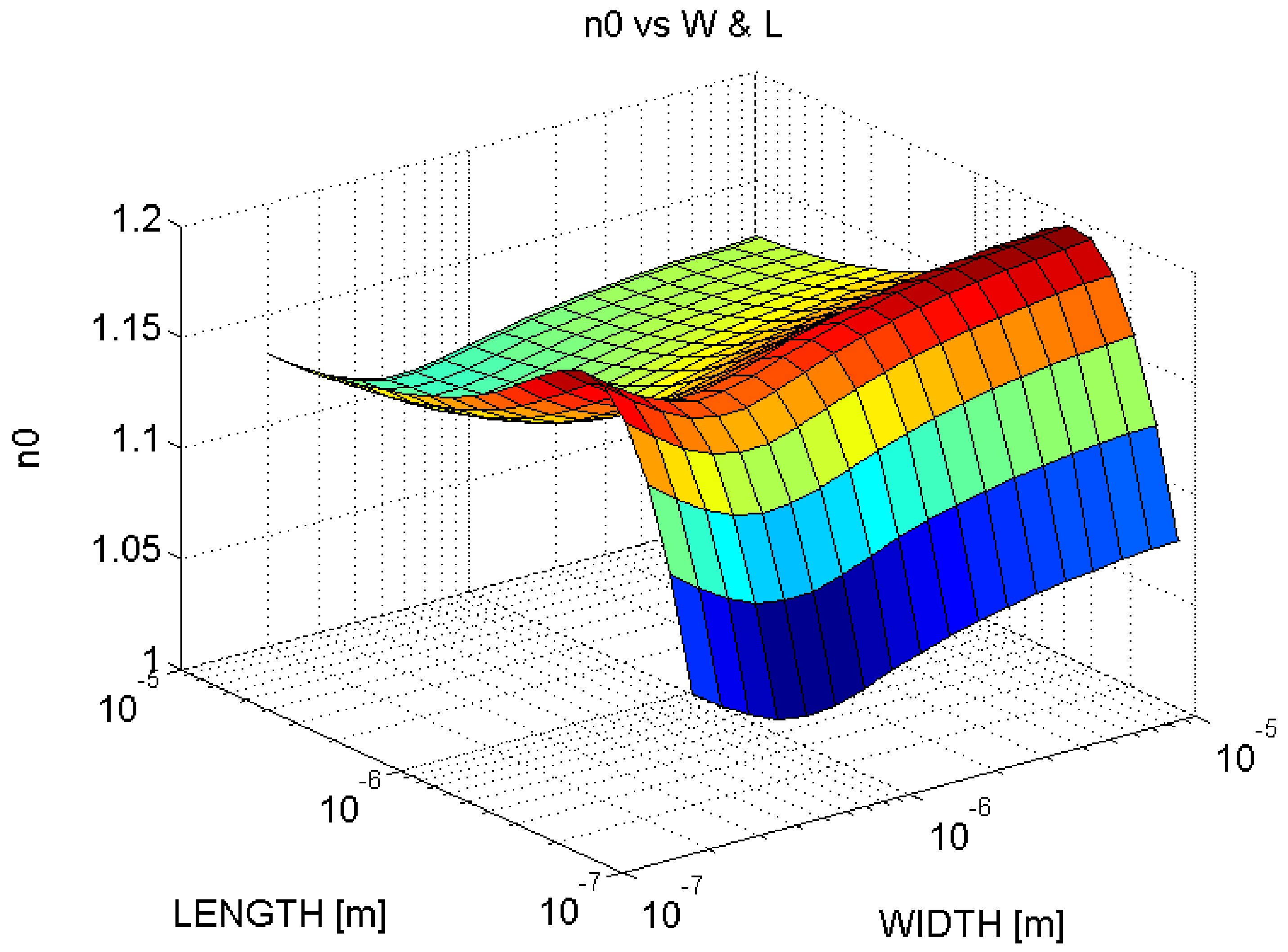
LETA



Threshold voltage vs. W & L



Slope factor vs. W & L



Summary

- EKV3.0 code is developed in Verilog-A
  - Verilog-A is the main platform of code development
  - Code tested in various simulators, among which ELDO & Spectre.
- A basic methodology of extracting EKV3.0 parameters has been presented
  - Methodology is similar over many CMOS generations
  - Effects of main EKV3.0 parameters on DC and CV characteristics have been illustrated.

Thank you very much
for your time and attention