MICRO ENCODER INC.

RELENTLESS INNOVATION

An EKV Model User's Perspective: For Low-Power Circuits and Beyond

EKV Users' Meeting/Workshop,
EPFL, Lausanne 4-5/11/2004

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Micro Encoder Inc

Agenda

- MEI introduction
- Why use the EKV model?
- Our experience using the model in a low-power circuit
- Where to get the models?
- Beyond low-power circuits: using EKV model for analog IC design in general
- Concluding comments

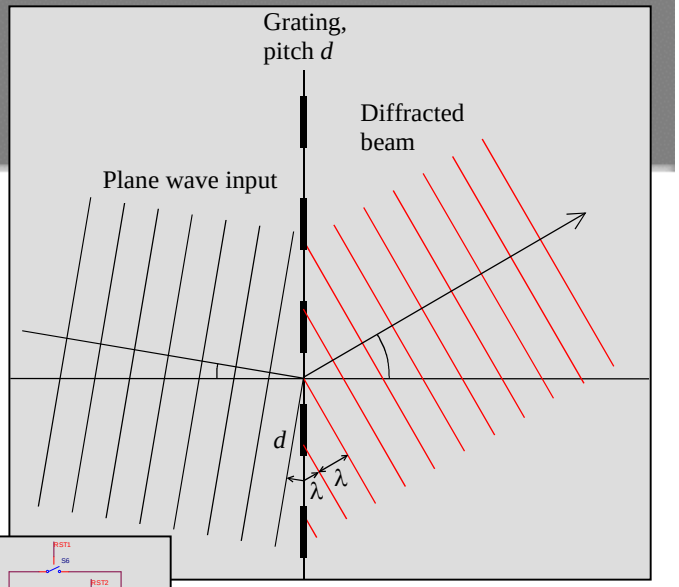
MICRO ENCODER INC.

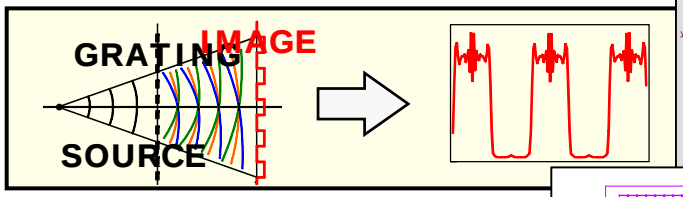
- Founded 1986
- Subsidiary of Mitutoyo Japan
- Independent Washington State Corporation
- Located in Kirkland, WA, USA
- 63 employees
- Research and development of technologies for dimensional metrology and other applications
  - Initial focus was capacitive encoder technology (Digimatic)
  - QuickVision vision measurement software & research started 1994
  - Now continuing QV work and other advanced sensor research

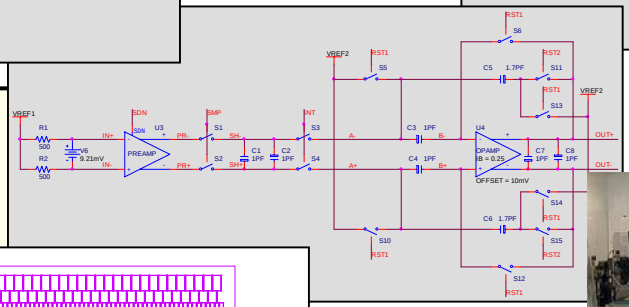
MEI's Work…

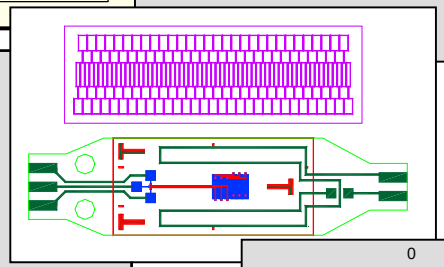
$$SIN_i' = \frac{2}{M}\sum_{m=0}^{M-1} S_i(\varphi_m - \delta)\sin(\varphi_m - i\alpha)$$
$$= \frac{2}{M}\sum_{m=0}^{M-1}\left[(1+dr_i)\cos(\varphi_m - i\alpha) + \delta\sin(\varphi_m - i\alpha) + \varepsilon_i\sin(\varphi_m - i\alpha) + \mu_i\right]\sin(\varphi_m - i\alpha)$$
$$= \frac{1}{M}\sum_{m=0}^{M-1}\left[(1+dr_i)\sin(2\varphi_m - i2\alpha) + \delta\left[1-\cos(2\varphi_m - i2\alpha)\right] + \varepsilon_i\left[1-\cos(2\varphi_m - i2\alpha)\right] + 2\mu_i\sin(\varphi_m - i\alpha)\right]$$
$$= \varepsilon_i + \frac{1}{M}\sum_{m=0}^{M-1}\delta - \frac{1}{M}\sum_{m=0}^{M-1}\delta\cos(2\varphi_m - i2\alpha)$$

$$c_n = \frac{1}{d}\int_{-l/2}^{l/2} T(x)\, e^{-i2\pi n\frac{x}{d}}\, dx = \frac{l}{d}\,\frac{\sin(\pi nl/d)}{\pi nl/d}$$



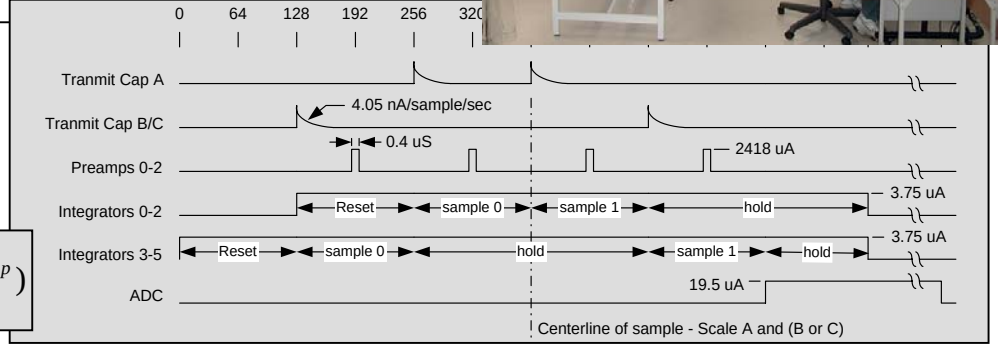






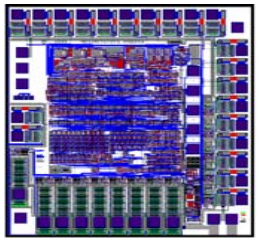
```
#ifndef QVAPI
   if ( m_pPickListManager )
   {
      QVRegistry& rRegistry = Singleton<QVRegistry>::Instance();

      int maxItems = m_pPickListManager->GetItemCount();;
      for ( int i = 1; i <= maxItems; i++ )
      {
         PICK_LIST_ITEM item;
         m_pPickListManager->GetNthItem( i, &item, FALSE ); // i IS ONE-BASED

         CString czSubKey = VPSECTION_PROGRAMCONTROL;
         czSubKey += _T("\\PickList");
         TCHAR Str[5] = _T("");
         _itot(i, Str, 10);
         czSubKey += Str;
                  rRegistry.WriteSTRING( czSubKey, _T("FileName"), item.m_szPath);
         rRegistry.WriteINT( czSubKey, _T("Start"), item.dwStart);
         rRegistry.WriteINT( czSubKey, _T("End"), item.dwEnd);
      }

      delete m_pPickListManager;
      m_pPickListManager = NULL;
   }
#endif
}
```

$$U(x,z) = \frac{e^{i2\pi z/\lambda - i\pi/4}}{\sqrt{2nn'}}\sum_{p=1}^{nn'} T(x + pd/n)\, e^{ip^2/(2nn')}\left(1 + i^{nn'}(-1)^p\right)$$



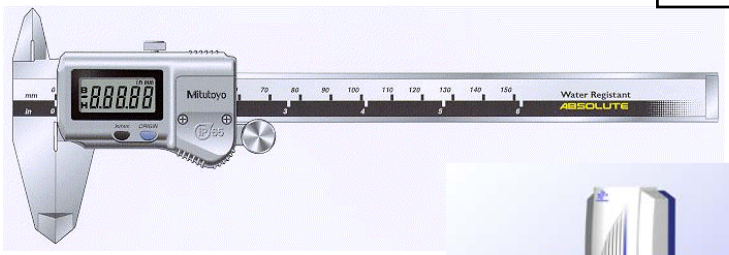
Mitutoyo Products with MEI Technology

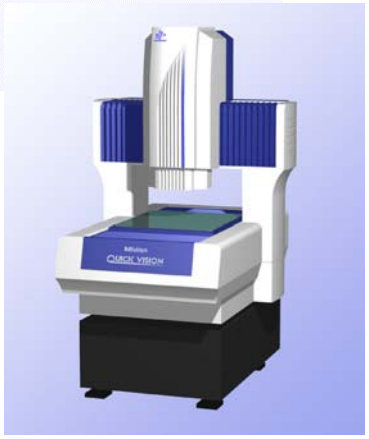
DIGIMATIC



Coming soon

Coolant Proof





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Why use the EKV model…

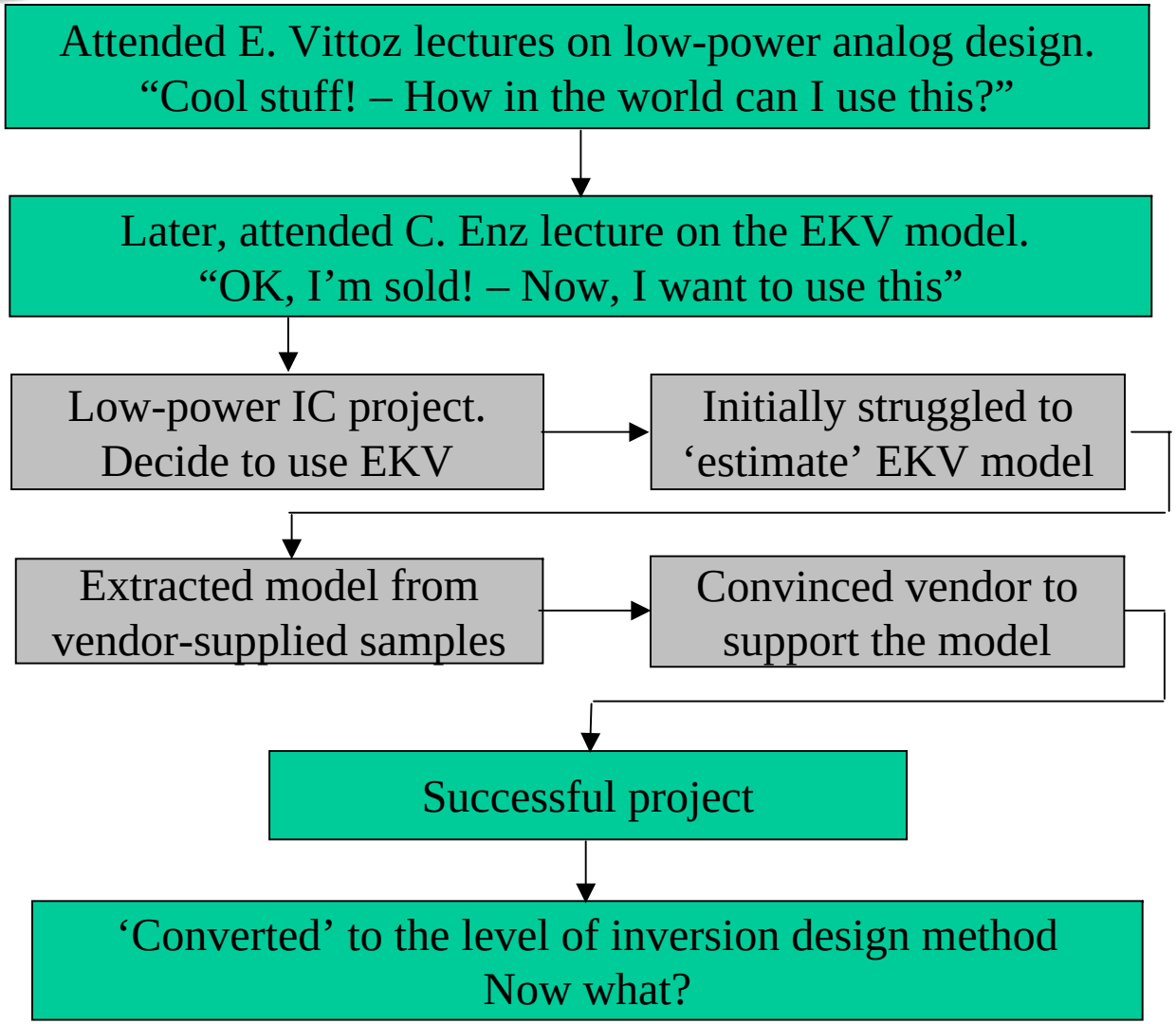
…when there is a perfectly good ‘industry standard’ model supported by all the foundries and EDA tool vendors?

Low power circuits:
- Better modeling of the weak and moderate inversion areas
- Initial intent of the model
- Most ‘accepted’ reason for using the model

Compact model:
- True ‘compact’ model (number of parameters)
- Hierarchical model: can be used both for simulations and hand calculation
- Faster simulations

Analog IC design:
- Better modeling of gm and noise, not just ID
- Analog circuits are usually biased with currents
- ‘Level of inversion’ design method

My experience with the EKV model



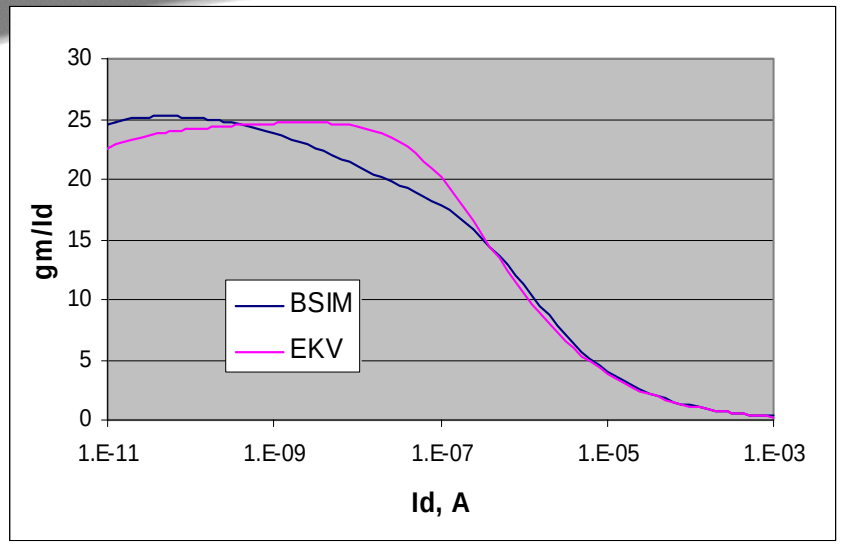
Getting started with the EKV model: a low-power (uAmps) analog circuit

- Many circuits used transistors in weak and moderate inversion – need for an accurate model through all modes of operations.
- At first, the foundry supplied us with transistor arrays to extract the model
  - We rented a HP4155B, and proceeded with doing our own extraction
  - We got reasonably good results, but not without challenges
- I presented the EKV model and its advantages for low-power design to the vendor.
- Eventually, the foundry's modeling expert 'bought' and studied the model, and the foundry supplied the models for this project (they have better hardware and software tools to do this).
- This was a successful story about promoting the model acceptance.

EKV 2.6 extraction challenges

- I am a circuit designer, not a modeling expert! (However, MOS modeling is definitely an interest of mine).
- The model is simple (few parameters), but getting the best possible fit for all sizes/conditions is not so easy.
- Limitation in hardware/software.
  - Hardware: very low current measurements required – HP4155B worked well.
  - Software: used Pspice + Matlab + Excel – no real extraction system.
- Some of the specific difficulties I encountered:
  - Short-channel NMOS: difficulty in matching the drain current both at low and high gate voltages. (due to absence of 2^{nd} order mobility reduction in EKV 2.6).
  - PMOS: difficulties in matching the drain current in both in linear and saturation regions.
- Solution: optimize the model for the project conditions.

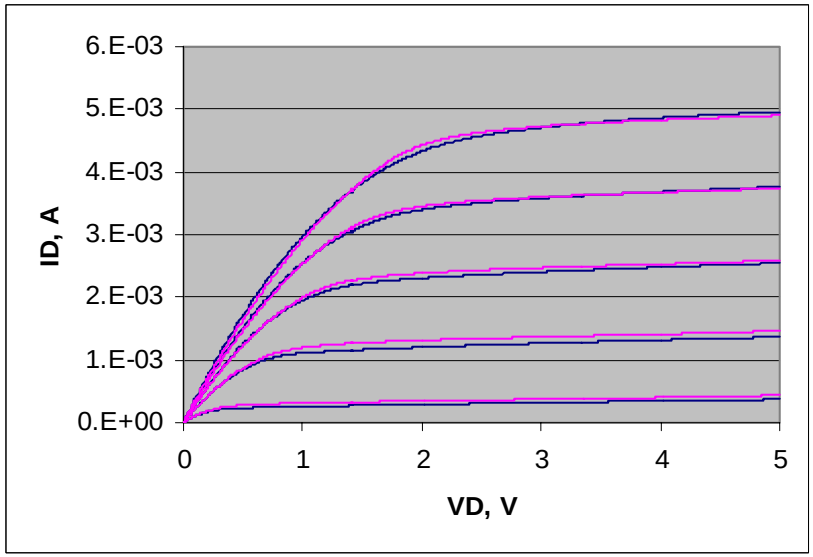
Where to get the models?:
1. - ‘Extract’ from the BSIM model (‘OK’)



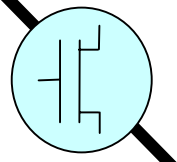
- Often, it is the only available option.
- However, we are extracting from a model that is not ‘perfect’.
- Upcoming tools?

<u>Possible compromise:</u>

- Get typical transistors curves from the foundry (if willing).
- Replay the model against the curves for fine tuning.
- Good solution for a better model with minimal involvement from the foundry.
- ‘Reality check’

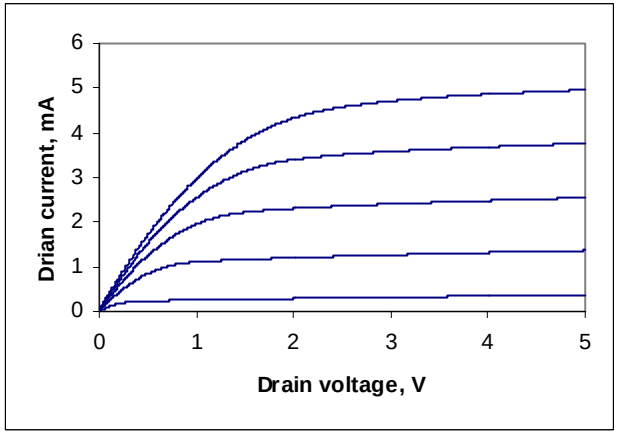


Where to get the models?:
2. - Extract from transistor samples (better)



Big questions/concerns:

- Typically, will work from a limited set of samples provided by the vendor.
- Are the samples representative of the ‘typical’ process?
- Requires some hardware (low current measurements).
- ‘Good’ extraction is not so easy.



Use a qualified extraction service

- Better solution, but…
- May be expensive.
- The concerns about the transistor samples remain valid.

Where to get the models?:
3. – Have the foundry supply the model (best)

- Best solution - the foundry has access to:
  - Knowledge of the process.
  - A lot of process data.
  - Extraction hardware/software.
- But… a lot of resistance
  - Difficult to convince the foundry to have to support another model.
  - Not ‘industry standard’.
  - Traditionally, the market has been dominated by digital IC’s.
  - However… mixed-signal SOC’s are becoming more relevant! – SOC is the new ‘buzz word’.
- Analog/mixed-signal foundries.
  - Should consider supporting the model for analog designers.
  - Low-power processes are prime candidates.

Beyond low-power circuits: Analog circuit design

- The EKV model is also very good for analog circuits in general
  - Several features useful for the analog IC designer: matching parameters, estimation of drain/source parasitics…
  - The model can be easily used for hand calculations and optimization (see next slide).
  - The gm/ID equation is based on currents – most analog circuits are biased with currents – So, why base our calculations on a voltage (Vdsat)?
  - The model was designed by analog IC designers for analog IC designers.
  - The model is valid for all modes of operation (weak – moderate – strong inversion).
- The main roadblocks are model acceptance and availability. The ‘industry standard’ BSIM model dominates the industry.
- Need to educate designers, foundries and EDA vendors.

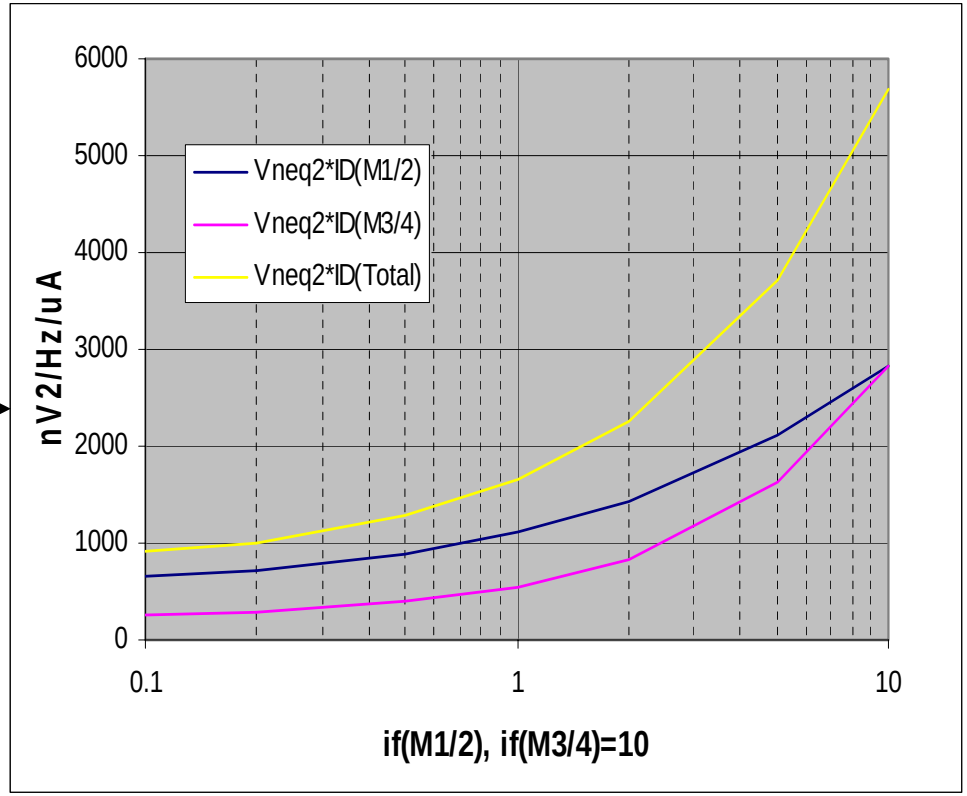
Example of circuit optimization using the EKV - equations: low noise (not low power) op-amp:

$$i_f = \frac{I_D}{I_S}$$

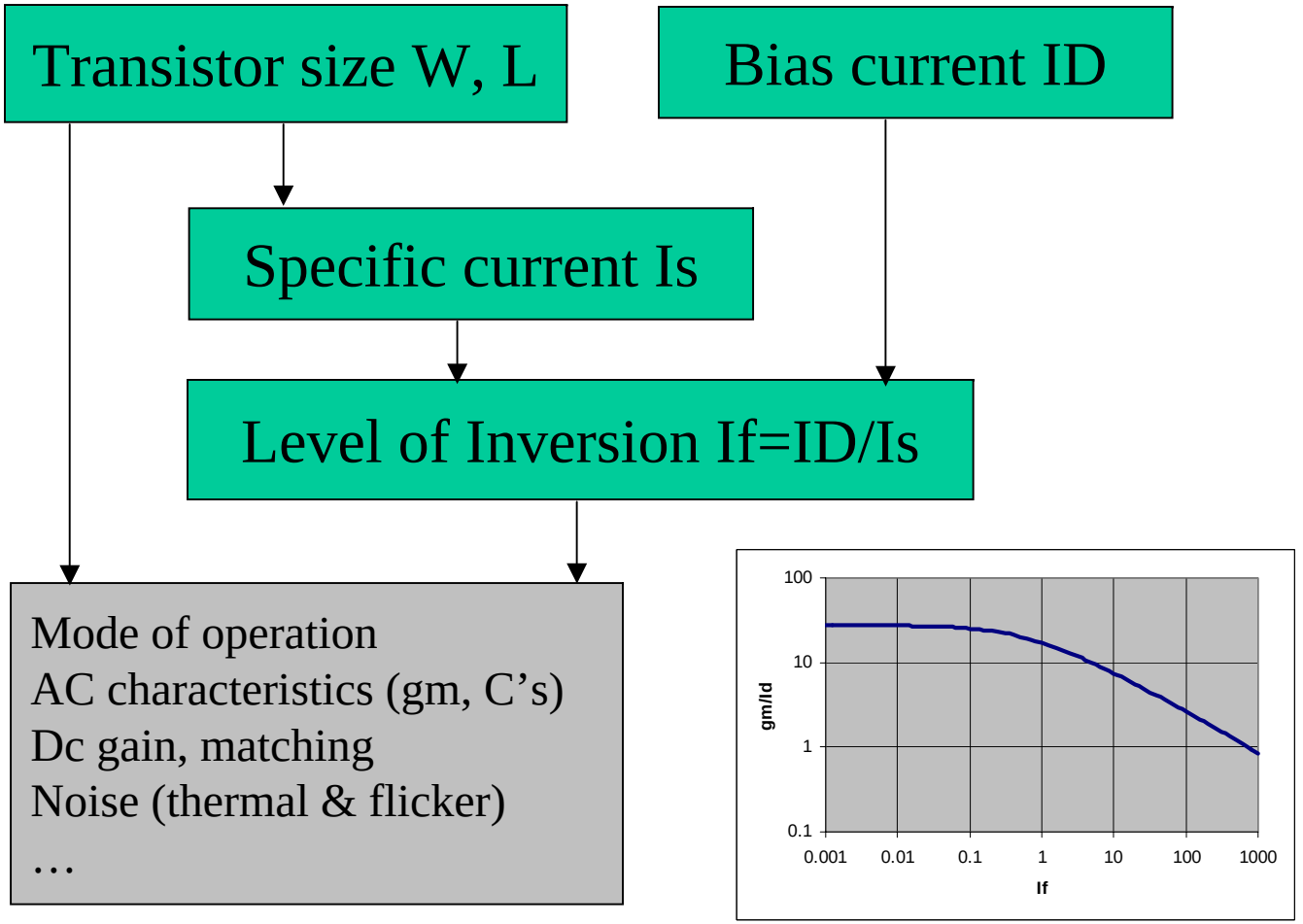
$$\frac{g_m}{I_D} = \frac{1}{n \cdot UT} \cdot \frac{2}{1 + \sqrt{4 \cdot i_f + 1}}$$

$$\gamma = n \cdot \frac{1}{1 + i_f} \cdot \left(\frac{1}{2} + \frac{2}{3} \cdot i_f \right)$$

$$V_n^2 = \gamma \cdot \frac{4KT}{g_m}$$



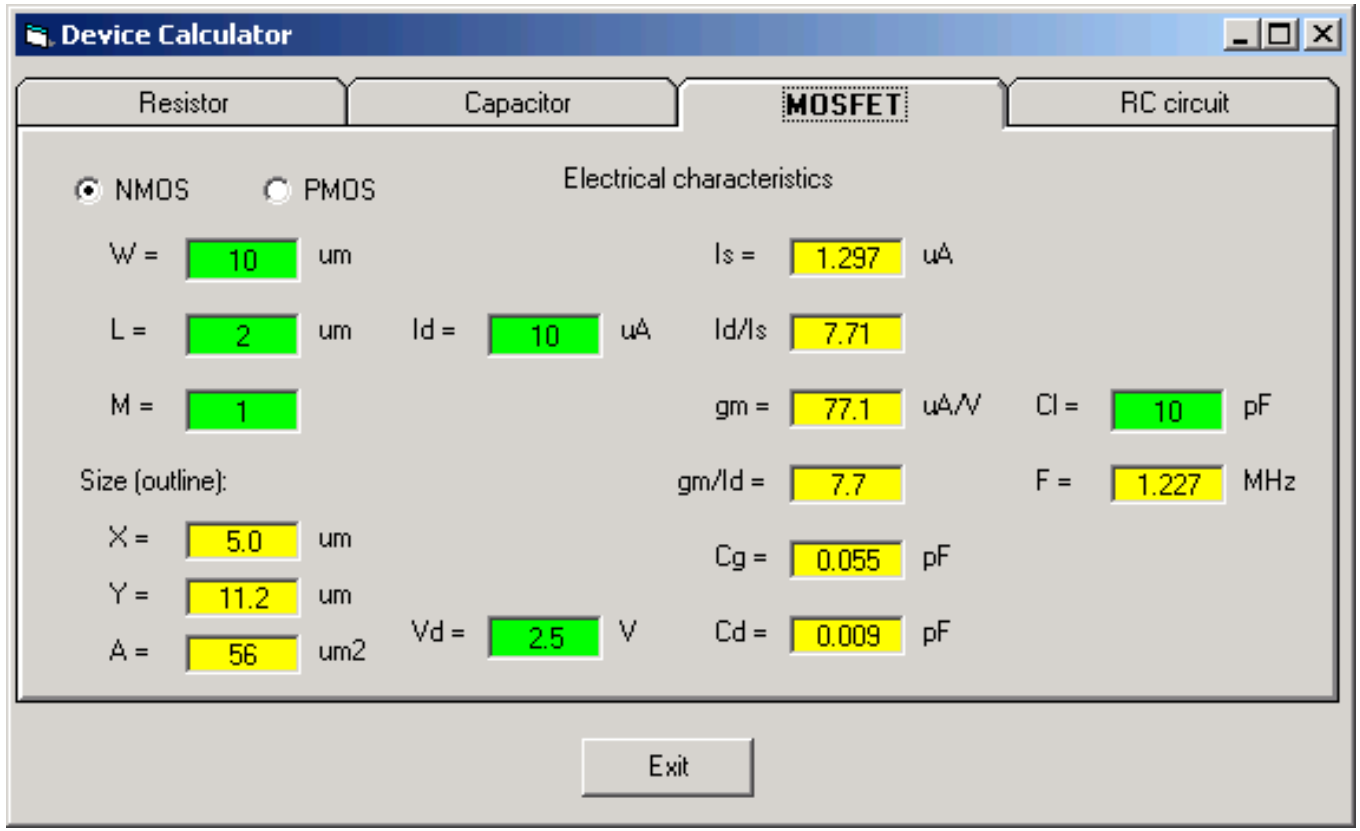
EKV model -> Level of inversion design method for transistor sizing



The Level of Inversion Methodology

- Uses continuous linear equations to calculate gm and thermal noise from transistor size and bias current, valid for all modes of operation of the transistor.
- I used this method to optimize a low-noise amplifier, in a normal (not battery powered) application. This was very successful. However, the BSIM model was used for simulations. (In the moderate to strong inversion, the BSIM is OK, at least for gm)
- More logical method of sizing transistors from the bias current.
- I now use this for all design. It just requires estimating the specific current for different transistor sizes (L).
- The level of inversion design method has now been presented in papers and seminars (D. Binkley, D. Foty) since then.

Example of ‘computer-aided hand calculations’: My handy transistor calculator!



Concluding comments

- The EKV model (2.6) is now supported by most EDA tools/simulators.
- It is a superior model for low-power analog IC design.
- The main issue for the user is ‘where to get the models’ – 3 different solutions.
- It is also a better model for analog IC design in general (‘level of inversion’ method).
- Any questions?

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