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EKV3.0 MOS Transistor Model for Advanced Analog IC Design

Matthias Bucher, TUC
François Krummenacher, EPFL
Antonios Bazigos, NTUA

bucher@electronics.tuc.gr
Electronics & Computer Engineering Department
Technical University of Crete (TUC)
GR-73100 Chania, Crete, Greece

EKV team & contributors to EKV3.0

- Team of universities contributing to EKV model R&D: EPFL, TUC/NTUA, U. Strasbourg
  - François Krummenacher, Christian Enz, Eric Vittoz
  - Jean-Michel Sallese, Wladek Grabinski, Ananda Roy
  - Matthias Bucher, Antonios Bazigos
  - Alain-Serge Porret
  - Christophe Lallement, Fabien Pregaldiny
- Code development: TUC/NTUA
  - Coordination with EPFL

The EKV2.6 model

- Developed at EPFL, 1997 [PhD M. Bucher]
  - Same physical basis as EKV3.0
    -- first widely used “charge linearization” model
  - < 20 parameters, many “analog” features
  - Available in many circuit simulators
    - ADS, AMI-Spice, Antrim-A/MS, APLAC, ELDO, IntuSoft, HSIM, LTspice/SwitcherCAD, Star-Hspice, MacSpice, Micro-CapV, MINIMOS-NT, MI-SUGAR, NanoSpice, Nexxim, NG-Spice, PSpice, SABER, SANCAD, SIMetrix, SmartSpice, SMASH, Spectre, SpectreRF, SPICE3, Spice-Opus, Synopsys, TopSPICE, TRANZ-TRAN, T-Spice, WinSpice …
  - http://legwww.epfl.ch/ekv/model.html#availability
- Mainly used by analog IC design teams
  - Fabless companies
    - Nokia, Xemics, Tektronix, Microen, CSEM, Advanced Silicon, …
  - Foundries/vertically integrated
    - Toshiba, Atmel, Microchip, Microelectronic Marin, NEC, …
  - Many universities & research institutes
    - EPFL, ETHZ, UNCC, CERN, LETI …

EKV3.0 outline – basis & motivation

- Motivation:
  - Efficient, truly compact model including for sub-100nm CMOS
  - Physical basis, predictivity & dependable behaviour
  - Low number of parameters, scalable, non-binned
  - Addressing design needs in advanced analog IC design
  - Co-development of design methodologies and characterization methods

- EKV3.0 MOST model for next generation CMOS
  - Evolution from EKV2.6, address known shortcomings
  - High level of code standardization
  - Next generation model standard evaluation (CMC procedure)

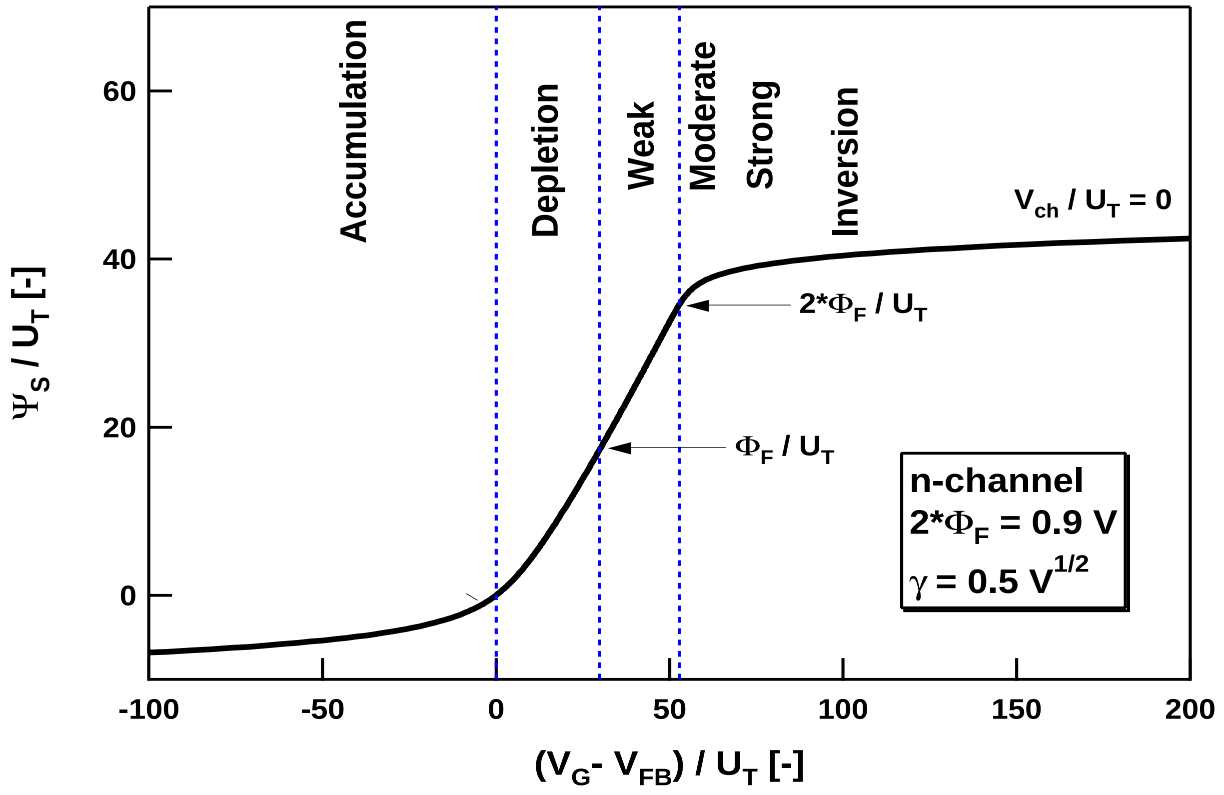
Outline

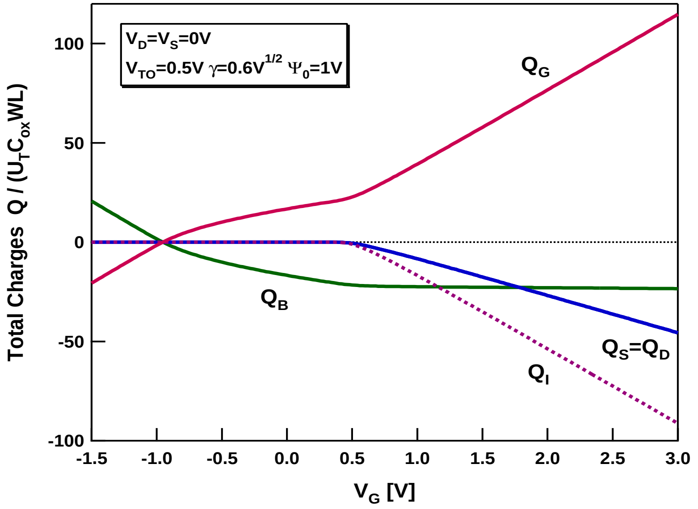
- EKV3.0 model structure
  - Charge model basics
  - Local/integral charge model
  - Polydepletion & quantum effects [François Krummenacher]
  - Short-channel capacitance model
  - Charge-based mobility model
  - Short-channel effects
  - Benchmarking
- Level-of inversion-centered view of the MOST
- Summary

EKV3.0 – basics of charge based model

- Model is based on surface potential model combined with inversion charge linearization
  - Linearization method brings much extended analytical capabilities
  - Uses same parameters as the surface potential model
- Substrate referred, symmetric forward/reverse operation
  - Model quantities are continuous, well behaved
- Coherent analytical model for all quantities:
  current, charge, noise,…
- Integral charge model is obtained by integration
- Consistent static, quasi-static, NQS, noise & matching
- Charge-based mobility/velocity saturation modeling

Surface potential in MOS structure

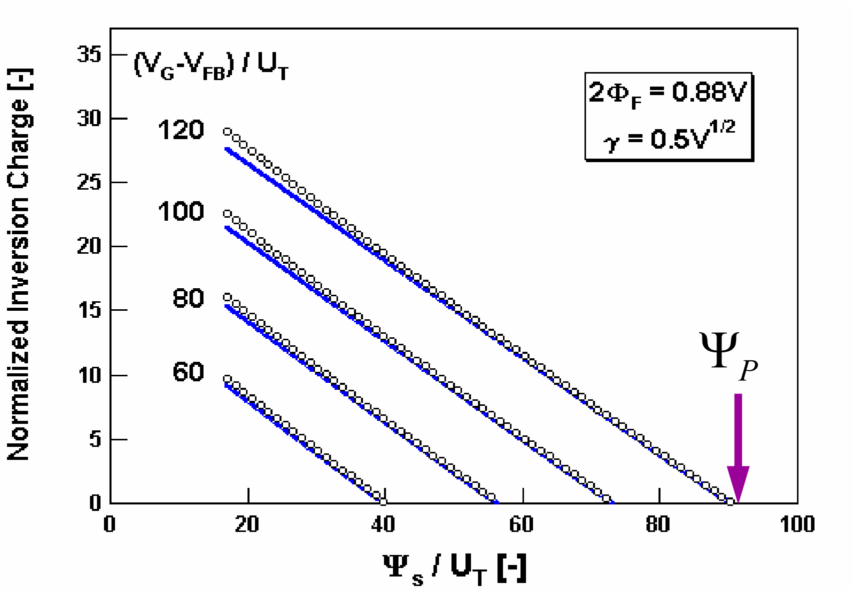


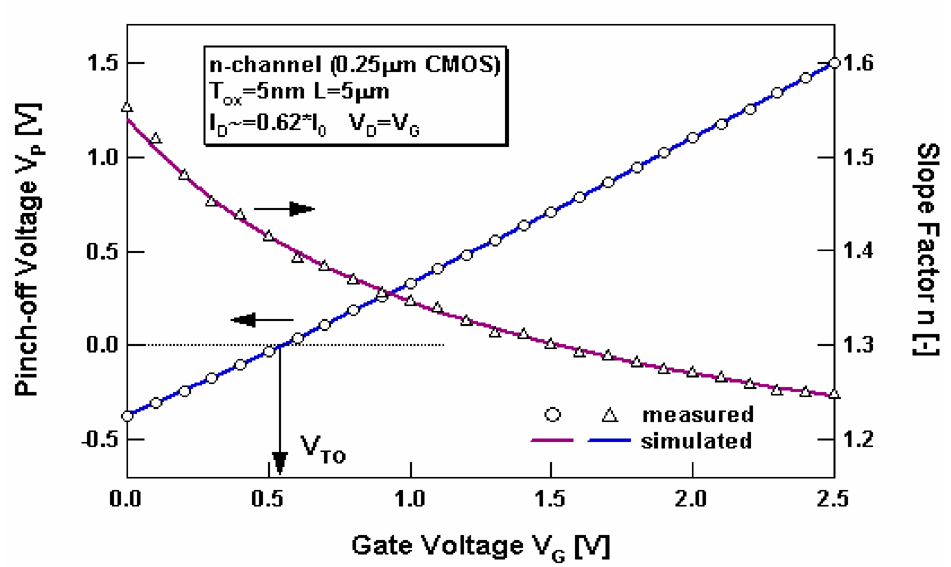


- Charge & voltage balance:

$$V_G - V_{FB} = \Psi_S - \frac{Q_b' + Q_i'}{C_{ox}}$$

Inversion charge linearization (I)





- Inversion charge vs. surface potential (fixed V_G) is essentially linear
- Explicit use of linearization defines *charge linearization factor* n_q
- Intersection with x-axis defines *pinch-off surface potential* Ψ_p

$$\Psi_P = V_G - V_{FB} + \gamma_s \cdot \left[\frac{\gamma_s}{2} - \sqrt{\left(\frac{\gamma_s}{2}\right)^2 + V_G - V_{FB}} \right] \quad where \quad \gamma_s = \frac{\sqrt{2q\varepsilon_{si}N_{sub}}}{C'_{ox}}$$

- Related concepts of *pinch-off voltage* $V_p = \Psi_p - \Psi_0$ and *slope factor* n_v
  - Use the same parameters (`TOX`, `NSUB`, `VFB`) as surface potential model

Inversion charge linearization (II)

- Relation between inversion charge and surface potential
  - Linear relationship among Q_i and Ψ_S: n_q is the inversion charge linearization factor

$$Q_i' = C_{ox}'(V_G - V_{FB} - \Psi_S - \gamma\sqrt{\Psi_S})$$

$$-\frac{Q_i'}{C_{ox}'} = n_q(\Psi_S - \Psi_P)$$

- Relationship among channel conductance and Q_i

$$\left.\frac{dI}{dV_{ch}}\right|_x = \mu\frac{W}{L}(-Q_i'(x))$$

- Current & charge normalization

$$I_{Spec} = 2n_q\mu C_{ox}'\frac{W}{L}U_T^2 \qquad Q_{Spec}' = 2n_q C_{ox}' U_T^2$$

- Voltage-charge relationship
  - Bucher e.a. ISDRS 1997, Bucher PhD Thesis 1999

$$\boxed{v_P - v_{ch} = 2q_i + \ln(q_i) \quad where \quad v = \frac{V}{U_T}, q_i = \frac{Q_i'}{Q_{Spec}'}}$$

- Drain current including drift & diffusion terms
  - Symmetric forward-reverse operation, valid in all modes of inversion

$$I_D = \mu W(-Q_i')\frac{dV_{ch}}{dx} = \mu W(-Q_i'\frac{d\Psi_S}{dx} + U_T\frac{dQ_i'}{dx})$$

$$\boxed{I_D = I_{Spec}(i_f - i_r) \quad where \quad i_{f(r)} = q_{iS(D)}^2 + q_{iS(D)}}$$

EKV3.0 outline – higher-order effects

- Non-uniform doping effects:
  - Vertical/lateral non-uniform doping effects
  - RSCE, pocket/halo doping related effects
- High-field effects, advanced technology:
  - Polydepletion & quantum effects
  - Gate tunnelling current, GISDL, substrate current
- Charge-based mobility modelling:
  - Vertical field mobility based on effective field
  - Velocity saturation/channel length modulation
- Short-channel effects:
  - DIBL, charge-sharing
  - INWE, combined short&narrow-channel effects
- Bias-dependent parasitics modelling:
  - Overlap charge/capacitance model
  - Bias-dependent series resistance model
- Temperature effects

EKV3.0 outline – additional features

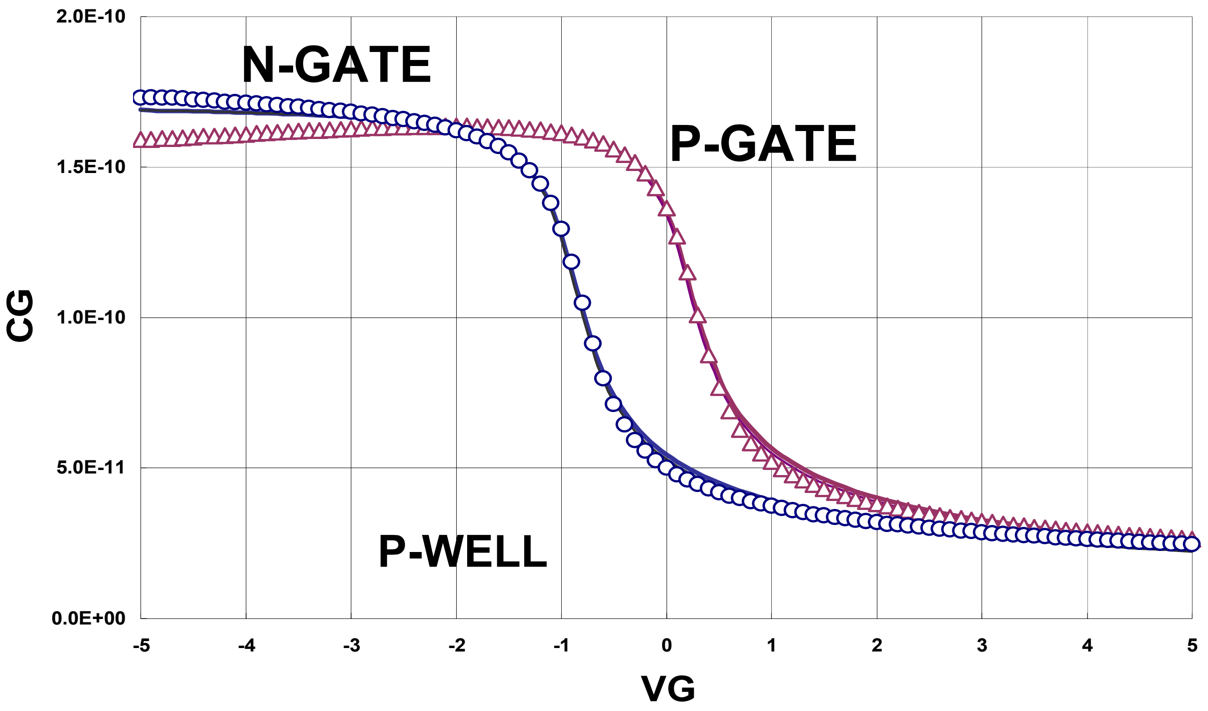
- 2^{nd}-order scaling of parameters:
  - Includes length-dependence of mobility
  - STI-stress related effects
- Non-quasistatic AC model
  - Companion model for transient under development
- Noise:
  - 1/f noise
  - Short-channel thermal noise
  - Induced noise in gate and substrate
- More analog-design oriented features:
  - Local mismatch models built-in
  - Feedback to designer w.r.t. level-of-inversion, tef, GBW, ...
- Choice of use: physical OR electrical parameters

EKV3.0 charge model – higher-order effects

- Polydepletion & quantum effects (PDE & QME)
- Modeling of short-channel effects in charge/capacitances
  - Basic channel/gate doping (RSCE), ….
  - …. & 2D effects (DIBL, CS) propagate into the charges model
  - Effective channel length for charges/capacitances:

    LeffC = L + `XL` + `DL` + `DLC`
  - Accounting for CLM & VSAT also in transcapacitances
- Bias-dependent overlap charge model
- Inner fringing charge/capacitance

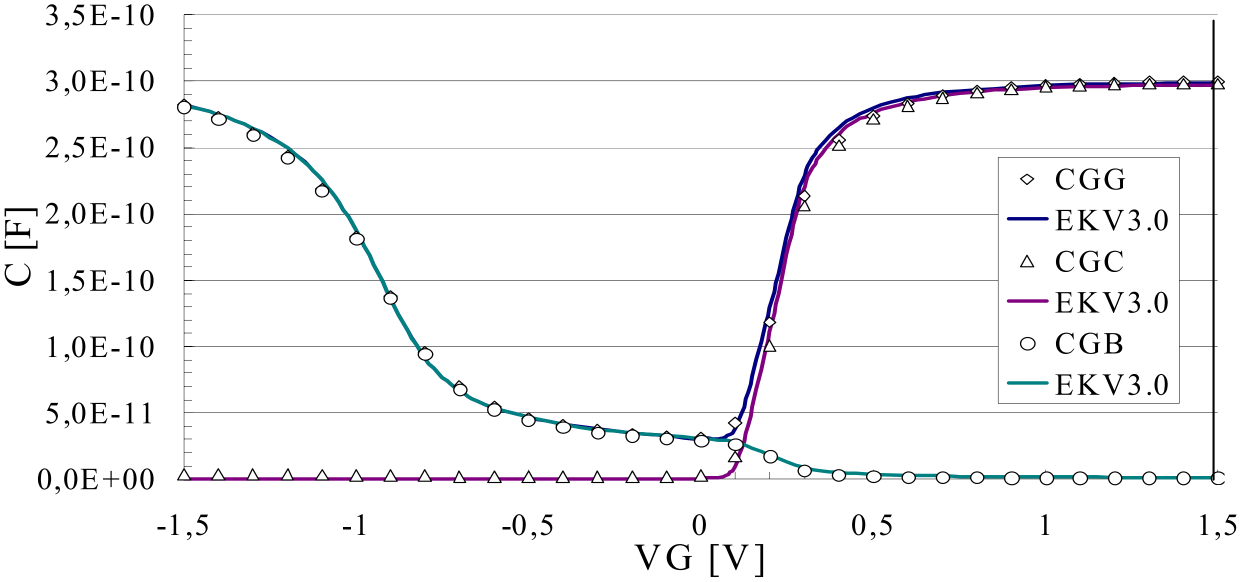
MOS capacitor/varactor modeling



- Model can be used to model MOS varactors
- PDE may occur in accumulation for opposite type of gate
  - Choice of the type of gate with a model parameter `TG`
  - Only change is for `NGATE`, `VFB`

Long-channel CV – 0.12um CMOS

L = 10um

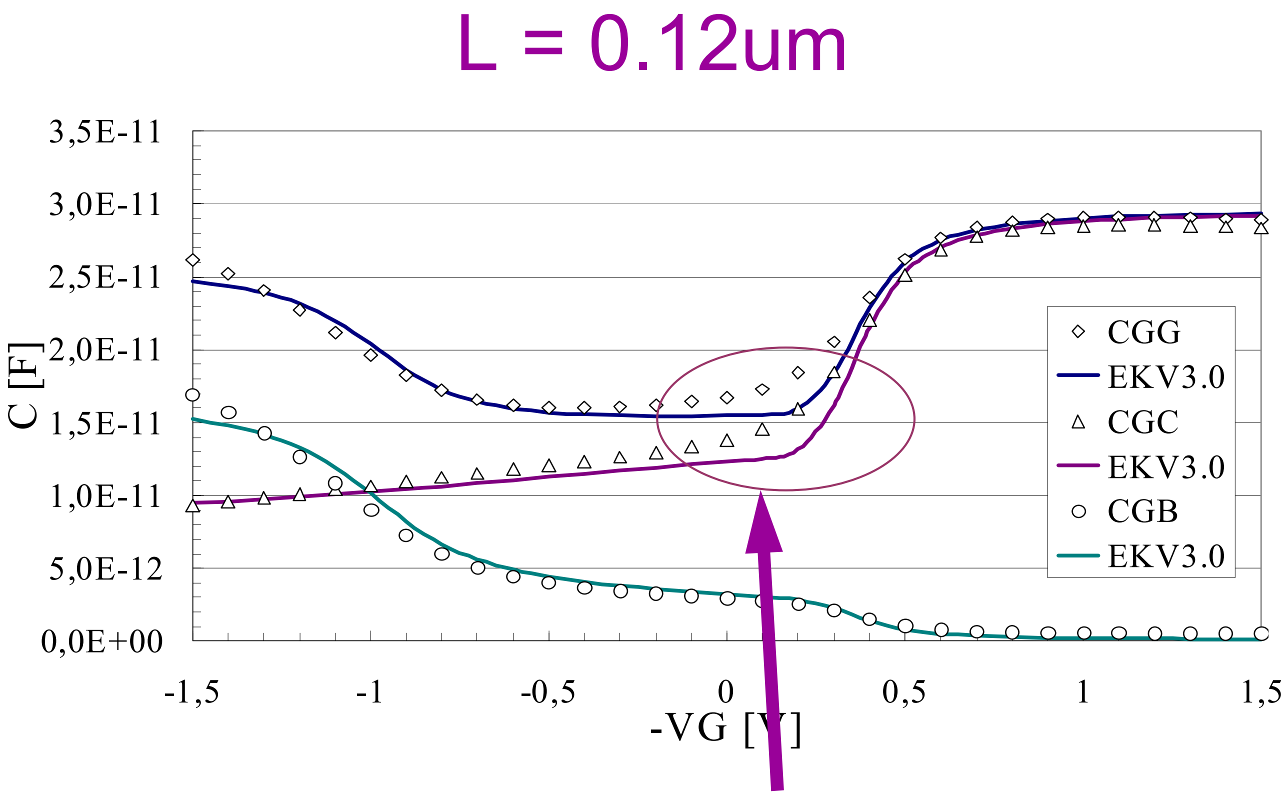


+PHIF	=	400m	V
+COX	=	12m	F/m2
+VTO	=	250m	V
+GAMMA	=	200m	$V^{-1/2}$
+GAMMAG	=	7	$V^{-1/2}$

Overlap charge/capacitance

- Model of (direct) Gate-to-S/D overlap
  - Local charge model w. depletion/accumulation
  - Similar as for varactor modeling
  - Higher-order effects: QME, PDE
  - Overlap parameters:
    - `VFBOV` – Flat-band voltage of Gate-S/D overlap
    - `NOV` [`GAMMAOV`] – Overlap region doping conc.
    - `LOV` – Gate-S/D overlap region length

Short-channel CV – 0.12um CMOS



+GAMMAOV = 2.5 $V^{-1/2}$

+LOV = 20n m

+VFBOV = 0 V

- Short-channel CV (L=0.12um) with example parameters
- Need to add *inner fringing term*

Inner fringing capacitance

- Charge-based model, empirically based but essentially related to surface potential at source/drain

$$\Delta Q_{IF,X} = A_{IF} \cdot (1 + B_{IF} V_X) \cdot \sqrt{V_{bi} + V_X - \Psi_{SX}}$$

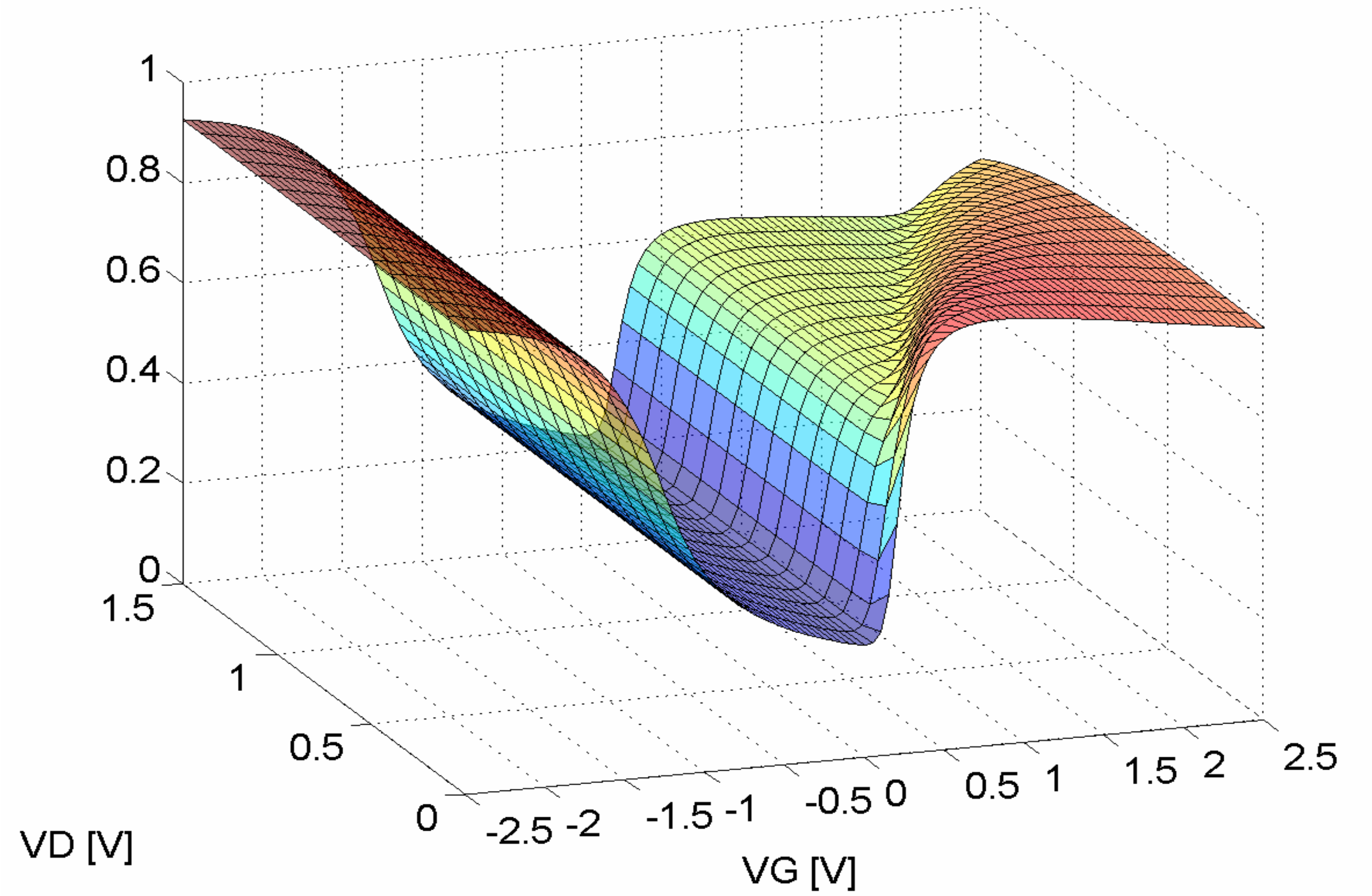
$$where \quad X = S, D$$

$$\Delta Q_G = -\Delta Q_{IF,S} - \Delta Q_{IF,D}$$

G. Gildenblat e.a., IEDM Tech. Digest 2003

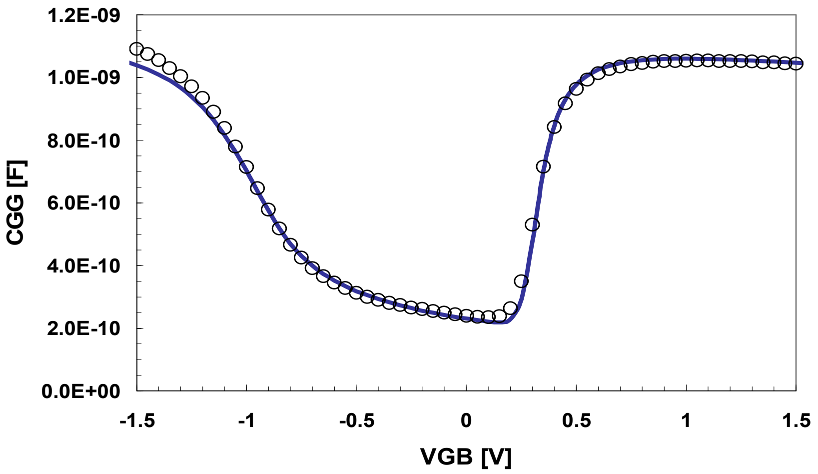
- 2 empirical fitting parameters, `AIF, BIF`

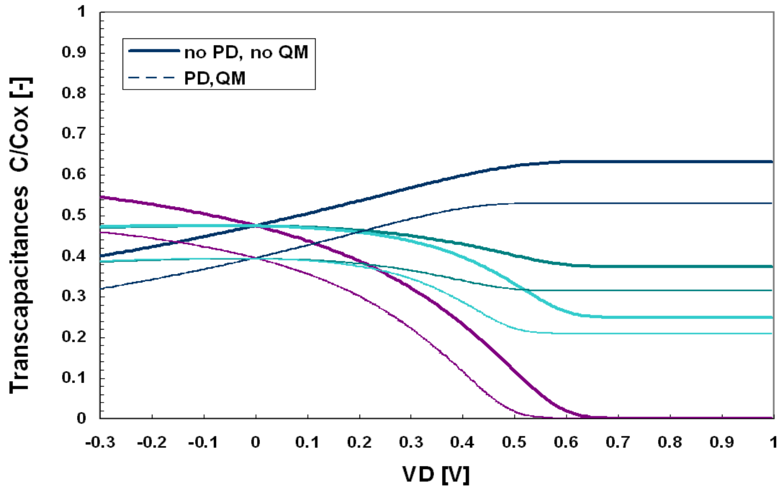
Capacitance benchmarks (I)

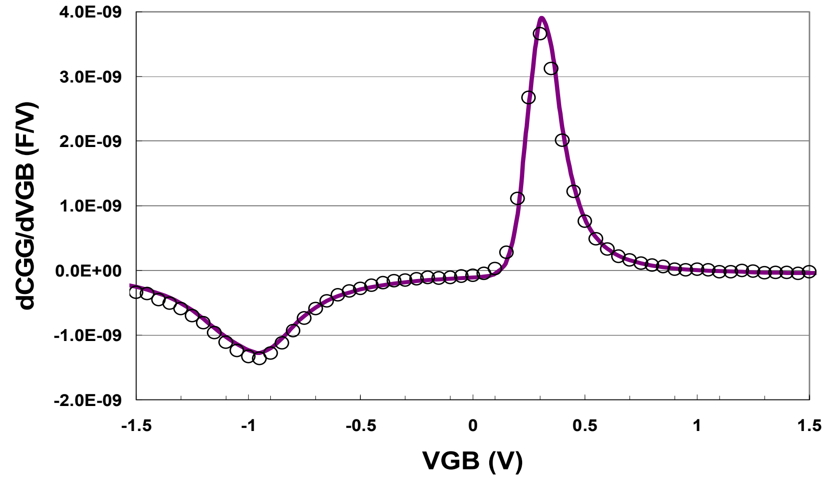


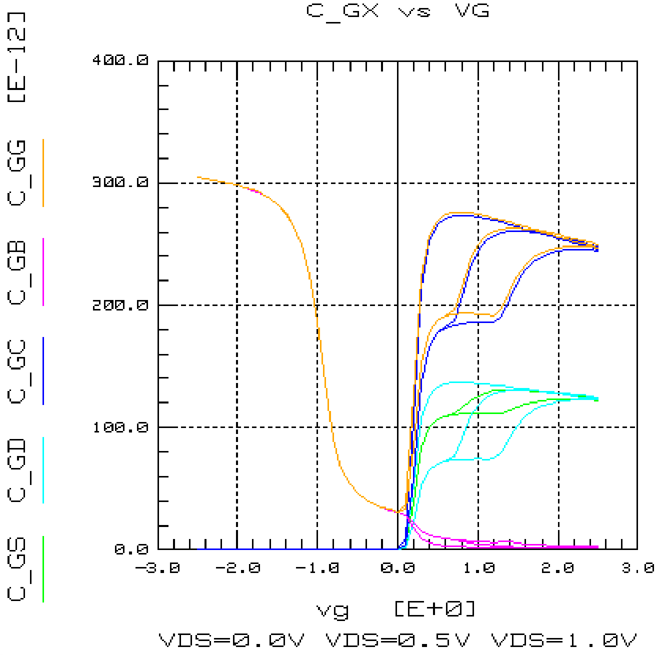
- Smooth, well-behaved CV model
  - From accumulation to depletion and inversion
  - From linear to saturation

Capacitance benchmarks (II)

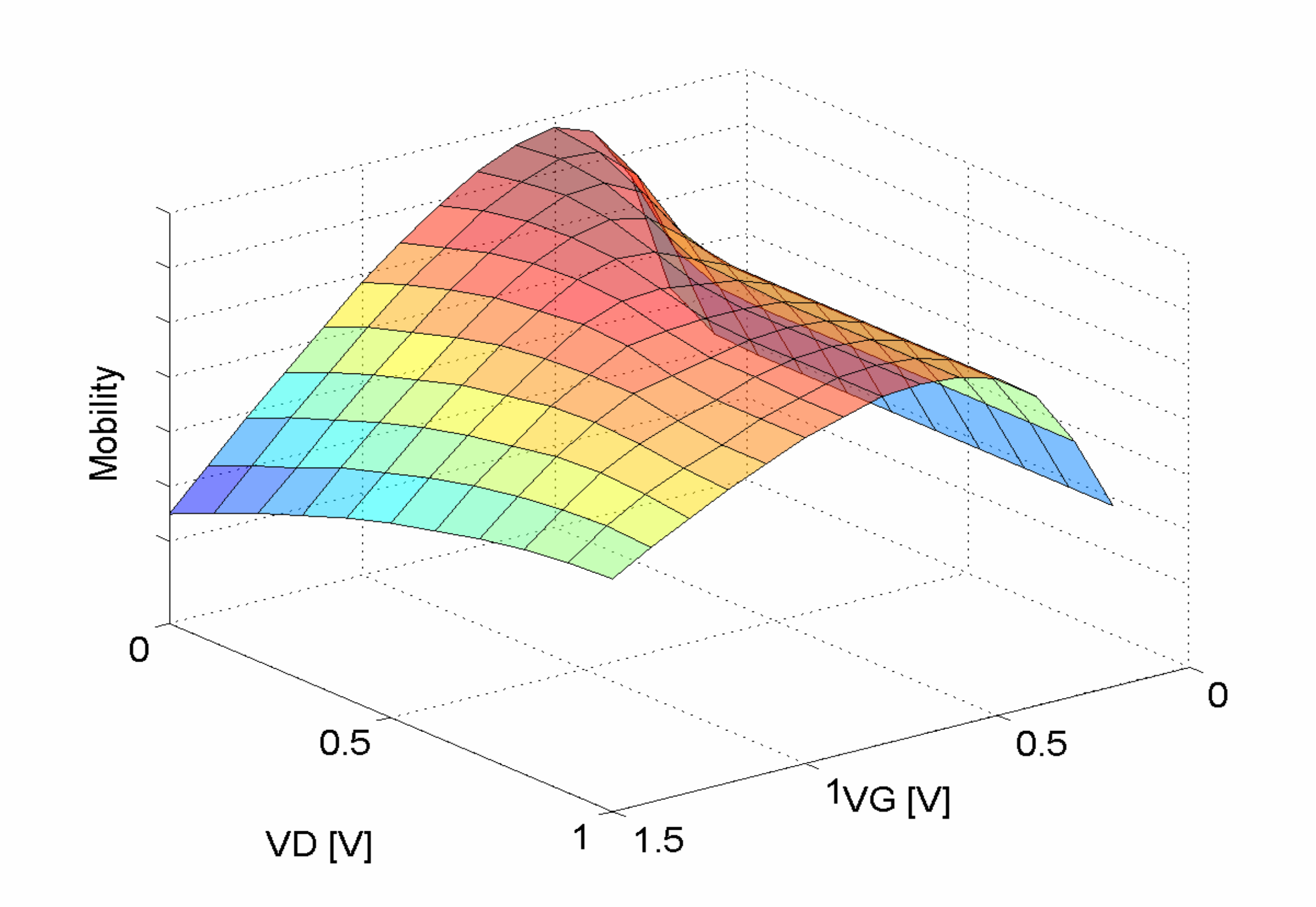






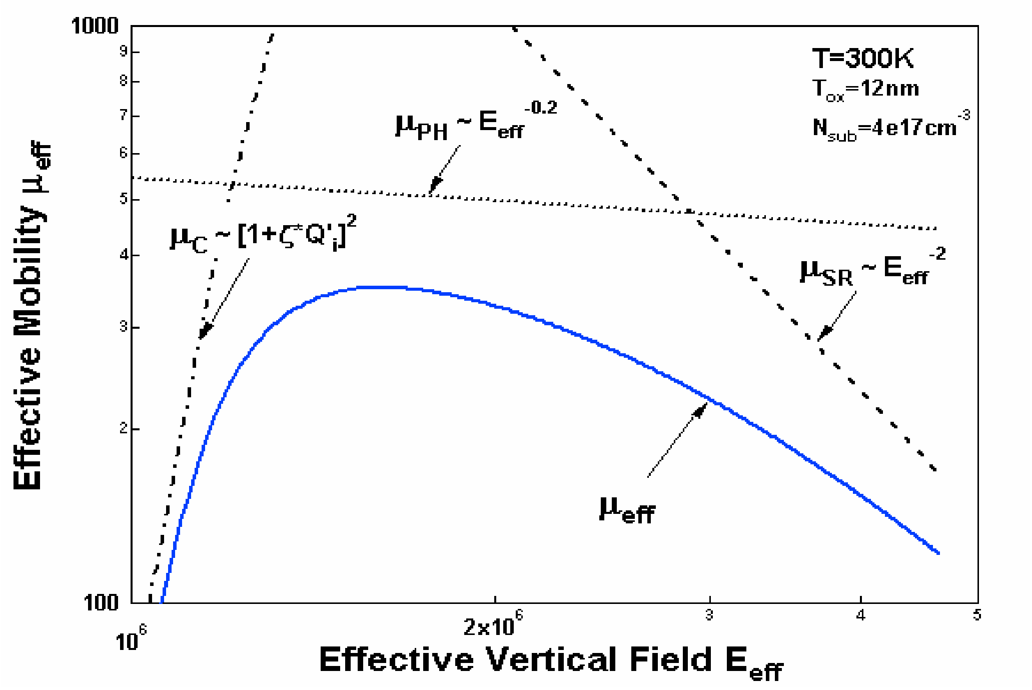


EKV3.0 mobility modeling (I)

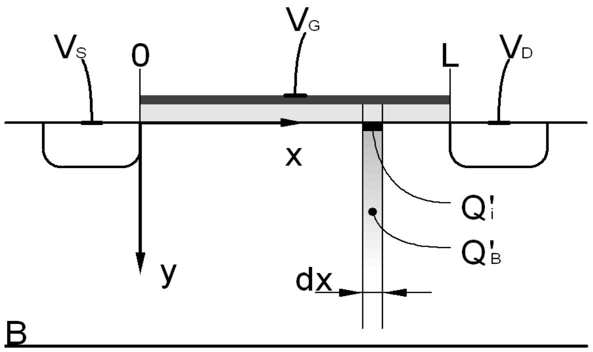


- Mobility versus VG, VD – EKV3.0 simulation
  - Coulomb scattering (low Eeff), surface roughness scattering (high Eeff)
  - Saturation behaviour is included naturally

EKV3.0 mobility modeling (II)

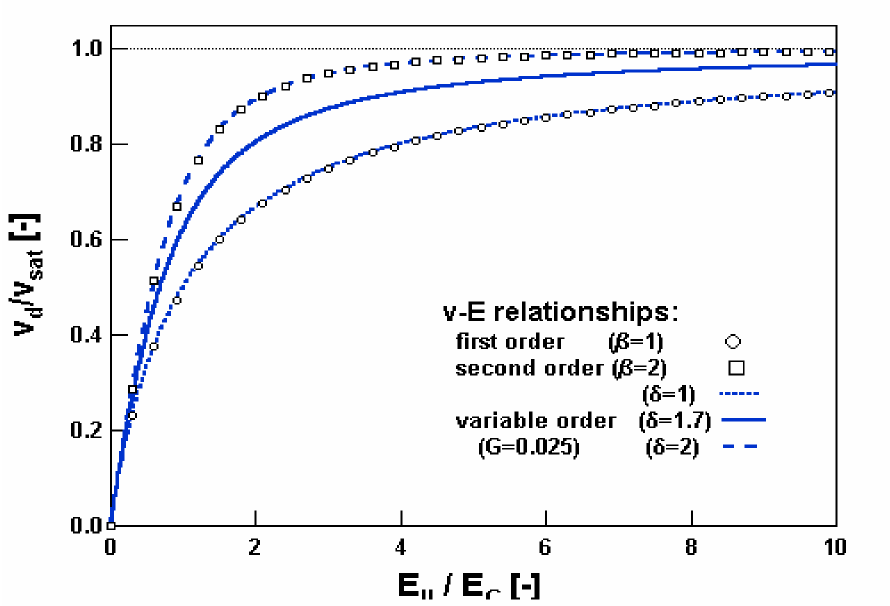


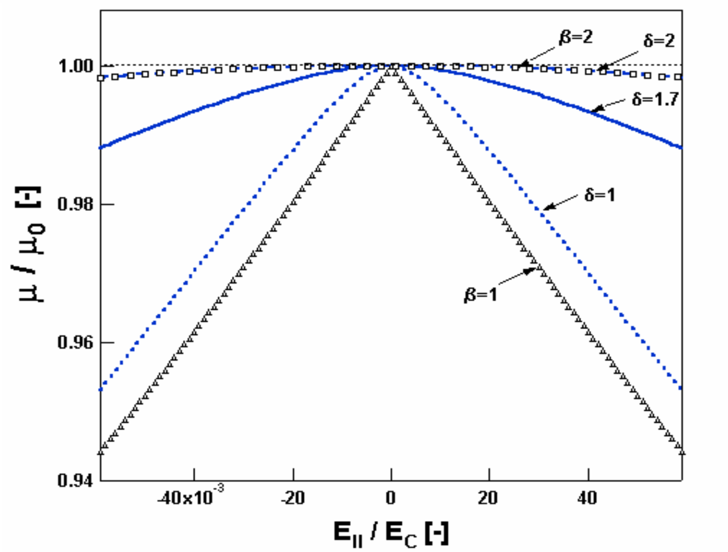
$$E_{eff} \propto Q_b + \eta \cdot Q_i$$



- Effective-field based mobility modeling
  - Surface-roughness scattering (high vertical field)
  - Phonon-scattering intermediate field strengths
  - Coulomb scattering effects (low vertical field; particularly at very high Nsub, low T)
- Local mobility is integrated along the channel
- 5 parameters in all:
  - `E0, E1, ETA, THC, ZC`

Velocity saturation modeling





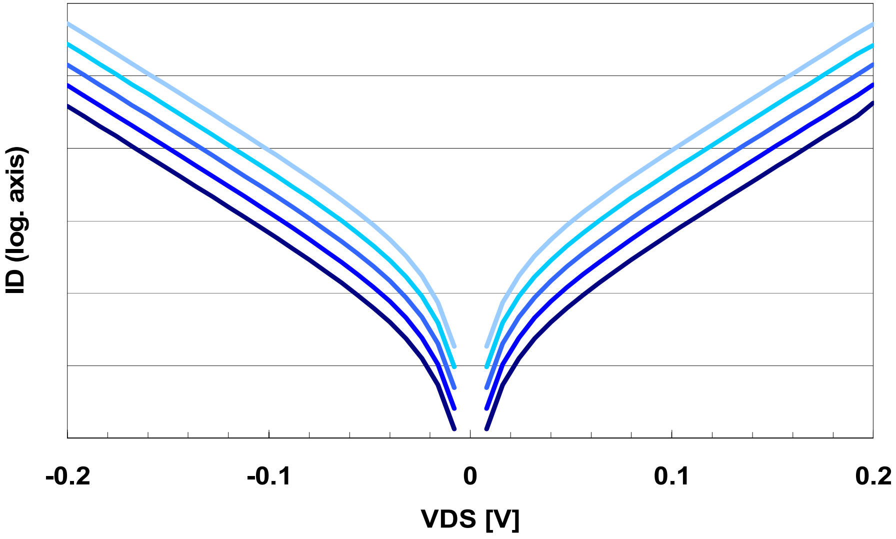
- Consider a *variable-order* (1st-2nd) velocity-field relationship
  - Requires 2 parameters:

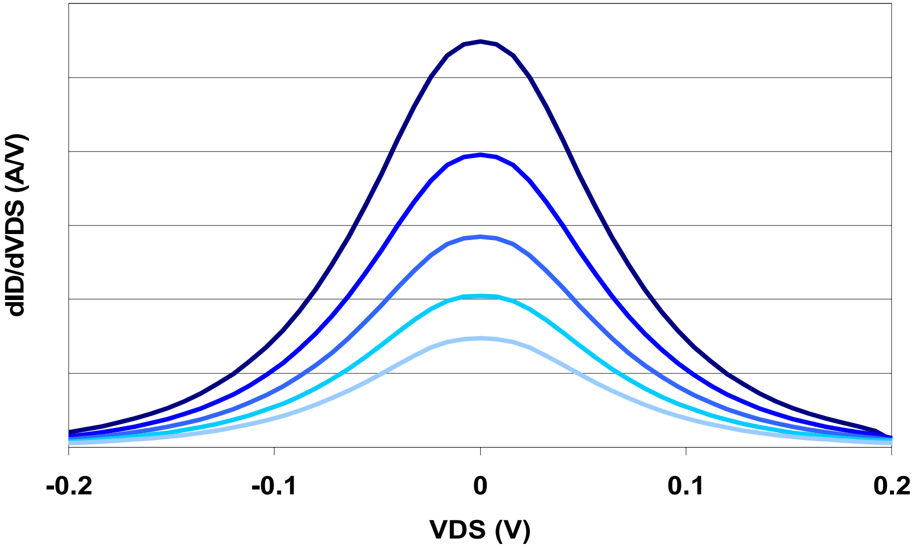
    `UCRIT, DELTA [1..2]`

- New charge-based channel length modulation (CLM) model.
  - *Continuous* at VD=VS

    `LAMBDA`

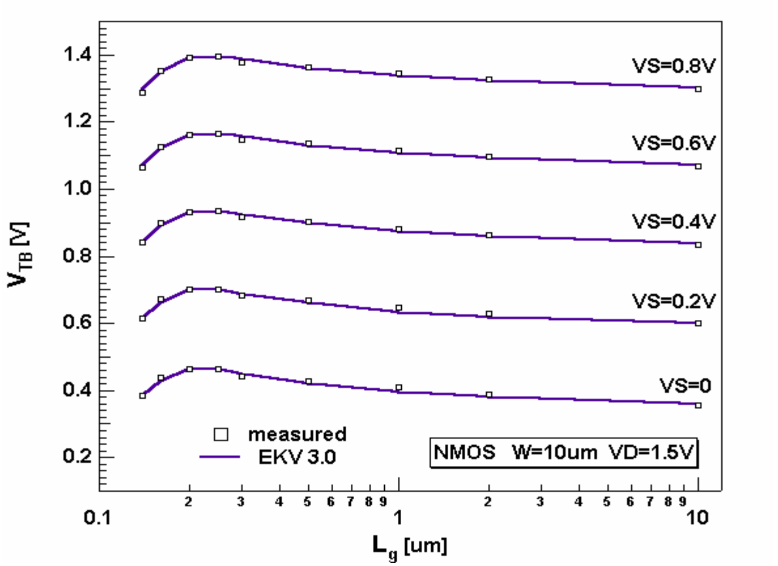
Gummel symmetry test

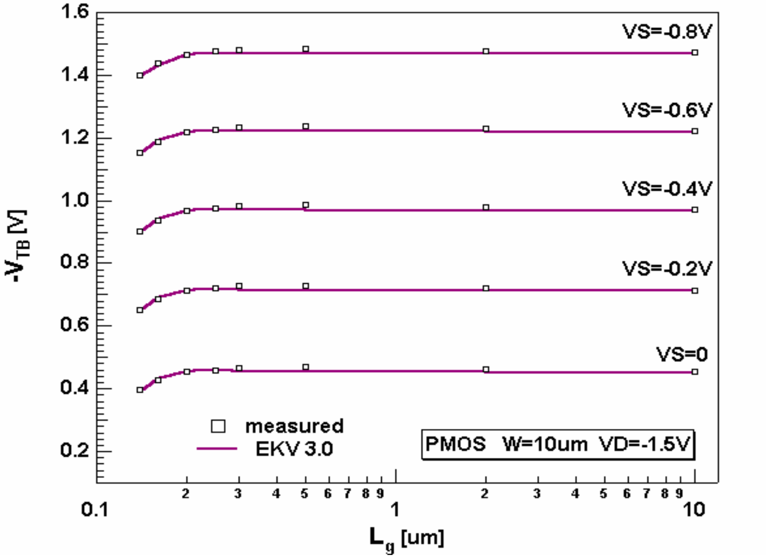




- EKV3.0 fulfills Gummel symmetry test
- All model aspects (mobility, velocity saturation, CLM, DIBL, CS,…) are formulated symmetrically

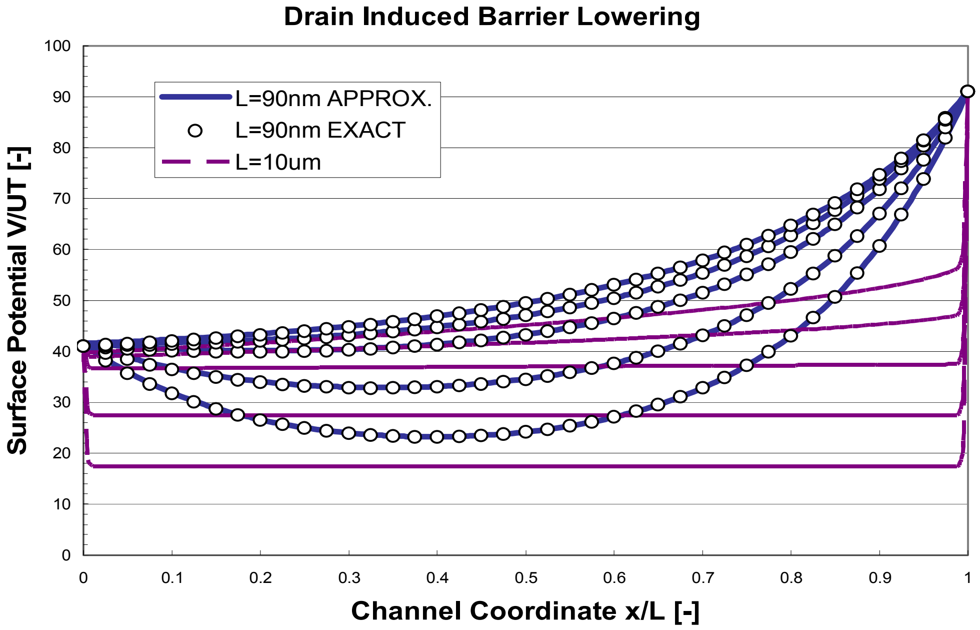
Threshold voltage/RSCE modeling





- Long-channel:
  - Substrate effect
  - Vertical non-uniform doping – NUD
- Short-channel:
  - Lateral non-uniform doping – RSCE
  - Drain induced barrier lowering – DIBL
  - Source/drain charge sharing – CS

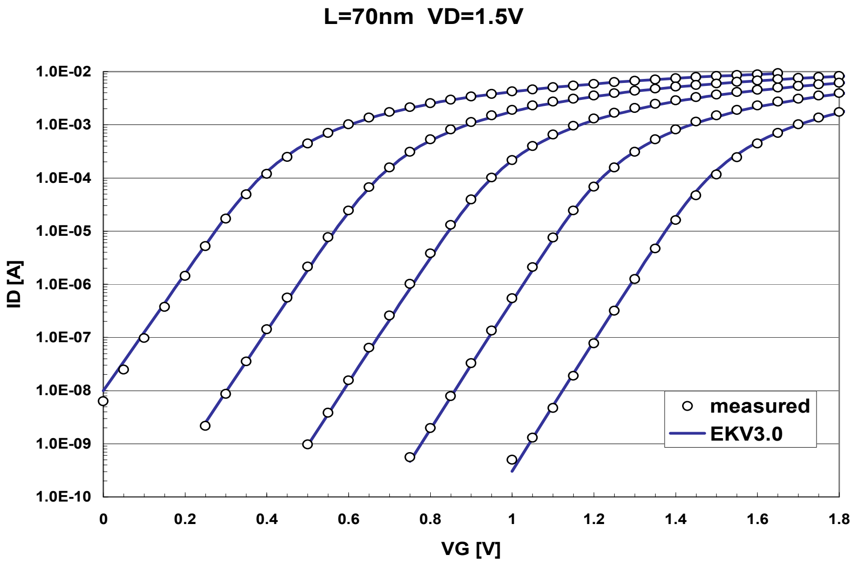
Drain induced barrier lowering

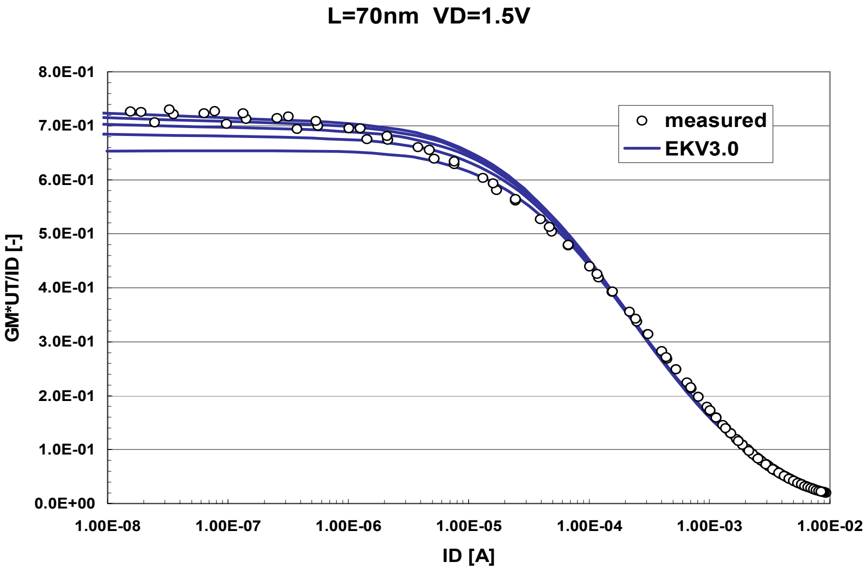


- **Quasi-2D solution for Surface potential, Liu e.a. IEEE TED'93**
- **Symmetric wrt. VD, VS**
- **Approximation uses one single exponential -- no bias dependence in exponential**
- **DIBL model scales with Tox, Nsub, T!** $L_0 \propto \sqrt{\frac{\varepsilon_{si}\gamma}{qN_{sub}}\sqrt{\Psi_0}}$
- 2 Parameters `ETAD`

EKV3.0 – short-channel characteristics

L = 70nm

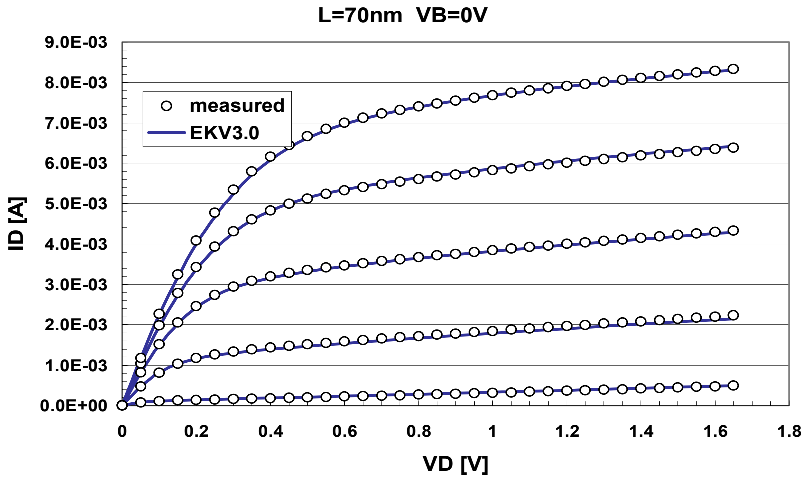


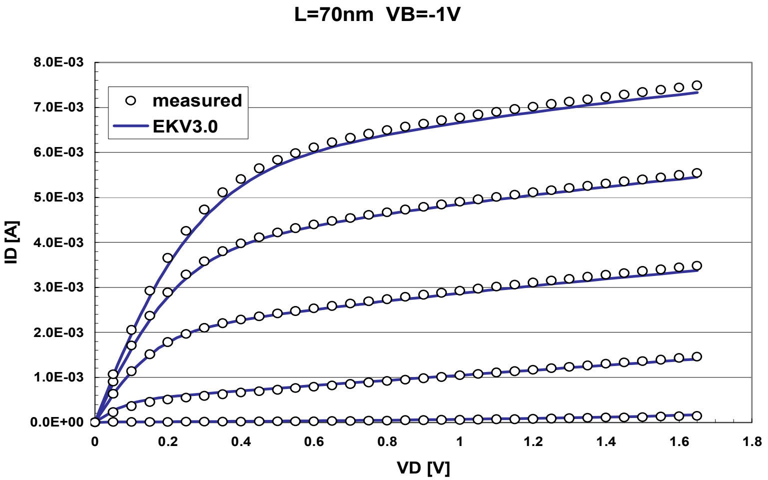


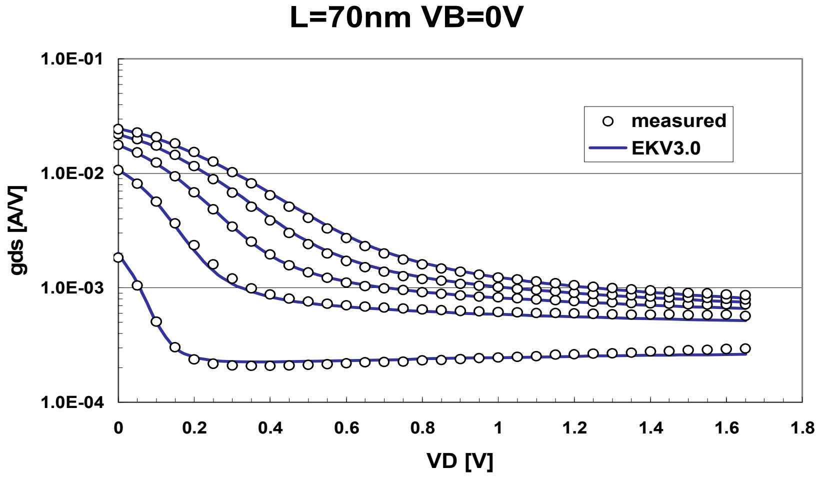
- Correct weak & moderate inversion behavior
  - Smoothness and correct asymptotic behavior
  - Correct weak inversion slope and DIBL modeling
- Transconductance-to-current ratio vs. drain current (log. axis)

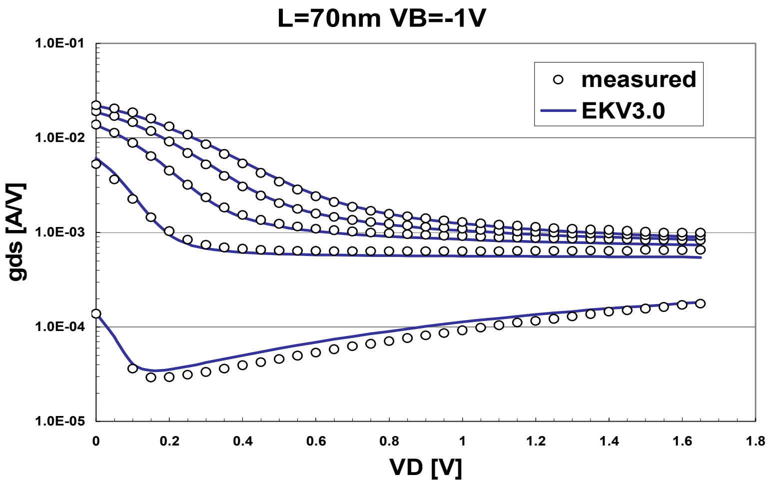
EKV3.0 output characteristics modeling

L = 70nm









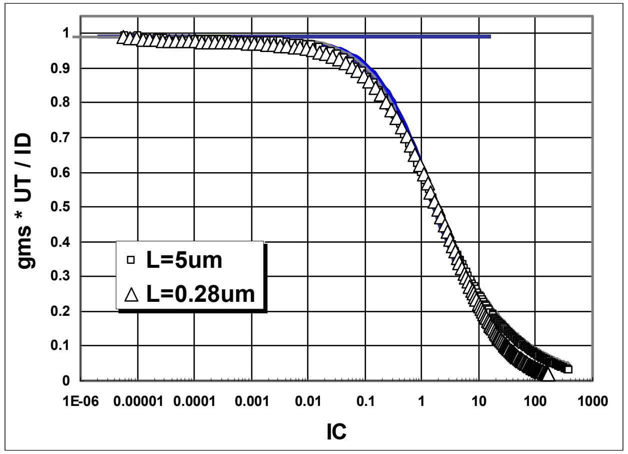
Ongoing R&D for EKV

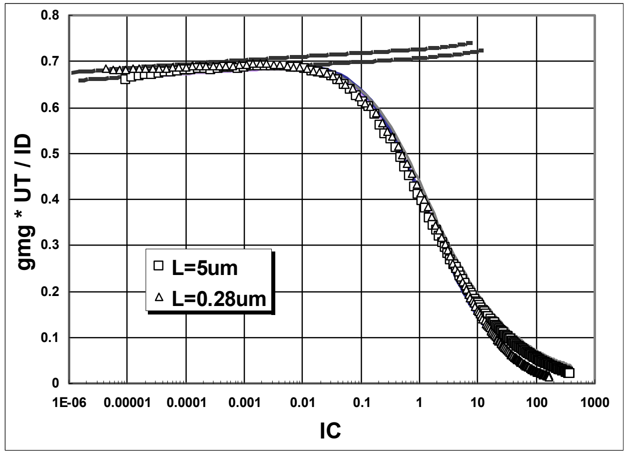
- Noise modeling:
  - Short-channel thermal noise modeling
  - NQS noise modeling: induced noise in gate and substrate
- NQS effects in transient analysis
- Modeling of generation/recombination effects in PD SOI
- Double-gate MOSFET
- Degradation of output conductance in long-channel MOSFETs due to pocket implant

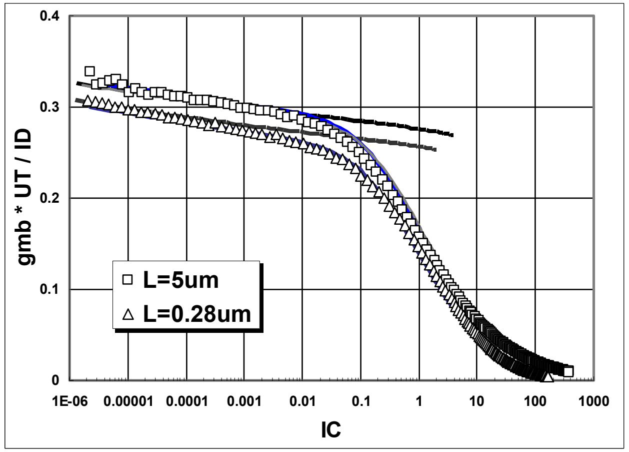
Inversion-level centered design method

- Transconductance to current ratio is a central design variable
- Dedicated measurement method has been developed to measure all transconductances vs. normalized drain current
- Method is useful for:
    - Understanding of CMOS process complexity
    - Direct input to design
    - Development of hand-calculation model
    - Parameter extraction
    - Verification of circuit simulation model
- Method to be complemented with HF gain, linearity, matching, noise,….

EKV3.0 -- normalized transconductances in 0.25um CMOS





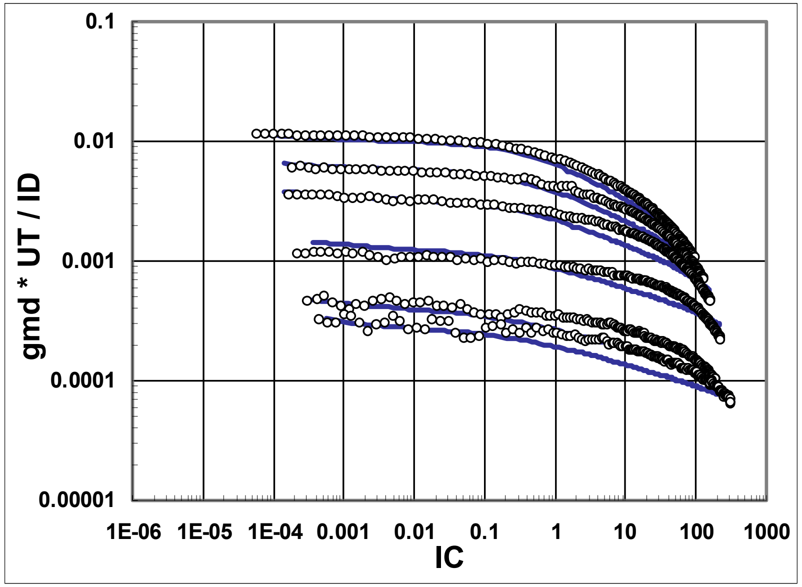


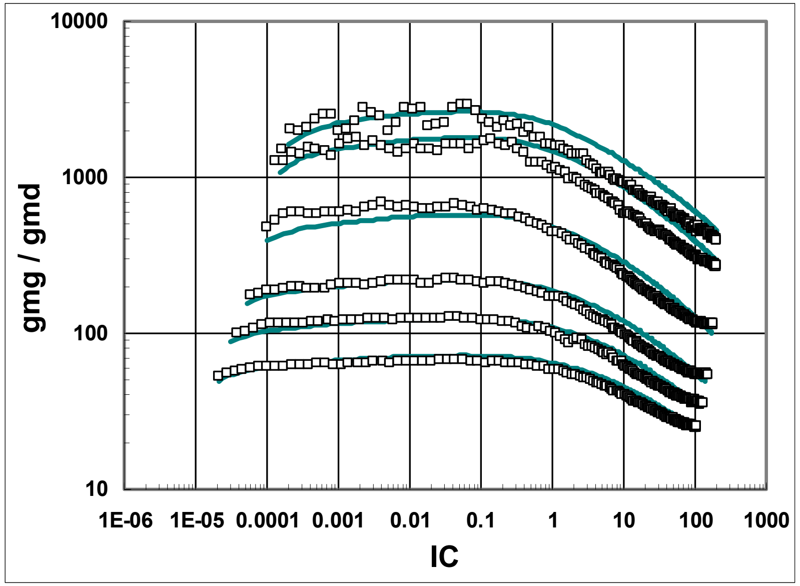
- IC – Inversion Coefficient (in saturation)
- Source-, gate, substrate transconductance vs. IC

$$G(IC) = \frac{1}{\frac{1}{2} + \sqrt{\frac{1}{4} + IC}} \qquad \frac{g_{ms} U_T}{I_D} = G(IC) \qquad \frac{g_m U_T}{I_D} = \frac{G(IC)}{n} \qquad \frac{g_{mb} U_T}{I_D} = \frac{n-1}{n} G(IC)$$

- G(IC) function and slope factor n allow to easily express normalized transconductance vs. Level of inversion
  - Exception in strong inversion/short channel (due to vel. Sat.)

EKV3.0 -- output conductance & self-gain in 0.25um CMOS



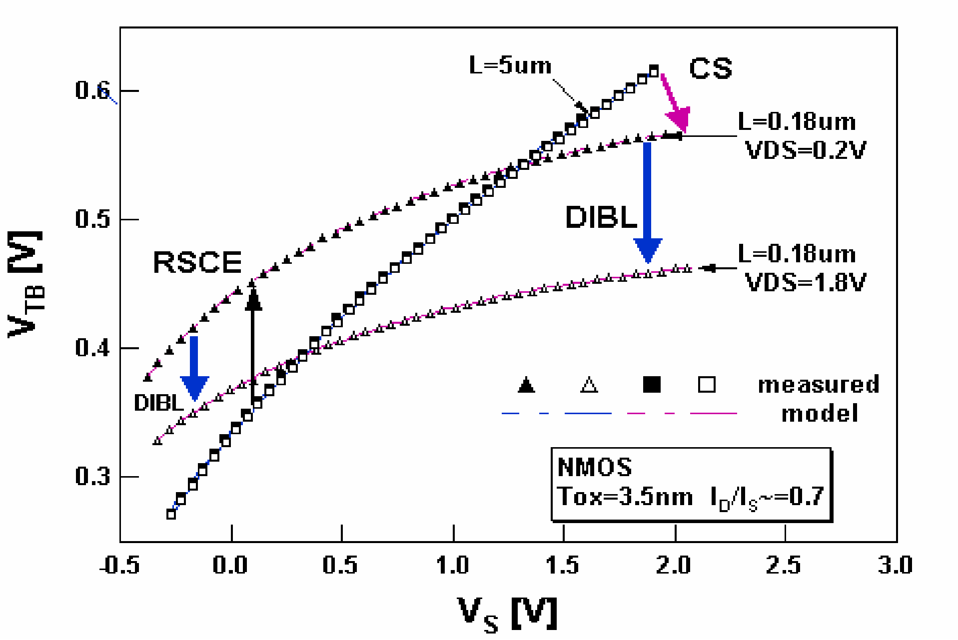


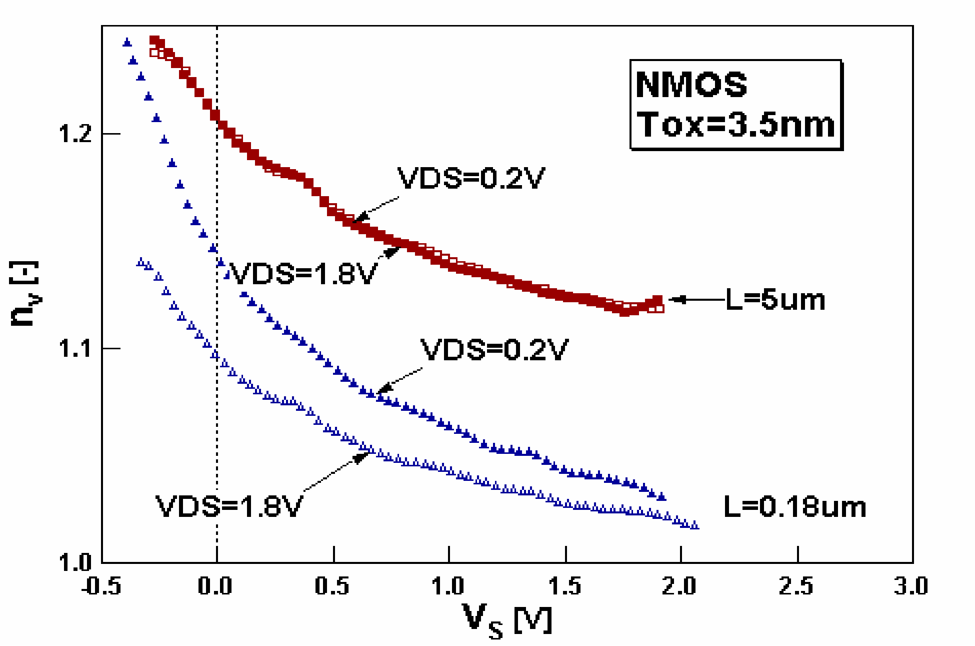
- EKV3.0 shows excellent gmd*UT/ID modelling with IC, L
  - L ranges from 0.28um to 5um

$$\frac{g_{ds} U_T}{I_D} \cong G(IC) \frac{\partial V_P}{\partial V_D} + \frac{U_T}{n} \frac{\partial n}{\partial V_D}$$

- DC self-gain is maximum in weak inversion, long-channel!

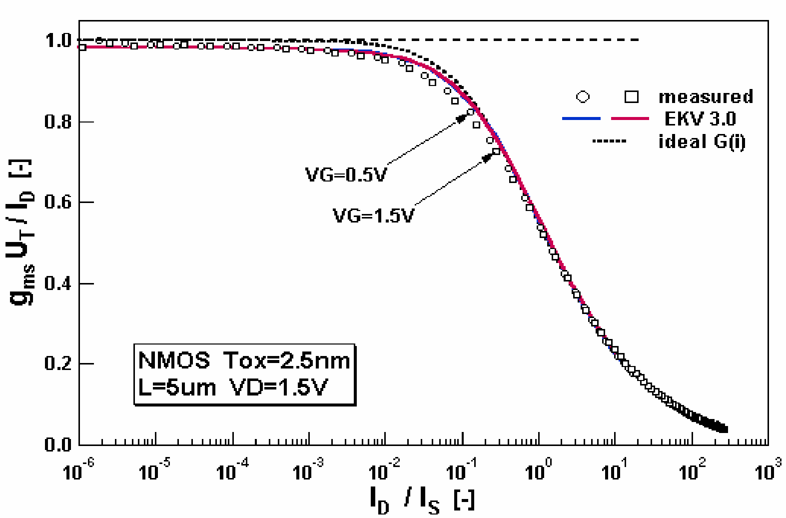
Sensitivity of VP [VT], n vs. VD

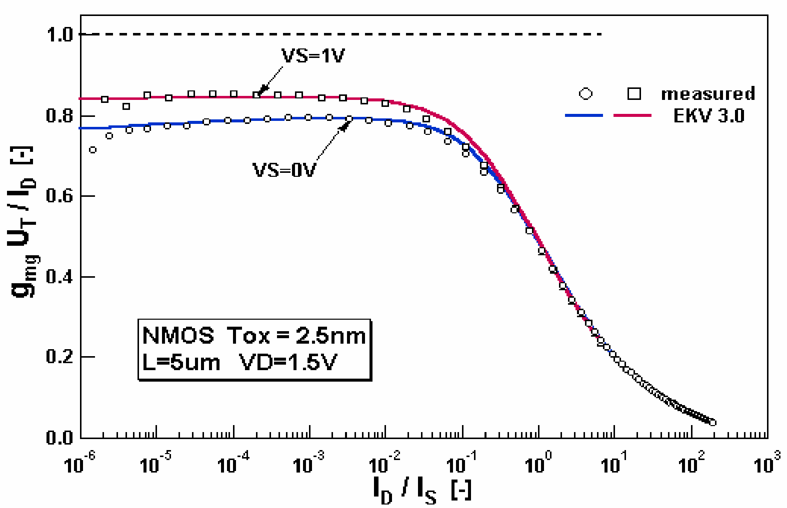


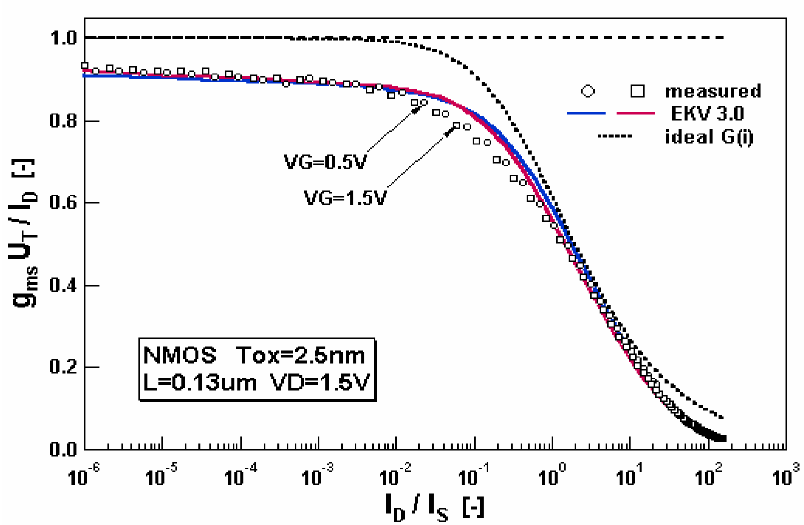


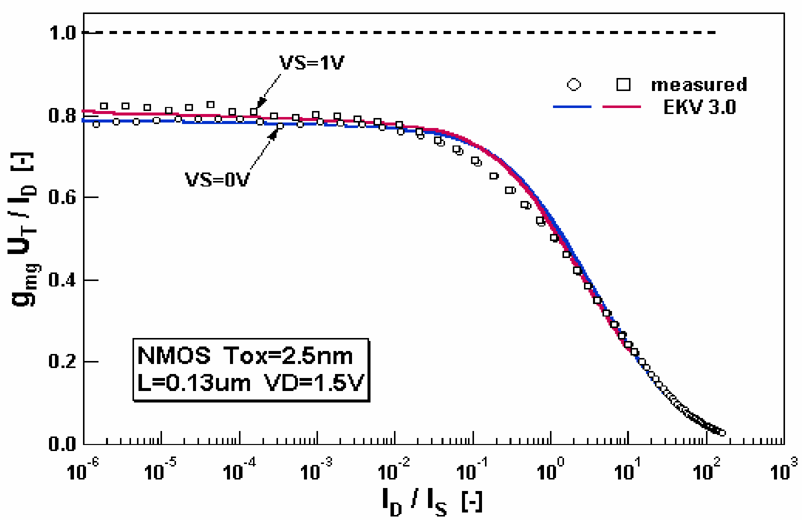
- Illustration of sensitivity of VP [via VT] and n vs. VD
- Explains the degradation of short-channel output characteristic
- Good hand-calculation expression for gds.UT/ID remains a challenge

EKV3.0 – normalized transconductance 0.13um CMOS

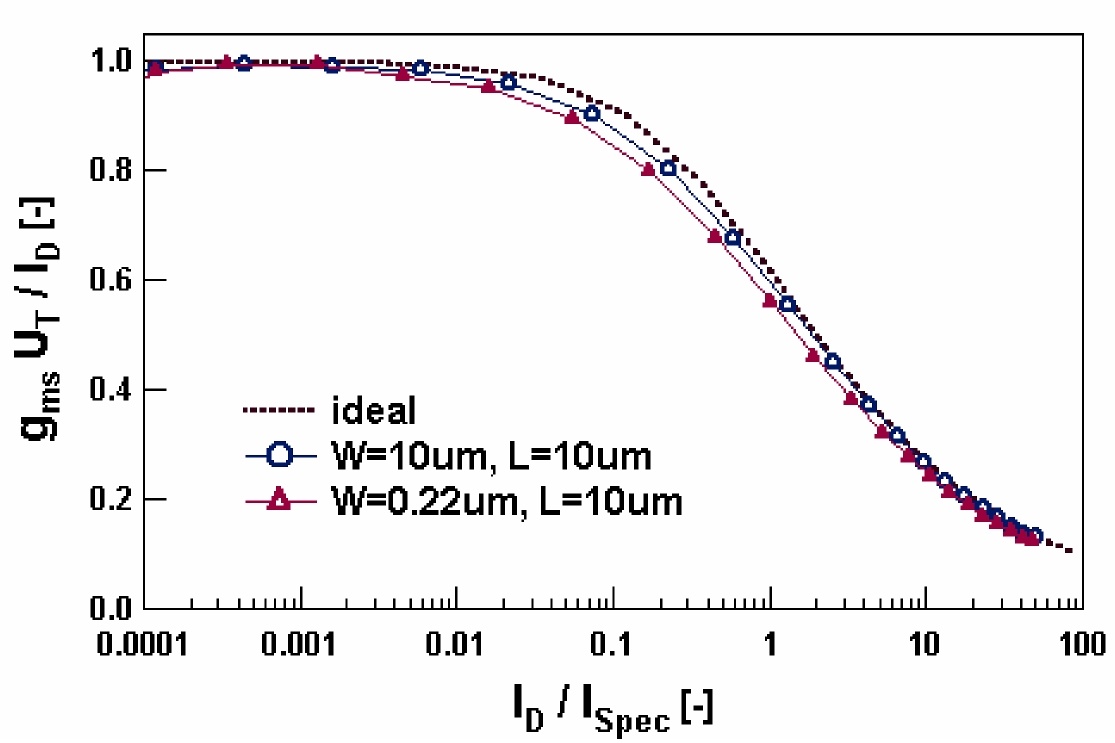






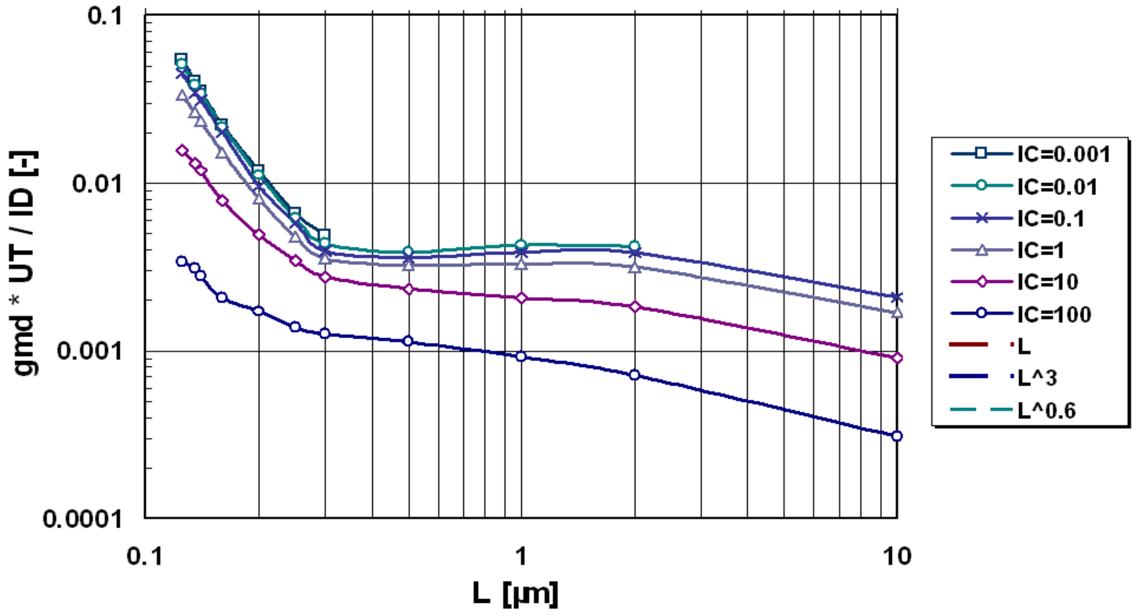


Shallow-trench isoloation (STI) effect



- Narrow devices are affected by stress due to vicinity of ST Isolation
- Degrades G(IC) function in moderate inversion
- STI stress is an important effect in CMOS <0.18um generations

Halo/pocket implant effect on norm. gds, 0.13um CMOS



Weak inversion: IC<0.1
Moderate inversion: 0.1< IC<10
Strong inversion: IC>10

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- Anomalous scaling of output conductance [gds*UT/ID] at fixed level of inversion vs. channel length (meas. only)
  - A dedicated characterization technique has been developed
  - Scaling: L^{-3} (short-channel, weak inversion), $L^{-0.6}$ (long-channel)
  - Pocket/halo implants degrade medium-long channel gds scaling -- severe issue for analog.
  - New model under development.

EKV3.0 summary (I)

- **EKV3.0, a physics-based, *design-oriented* compact model**
  - **Charge linearization principle**
  - **Coherent framework for static-dynamic model, NQS, noise, matching**
  - **Continuous, symmetric forward-reverse operation**
  - **Supports advanced analog IC design practice**

- **EKV3.0 validated for 0.11um CMOS**
  - **Includes all major physical effects for present CMOS technologies**
  - **Favorable efficiency/complexity trade-off**
  - **Number of parameters: ~ 50 (basic intrinsic) + 20 (2nd order scaling)**
  - **90nm CMOS validation underway**

EKV3.0 summary (II)

- **EKV3.0 for next generation CMOS**
  - **Extension of EKV formalism to SOI, double gate, FinFETs, ballistic MOSFET under development**
  - **HVMOS MOSFET model under investigation**
- **EKV3.0 for public-domain**
  - **Code standardization using Verilog-AMS**
  - **Implementations being tested in several simulators**
  - **EKV3.0 model release: “Light Edition” (2004)**
    - **ELDO beta release Jan. 2005**

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- All EKV team
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Contact

Matthias Bucher
Assistant Professor

Technical University of Crete
Dept. of Electronics & Comp. Eng.
73100 Chania, Crete, Greece

phone: +30 28210 37210
fax: +30 28210 37542
bucher@electronics.tuc.gr