New Capabilities for the Verilog-A EKV Model

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Analog Model Portability

Historically, analog models and the simulators in which they are embedded form a single analog simulation kernel.

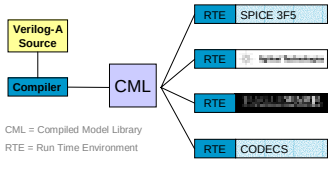
As a consequence, while model interfaces generally serve the same function (allowing the model to define the differential equations of a system), the mechanics of each interface is specific to its simulator. The interface is complex and is tightly interwoven with the analysis engine. Adding a new model such as the EKV to any analog simulator is a task that is measured in engineer-months requiring intimate knowledge of the simulator's architecture and, in many cases, thousands of lines of C code (BSIM4 is ~20k lines in SPICE3).

Verilog-A provides a natural, concise language for describing compact models and new language extensions specifically for compact models have been proposed to the standards committee. However, user acceptance is dependent on the solution supporting all the analyses of native models and comparable simulation performance.

The Technology

The Tiburon solution consists two components, a Verilog-A compiler and a simulation interface library (the latter component is referred to as the *run-time environment* or RTE). Libraries produced by the Compiler are called *compiled model libraries* (CML) and are simulator independent.

The CML file is a shared library that may be used across simulation platforms. Examples of simulators implementing the interface include CODECS, SPICE3f5, Eagleware's GENESYS and Agilent's ADS/RFDE



Adding new complex models to a simulator is now a small investment that may be measured in engineering-days or weeks. The investment is totally focused on model definition. Perhaps the biggest advantage is that the investment is not simulator specific. Once a model has been developed in Verilog-A it may be used in any simulator that supports the Verilog-A standard.

In addition, because of the RTE architecture, the CML file itself is portable across simulation platforms. When comparing simulation results across multiple platforms the user can now assume that any differences observed are not model related as they are using exactly the same compiled model code in all simulators.

Compact Model Examples

The ability to easily add new complex compact models and easily modify existing models opens up a whole new set of possibilities in analog modeling. The complicated relationship between the model developer, the CAD vendor, the foundry and the end user is simplified.

The architecture is designed so that all of the complexity of the compilation process is hidden from the user.

Tiburon has developed a complete set of Verilog-A based compact models as a demonstration on the power of the technology and to provide a starting point for new users of the system. Developers of other models, such as VBIC and EKV, release models in Verilog-A.

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BSIM3, BSIM4.3, BSIMSOI, SPICE
Gummel-Poon, Diode, JFET,
MEXTRAM, MOS 9, MOS 11,
Triquent, Curtice, Parker-
Skellern, Raytheon-Statz,
Angelov, UCSD (Aspeck) GaAs
HBT, HiSIM, Shur-RPI TFT, HICUM
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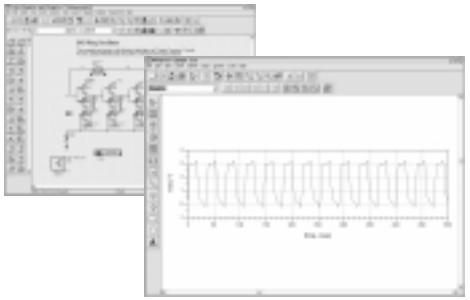
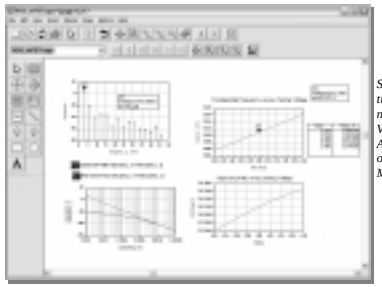
A ring oscillator from the ADS example set is used as an illustration. The circuit was simulated in ADS using the Verilog-A version of the EKV compact model developed by Wladek Grabinski. The Verilog-A model supports all of the analyses available in the simulator. The EKV model is not available in ADS otherwise.



EKV model, version 2.6, implemented in Verilog-A running in Agilent Technologies Advanced Design System.

Complex analyses, including harmonic balance and nonlinear noise, must be supported by the interface for users to use models distributed in Verilog-A. This example shows a VCO using BSIM3 with HB and noise results.

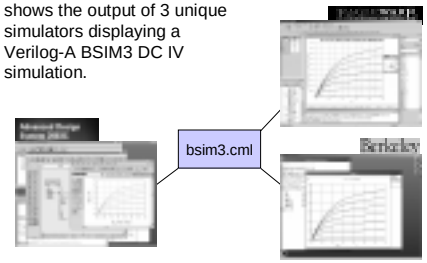
BSIM3, version 3.2, implemented in Verilog-A running in Agilent Technologies Advanced Design System.



Spectral response, tuning range, and noise output of VCO using Verilog-A implementations of BSIM3 MOSFET.

Multiple Simulators Sharing Model

A major advantage of this architecture is that different simulators can share the same compiled model library object file. This example shows the output of 3 unique simulators displaying a Verilog-A BSIM3 DC IV simulation.



Simplified Model Development

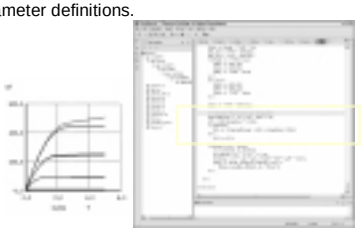
Because Verilog-A calculates the necessary derivative and matrix load stamps, developing new models or extending existing models is greatly simplified. For example, the SPICE Gummel Poon model is approximately 10k lines in C-code, but is just a few hundred lines (including parameter definition) in Verilog-A.

The simplicity of the language for model development is nicely illustrated in an example where self-heating is added to the EKV model.

In C-code, the number of derivatives that need to be calculated for a complicated model can be significant. However, in Verilog-A, the developer only needs to add a simple thermal circuit and shift the device temperature by the associated voltage change due to the power dissipated in the thermal circuit.

This is usually less than a few dozen lines, including all the new parameter definitions.

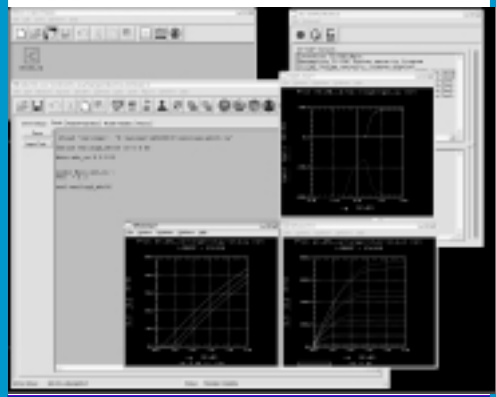
EKV with self-heating thermal circuit added (red), shown with standard model (blue). Note the simple code change.



IC-CAP Parameter Extraction

IC-CAP is a popular parameter extraction program from Agilent Technologies.

IC-CAP works seamlessly with Verilog-A models. The EKV Verilog-A source file need only be placed in a directory available to the search path.



Conclusion

Verilog-A has been demonstrated to be a capable language for describing a wide variety of analog behavior in a diverse set of platforms including commercial and research simulators.

The architecture presented allows relatively easy implementation in commercial and proprietary simulators to provide complete support for compiled Verilog-A., making distribution of models such as the EKV simple. The technology is already available in commercial simulators and more simulators with this capability will be available soon.

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