Analytical noise optimization of the front end amplifiers for silicon detectors using part of the EKV model

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The subject of the optimum noise filtering for the nuclear spectroscopy systems is very broad. Here we present an example of the noise optimization of the CMOS front end amplifiers for readout of the silicon detectors in multi-channel systems. For these applications, in addition to the noise performance of the front end, another important aspect of the design is the simplicity and power consumption of the circuit. A good trade-off between these parameters is use of the conventional band-pass CR-(RC)^n filters consisting of one differentiating and n integrating stages. In that case, the sigma rms value of the noise at the output of the shaper can be obtained simply by integration of the noise spectra densities at the filter output over the full frequency range. Knowing the pulse gain of the processing chain, one can easily obtain the value of the equivalent noise charge (ENC).

In the properly designed charge sensitive preamplifier, the ENC depends on the contributions from the noise sources related to the input transistor and the feedback circuit only. Using elementary network theory it is possible to calculate the propagation of these noise sources to the preamplifier output and after some algebra to obtain expressions for the ENC as a function of the basic transistor parameters like transconductance and gate capacitance. Since from the designer point of view, the basic transistor parameters to be optimized are transistor dimensions and bias current, it is indispensable to calculate accurately the transconductance and intrinsic gate capacitances for each current density.

For that reason we use an analytical EKV model offering simple formulas for the basic transistor parameters and providing the continuity between weak, moderate and strong inversion regions. Since the presented analysis is focused on the noise performance of MOS devices, we simplify the general model assuming that the transistors work in saturation, between the weak and moderate inversion. This assumption allows us for use a constant value of the slope factor n, which is in general case bias dependent, and therefore for limitation of the number of variables and equations without any degradation of the accuracy for the analyzed case.

For the noise simulation we use the model proposed by Van Der Ziel, but slightly modified for moderate inversion region applying an EKV approach for the interpolation of the γ parameter between weak and strong inversion. The excess noise observed in short channel devices is modeled by introducing the excess noise factor Γ. For the example of IBM process we used, the excess noise factor Γ takes values between 1.3 and 1.25 for NMOS and PMOS transistor with the gate length greater the 0.4µm and working in moderate inversion region.

In order to facilitate the calculations we use CERN program ROOT, which offers an user friendly graphical interface for the analytical formulas obtained from the noise calculation.

The presented examples shows;

• optimization of the input transistor dimensions for the given value of the input capacitance and required value of the response peaking time (series noise dominating)

• optimization of the peaking time and transistor dimensions for a given value of the input capacitance and active feedback bias (optimization of the series and parallel noise contributions)

• calculation of the ENC as a function of the input capacitance for a given bias current and peaking time

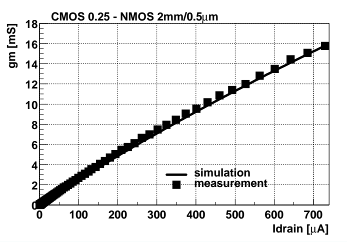


Fig. 3. Comparison between measured and calculated transconductances of an NMOS input transistor for wide range of drain current assuming constant value of the slope factor n.

$$g_m = G(I_f)\cdot\frac{I_D}{n\cdot U_T}$$

$$G(I_f) = \frac{1}{\sqrt{I_f + \frac{1}{2}\cdot\sqrt{I_f} + 1}} \qquad I_f = \frac{I_D}{I_S}$$

$$I_S = 2\cdot n\cdot\beta\cdot U_T^2 \quad \beta = K_P\cdot\frac{W}{L} \quad U_T = \frac{k\cdot T}{q}$$

Fig. 1. Schematic diagram of one channel of the ABCDC1 chip implemented in IBM 0.25um technology. Shaping: CR-RC^3, 22ns peaking time, optimized for 20pF input capacitance.

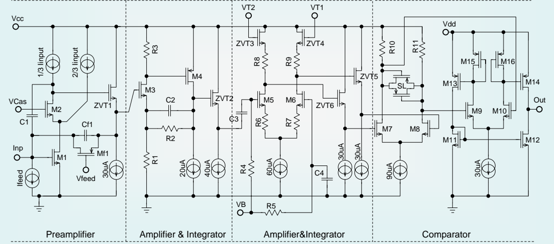
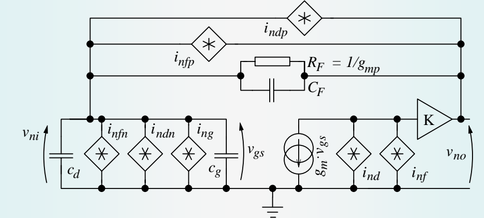


Fig. 2. Equivalent schematic of the transimpedance preamplifier with active feedback including all noise sources related to the input transistor and feedback circuit.



Considered noise sources:

Thermal channel noise: $\overline{i_{nd}^2} = 4\ k\ T\ G_{Nth}\ \Delta f$ where $G_{Nth} = \gamma\ (g_{mb} + g_m) = \gamma\ n\ g_m$

Gate Induced Current noise: $\overline{i_{ng}^2} = 8\gamma\, k\, T\, g_{gs}\, \Delta f$ where $g_{gs} = \frac{4}{45}\frac{\omega^2 C_{OX}^2}{n\, g_m}$

Correlation GIC and thermal: $\overline{i_{ng}\, i_{nd}^*} = \frac{\gamma}{6}\, j\,\omega\, C_{OX}\, 4\, k\, T\ \Delta f$

Flicker noise: $\overline{i_{nf}^2} = \frac{K_a}{f}\frac{g_m^2}{C_{OXU}^2\, W\, L}\,\Delta f$ where $C_{OXU} = \frac{\varepsilon_{OX}}{t_{OX}}$

Where gamma noise parameter is parameterized as:

$$\gamma = F_n(I_f)\ \Gamma \quad \text{where} \quad F_n(I_f) = \frac{1}{1+I_f}\left(\frac{1}{2} + \frac{2}{3} I_f\right)$$

and Γ excess noise parameter must be characterized for a given technology, transistor type, transistor length and inversion region.

Assuming CR-RC^3 shaping of the filter, the ENC partial contribution from the input transistor are as follows:

Thermal: $ENC_{Id}[e-] = \frac{e^3}{12\sqrt{3}}\sqrt{\frac{4kTn\gamma}{g_m}}\,\frac{c_d + c_g + C_F}{\sqrt{t_{peak}}}\,\frac{1}{q}$

GIC: $ENC_{GIC}[e-] = \frac{e^3\sqrt{2}}{9\sqrt{15}}\sqrt{\frac{kT\gamma}{n\, g_m}}\,\frac{C_{OX}}{\sqrt{t_{peak}}}\,\frac{1}{q}$

Correlation GIC and thermal: $ENC_{corr}[e-] = \frac{e^3}{18}\sqrt{\frac{kT\gamma}{g_m}}\,\frac{\sqrt{C_{OX}\,(c_d + c_g + C_F)}}{\sqrt{t_{peak}}}\,\frac{1}{q}$

Flicker noise: $ENC_{If}[e-] = \frac{e^3\sqrt{2}}{9\sqrt{3}}\sqrt{\frac{K_a}{WL}}\,\frac{c_d + c_g + C_F}{C_{OXU}}\,\frac{1}{q}$

Assuming CR-RC^3 shaping of the filter and one AC coupling (τ~300ns) the ENC contribution from the feedback transistors are as follows:

Thermal noise: $ENC_{th}[e-] = \frac{e^3}{18}\sqrt{\frac{5}{3}}\sqrt{kTn\gamma\, g_m t_{peak}}\,\frac{1}{q}$

Flicker noise: $ENC_{1/f}[e-] \approx 2.3 g_m t_{peak}\sqrt{\frac{K_a}{WL}}\,\frac{1}{C_{OXU}}\,\frac{1}{q}$

Results of the analysis and comparison of noise model with the experimental data

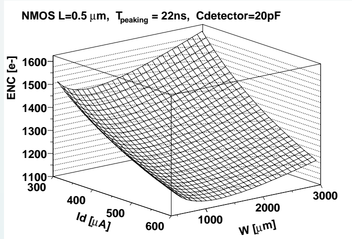


Fig. 4. The ENC related to the input transistor as a function of bias current and input transistor dimensions for 22 ns peaking time and detector capacitance of 20pF. Optimization for the input transistor width for ABCDC1 chip.

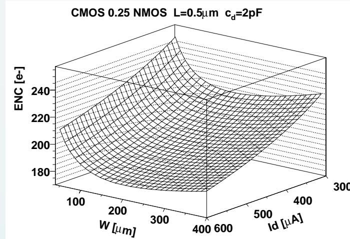


Fig. 5. Optimization of the input transistor width for 22 ns peaking time and detector capacitance of 2pF. Optimum width in the range of 250um.

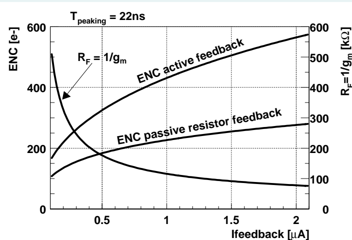


Fig. 6. Comparison of the ENC generated by an active feedback and by a passive resistor of the same equivalent resistance. Left axis shows the ENC and right axis shows the equivalent feedback resistance. ABCDC1 chip.

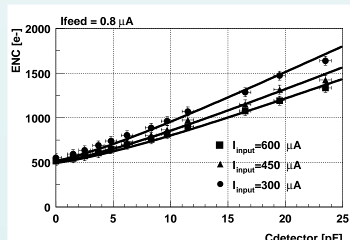


Fig. 7. Total ENC (input transistor + feedback circuit) as a function of the input capacitance measured for different bias currents in the input transistor (points) and calculated noise using noise model based on EKV parameters (lines). ABCDC1 chip.

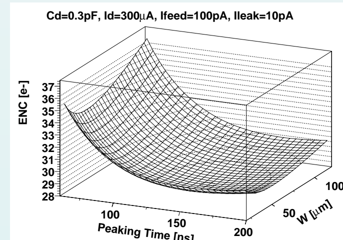


Fig. 8. Optimization of the transistor width and the peaking time for the MACROPAD chip (readout of thin film a-Si:H). Considered ENC contributions from input transistor and active feedback circuit. Results: optimum peaking time 160ns, transistor width 80um, ENC of 30e- for 0.3pF input capacitance (good agreement width experimental data).