EM MICROELECTRONIC - MARIN SA

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Needs in modeling of 0.18um EM processes: past experience and future requirement

EM process development
development + industrialization:
own processes + options (… 0.50um, 0.35um, … 0.18um)

device models → **design support** → DK for **BUs**

↑

external IC production

Needs in modeling of 0.18um B (baseline), F (flash) + options:

- specific MOSFET model not preferred, but
- specific model features required
- EM has specific needs different from general purpose foundry processes

Any MOSFET model selected and applied must be:

1. **Physics based**
   - due to EM modeling methodology:
     model for basic devices (1.8V, 3.3V, HV) → model for other devices
     - remote D HV N/PMOST
     - remote SD HV N/PMOS
     - inv. gate LV/HV N/PMOST
     - ESD devices
   - generation of model corners from basic in-line and electrical PCM data
   - link of model parameters with statistical process control
   - designers may read basic MOSFET parameters from the design-kit library file, for initial hands-on design

2. **Should perform with no bins (or just a limited number),**
   due to: a) analog design
   b) (huge) job for model verification (bin matching at the borders)

   Some exceptions allowed: e.g. HV 1.5um for 10-15V, and HV 1.0um for 5.0V.

3. **Model must include DIBL effect**
   real $\phi_{bS}(V_{DS})$ effect,
   not just ΔV_{th} due to charge-sharing

   Needed in modeling of native LV, MV and HV MOST that shows huge DIBL effect at shorter gate lengths and increased Vds (even, for Vds just above 0.1V).
   We need DIBL effect dependent on W, as well.

4. **Must include poly-gate depletion**
   - for MOSFETs
   - for MOS capacitors (target N+ gate/Nwell LV, MV and HV capacitors)

5. Noise model needed

SPECTRE ≡ HSIM

6. Matching model needed

7. Model for HV (lateral) MOST (probably) needed

- lateral MOST (not LDMOST), with Nwell/FOX remote drain
- if request for 20V devices availability, then devices should be characterized, defined in DK and modeled

8. Good MOSFET RF model, potentially will be required in ALP018B/E

- 0.18um process attractive for EM RF business development
- core MOSFET basic (DC and low-f AC) models should be extendable to RF MOSFETs

9. Good model for MOSFET junction diodes

- IV forward o.K.
- CV reverse o.K.
- IV reverse – not acceptable for LV and MV (in EKV 2.6)

10. Must implement narrow-width and inverse-narrow-width effect

- both simultaneously on the same device (with W variation)
  $\Delta V_{th}(W) > 0$ and $\Delta V_{th}(W) < 0$
- desired effect of short L on $\Delta V_{th}(W)$

11. Non-uniform bulk doping model

For some devices, in some applications, accurate model of back-bias effect required, due to non-uniform bulk doping profile

12. Must provide identical results in HSIM and SPECTRE implementation

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