ACTIVITY REPORT

2023-2024

EUROPRACTICE

Results

We have managed to design, send to fabrication, and perform measurements of the 2048-channels integrated circuit dedicated to photon counting detectors. The measurements with an X-ray beam performed at bending magnet beamline in the European Synchrotron Radiation Facility in Grenoble showed that the chip's count-rate performance exceeds largely currently existing detectors. This has been achieved mainly thanks to the special readout features implemented in SPHIRD, the pile-up compensation methods, the pixel relocation algorithms, and TSMC 40nm process used.

Additionally, the on-chip pixel relocation techniques reduce the photon losses at the pixel corners opening the door to the implementation of detectors with pixel pitch smaller than 50 µm. Importantly, moving to smaller pixels will not only increase the intrinsic spatial resolution of the detector, but also allow to better exploit the subpixel relocation modes.

Why EUROPRACTICE?

AGH University has benefited from the EUROPRACTICE offer for many years, with a lot of successful tapeouts. EUROPRACTICE offers affordable fabrication of our prototypes in MPWs and mini@sics and provides access to a wide variety of design tools. It is an essential partner in our research.

Acknowledgements

The chip design was realized by P. Grybos, R. Kleczek, P. Otfinowski, and P. Kmon (AGH UST) while synchrotron experiments were conducted by P. Fajarado, D. Magalhaes, and M. Raut.

References

[1] P. Grybos,et.al., "SPHIRD–Single Photon Counting Pixel Readout ASIC With Pulse Pile-Up Compensation Methods", IEEE IEEE Transactions on Circuits and Systems--II: Express Briefs, vol. 70, no. 9, 2023, p. 3248-3252.

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HEEPocrates: An Ultra-Low-Power RISC-V Microcontroller for Edge-Computing Healthcare Applications

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Technology: TSMC 65nm LP MS/RF
Die Size: 2mm x 3mm
Design Tools: Siemens Questasim, Synopsys Design Compiler, Cadence Innovus
Application Area: Healthcare

Introduction

The field of edge computing in healthcare has seen remarkable growth due to the increasing demand for real-time processing of data in applications. However, challenges persist due to limitations in healthcare devices' performance and power efficiency. To overcome these challenges, heterogeneous architectures that combine host processors with specialized accelerators have emerged, leading to improved performance and power consumption.

In this work, we present HEEPocrates, an ultra-low-power RISC-V microcontroller for edge computing healthcare applications. The chip combines the open-source eXtendible Heterogeneous Energy-Efficient Platform (X-HEEP) [6] with a coarse-grained reconfigurable array (CGRA) [3] and in-memory computing (IMC) [7] accelerators, both of which are efficient in reducing the energy consumption of healthcare applications [2].

Description

Figure 1 shows the HEEPocrates architecture and how the CGRA [3] and IMC [7] accelerators are integrated.

The X-HEEP host platform [6] is configured with:

1) a CV32E20 core [5], which is optimal for running control tasks and offloading performance-intensive computations to the external accelerators;
2) 8 SRAM banks of 32 KiB to accommodate variable lengths of data while power-gating the unused banks;
3) a fully connected bus to provide high-bandwidth capabilities to the CGRA [3];
4) all the available peripherals in place to deliver high flexibility;
5) a CGRA [3] and IMC [7] accelerators connected to the external eXtendible Accelerator InterFace (XAIF).

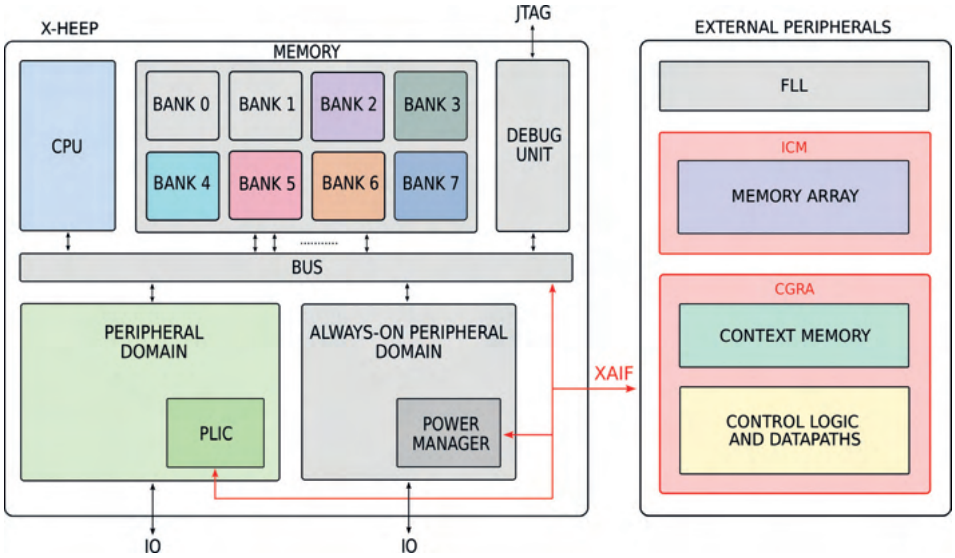

Fig.1: HEEPocrates architecture. Power domains are visually marked using different colors. The components highlighted in grey are always on. The accelerator integration is marked in red.

The design includes 11 power domains, marked with different colors, which can be independently clock-gated or power-gated when unused to reduce power consumption. Memory banks can also be set in retention mode.

Results

Figure 2 shows the HEEPocrates layout, the silicon photo, and the physical realization. The chip has been tested from 0.8 V to 1.2 V, achieving a maximum frequency of 170 MHz and 470 MHz, respectively. The power consumption ranges from 270 µW in 32 kHz and 0.8 V, to 48 mW at 470 MHz and 1.2 V.

To validate the design, we measured the energy consumption of healthcare applications running on the host CPU of HEEPocrates and on state-of-the-art microcontrollers commonly adopted in this application domain.

The selected microcontrollers cover the spectrum of ultra-low-power edge devices, ranging from top-tier power efficiency, with Apollo 3 Blue, to top-tier performance, with GAP9. Similarly, the benchmark covers the spectrum of ultra-low-power healthcare applications, ranging from acquisition-dominated, with heartbeat classifier [1], to processing-dominated, with CNN for seizure detection [4].

We have measured each application phase at each microcontroller's optimal frequency and voltage configuration. For HEEPocrates, we have run acquisition phases at 1 MHz, 0.8 V to reduce power while offering enough performance to acquire bio-signals in the order of hundreds of Hertz, and processing phases at the maximum speed of 170 MHz, 0.8 V to minimize processing time and race to sleep.

Figure 3 shows the energy alignment of HEEPocrates with the selected microcontrollers for both computationally hungry and acquisition-dominated healthcare applications. This demonstrates the real-world suitability of the chip for this application domain, known for its strict power and performance constraints.

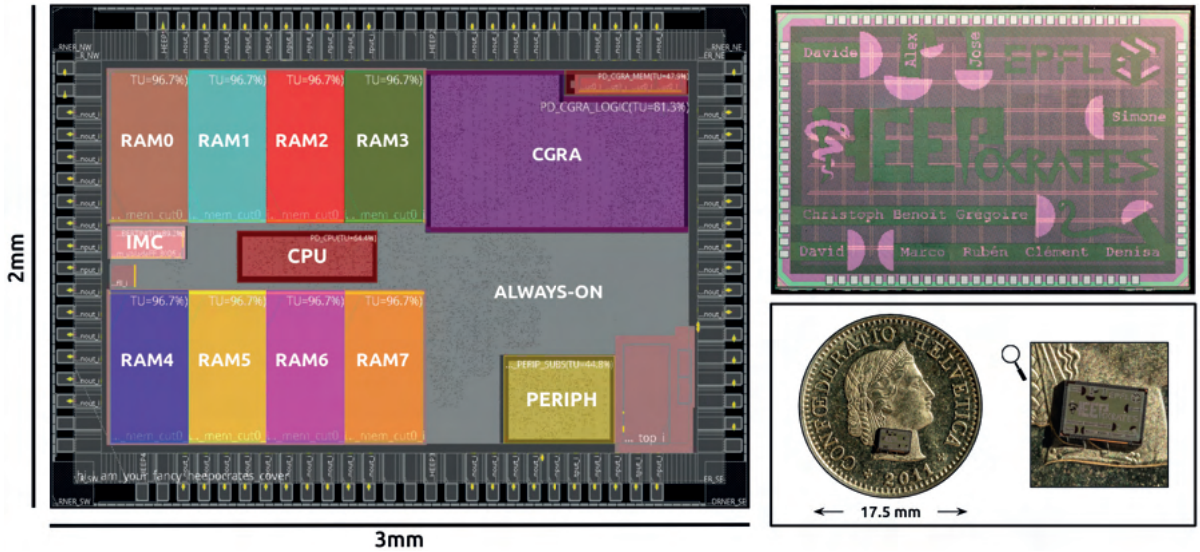

Fig.2: HEEPocrates layout, silicon photo, and physical realization (on a Swiss 5-cent franc coin).

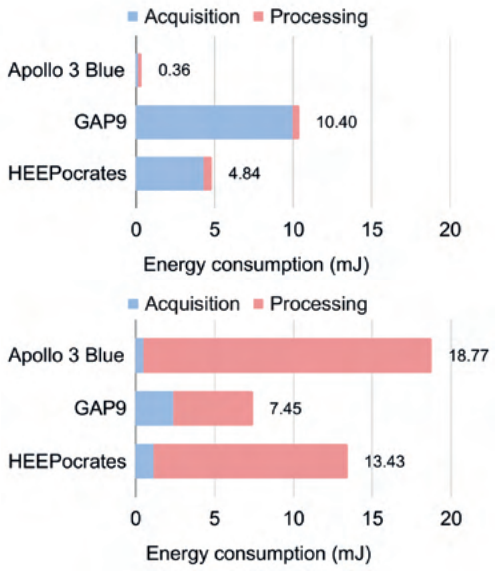

Fig.3: Energy consumption of the benchmark running on relevant healthcare microcontrollers and on HEEPocrates. (a) Heartbeat Classifier. (b) Seazure Detection CNN.

Why EUROPRACTICE?

EUROPRACTICE support is a key element in the success of this project. Their assistance in acquiring EDA tool licenses, access to technology design kits, participation in their mini@sic MPW program, and the design support from their team, which addresses all sorts of tricky questions, are extremely valuable for universities. Having such a partner is a great asset for EPFL, enabling high-quality research on systems-on-chips (SoC).

References

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PicoTDC: 64 channels Time to Digital Converter with ps time resolution

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Die size: 5mm x 5mm
Design Tools: Cadence design tools
Application Area: High Energy Physics (HEP)

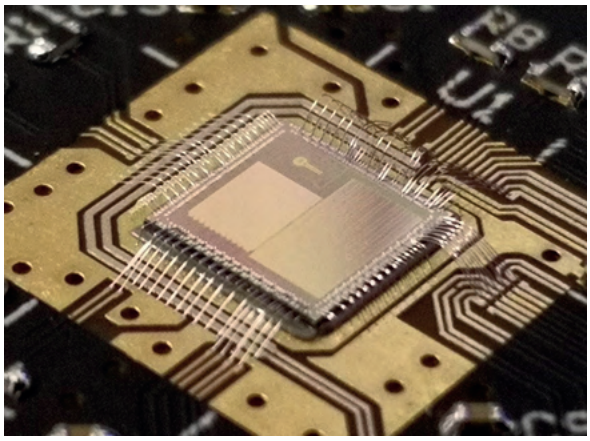

Fig.1: PicoTDC directly wirebonded to test board.

Introduction

The HEP community has an increasing need for very high time resolution measurements on a large number of channels for Time Of Flight (TOF) detectors and similar applications. The PicoTDC chip has therefore been developed as a successor of a previous TDC (named HPTDC), extensively used in the HEP community during the last 15 years.

Description

The PicoTDC is a 64 channel Time to Digital Converter (TDC) ASIC that can measure the time of digital signals with a time binning of 3ps or 12ps. Digitized timing of leading and/or trailing edges can be buffered on chip and also have the possibility to be filtered based on a trigger with configurable latency and time window.

The time of signal edges are measured relative to an input reference clock of 40MHz and digitized using on a very low jitter 1.28GHz PLL (Phase Locked Loop) followed by a time interpolator DLL (Delay Locked Loop), getting to a final timing binning of 3/12ps. Measurements are encoded to contain timing information of leading edge and/or trailing edge or alternatively

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Chips JU

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