Embedded Systems Laboratory (ESL)
Director: Prof. David Atienza Alonso http://esl.epfl.ch

Hardware accelerator design with Chisel and integration in a RISC-V full system

☐ Contact:

ESL - Ruben Rodriguez Alvarez (ruben.rodriguezalvarez@epfl.ch)

ESL - Dr. Denisa Constantinescu (denisa.constantinescu@epfl.ch)

SCALA Center - Jamie Richard Thompson (jamesrichard.thompson@epfl.ch)

SCALA Center - Anatolii Kmetiuk (anatolii.kmetiuk@epfl.ch)

ESL - Prof. David Atienza (david.atienza@epfl.ch)

Project Description

Background and motivation

The aim of this project is to design a **specialized hardware accelerator** for a real-world Machine Learning (ML) **keyword spotting** algorithm for wakeword command voice detection (e.g. “Hey Siri, turn on the lights”). In particular, you will use **Chisel**, a hardware construction language embedded in **SCALA** for agile hardware design. You will have the opportunity to test your design in an FPGA and explore different optimization opportunities. Finally, you will be able to test the keyword spotting application execution by integrating your accelerator in a state-of-the-art RISC-V open-source platform: **X-HEEP** (eXtendable Heterogeneous Energy-Efficient Platform). Moreover, through this process, you will collaborate with experienced engineers and researchers from the Embedded Systems Lab (ESL) and SCALA Center.

The RISC-V open-hardware initiative removed the high-cost barriers imposed by the industry when designing hardware and enabled the development of X-HEEP by ESL and EcoCloud Sustainable Computing Center. X-HEEP is a low-cost RISC-V microcontroller for running end-to-end applications and can be extended with hardware accelerators. A specialized hardware accelerator is a digital circuit that optimizes the latency, energy consumption, and hardware resources of a given application. **Throughout this project, you will gain hands-on experience with open-source tools developed by the RISC-V community and used by the industry and academia to design novel digital circuits for hardware accelerators.**

This project targets accelerating an ML application by designing hardware accelerators with **Chisel**. Chisel is a Hardware Construction Language (HCL) proposed as an alternative to the traditional Hardware Description Languages, such as Verilog and VHDL to describe hardware designs. Chisel is a hardware library embedded in **Scala:** a high-level, general-purpose language that features a blend of functional and object-oriented programming paradigms. This combination enables developers to express complex ideas more concisely than many other languages, significantly reducing the amount of code required. Scala facilitates abstraction over hardware. It allows for the efficient capturing of hardware patterns using high-level language constructs, enabling the description of more hardware scenarios with less code compared to traditional languages like SystemVerilog. You can think of the combination of Scala and Chisel as a flexible templating system. Furthermore, Scala enhances circuit testing through the Chisel workbench, a high-level framework that simulates circuits. This approach simplifies testing to the ease of evaluating a software function, marking Scala as an instrumental tool in both software and hardware development realms.

This project presents an exclusive opportunity for you to work with ESL and SCALA Center to experience globally-used tools developed at EPFL. You will be working with X-HEEP, an open-hardware platform from ESL that has gained attention from both industry and academics to deploy real-world applications. You will also be working with SCALA, developed by the SCALA Center, which has various applications beyond the domain of digital circuits, such as data engineering and processing at scale. It is utilized in the infrastructures of popular web services like Disney Streaming and Netflix, making it a highly valuable skill in the tech industry. In addition, you will be able to exploit the extended potential of digital design with Chisel, supported by the combined expertise of engineers and researchers of the two groups.

This project has the following **learning objectives**:

- You will practice the hardware design process: specification, design, test, integration, and validation
- you will know how to accelerate a real-world application with specific hardware accelerators
- You will be able to use the extended potential of the Chisel library embedded in SCALA to efficiently describe hardware accelerators
- You will integrate a hardware accelerator with the X-HEEP framework to simulate the full application
- You will be able to present and communicate the design decision making and results
- You will learn scientific inquiry-based skills by analyzing the application, formulating a hypothesis of design, testing your design, questioning and interpreting the results

Prior knowledge required

- Previous experience (project or course) in any hardware description languages such as VHDL or Verilog.
- Previous experience (project or course) working with Xilinx FPGAs.
- Previous experience (project or course) with C, C++ programing languages.
- Previous contact (project or course) with ML concepts and algorithms.

Type of work: 25% theoretical analysis, 75% design and experiment execution.

References

- X-HEEP GitHub: https://github.com/esl-epfl/x-heep
- Chisel introduction: https://www.chisel-lang.org/docs
- Scala webpage: https://www.scala-lang.org/