Multi-Processor System-on-Chip (MPSoC) Thermal Behavior Exploration Based on HW/SW FPGA-Based Emulation

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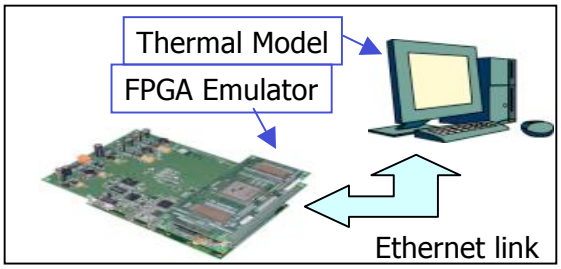
Presentation

New applications ported to embedded systems (scalable video rendering, wireless protocols) demand single-chip multi-processor designs to meet their real-time requirements while respecting other critical embedded design constraints (low-power or implementation size). In this context, Multi-Processor Systems-on-Chips (MPSoCs) have been proposed as a promising solution. Nevertheless, one major new design challenge is how to select the most suitable MPSoC architecture in future technologies when the final system shows an alarming temperature rise on the die.

In order to explore the HW/SW interaction, MPSoC simulators have been developed at the transaction and cycle-accurate levels, using HDL languages and SystemC. Also, several SW tools recently developed can be added to them to evaluate thermal pressure in on-chip components based on run-time power consumption and floorplanning information of MPSoCs. Nevertheless, these complex SW environments are limited in performance (circa 100 Khz) due to signal management overhead. Thus, such environments cannot be used to analyze MPSoC solutions with complex applications. Moreover, higher abstraction levels simulators attain faster simulation speeds, but at the cost of a significant loss of accuracy. Hence, they are not suitable for fine-grained architectural tuning and thermal modeling.

One solution for the speed problems of cycle-accurate simulators is HW emulation. However, it is usually very expensive for embedded design (between $100K and $1M). Moreover, it is not flexible enough for MPSoC architecture exploration since they mainly aim at large MPSoCs prototyping or SW debugging. Typically, the baseline architectures (e.g. processing cores or interconnections) are proprietary, not permitting internal changes. Furthermore, no flexible interconnection interfaces between HW emulation and the existing SW thermal libraries exist today. Thus, thermal effects can only be verified in the last phases of the design process, when the final components are available, which can produce large overheads in the production process due to cores and overall MPSoC architecture redesigns.



Goal

The purpose of this project is to design an efficient HW/SW FPGA-based emulation framework that enables exploring a large number of design alternatives of MPSoCs at cycle-accurate level, while exploring their thermal characteristics in real-time. This work involves defining flexible HW emulation interfaces for on-chip MPSoC components interacting in real-time with a SW thermal model running on a host computer via an Ethernet port. Our current results have shown speed-ups of three orders of magnitude compared to cycle-accurate MPSoC simulators when performing thermal modelling of MPSoCs. Future work in this research line includes development of run-time thermal management strategies for MPSoCs with real-life inputs.

Publications:

- **"A Fast HW/SW FPGA Based Thermal Emulation Framework for MultiProcessor System-on-Chip",** David Atienza, Pablo G. Del Valle, Giacomo Paci, Francesco Poletti, Luca Benini, Giovanni De Micheli, Jose M. Mendias, accepted for Proceedings of the ACM/*IEEE Design Automation Conference (DAC '06)*, San Francisco, USA, to appear in July 2006.