Efficient Emulation Mechanisms and Scalable Interconnection Paradigms (NoCs) for MPSoC Systems

Personnel: **Prof. David Atienza (david.atienza@epfl.ch)**

Partners: **Computer Architecture and Automation Department (DACYA)**, UCM, Spain; **Electrical Engineering and Computer Science (DEIS),** Bologna Univ., Italy;

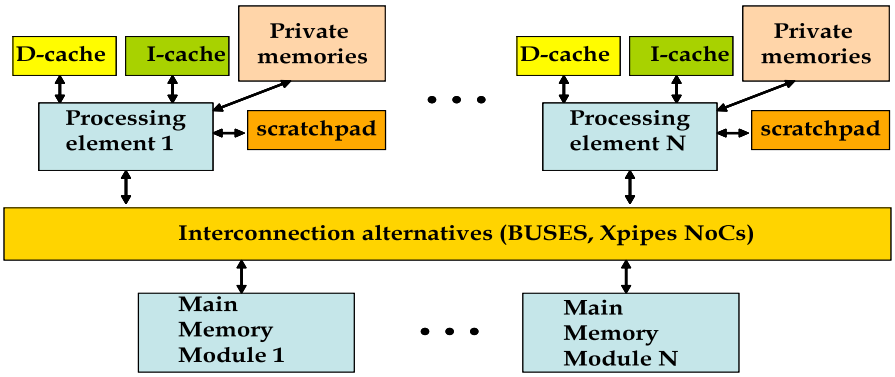
Keywords: *emulation systems, FPGA, hardware/software co-design, buses, processing cores*

Presentation

With the growing complexity in consumer embedded products and the improvements in process technology, Multi-Processor System-On-Chip (MPSoC) architectures have become widespread. These new systems are very complex to design as they must execute multiple complex real time applications (e.g. video processing, or videogames), while meeting several additional design constraints (e.g. energy consumption or time-to-market). Therefore, mechanisms to efficiently explore the different possible HW/SW design interactions. In order to overcome these problems of efficient modeling of MPSoC systems we propose the use of FPGA emulation, which attains significant speedups compared to cycle accurate mpSoC simulators. Additionally, we include in our emulation framework the exploration of the Network-On-Chip (NoC) interconnection paradigm, a technology recently proposed as a promising replacement for buses and dedicated interconnections.

Goal

The goal of this research line is to explore how to extract realistic statistics of mpSoC systems with many cores via FPGA-based emulation mechanisms without deteriorating the performance of such frameworks as occurs with state-of-the-art cycle-accurate simulators. Also, in this line it is studied the complex design space of the new NoC on-chip intercommunication paradigm versus complex high-performance buses.



Example of baseline MPSoC architecture considered

Publications:

- **"Network-on-Chip design and synthesis outlook"** David Atienza, Federico Angiolini, Srinivasan Murali, Antonio Pullini, Luca Benini, Giovanni De Micheli, Integration, 41(3), pp. 340-359, 2008.
- **"A Complete Network-On-Chip Emulation Framework",** Nicolas Genko, David Atienza, Giovanni De Micheli, et al., in Proceedings *DATE '05*, pp. 246-251.
- **"NoC Emulation on FPGA: HW/SW Synergy for NoC Features Exploration"**, Nicolas Genko, David Atienza, Giovanni De Micheli, in Proceedings of *ParCo '05*, pp. 115-122.
- **"Versatile FPGA-Based Functional Validation Framework for Networks-on-Chip Interconnections Designs"**, Javier B. Perez Ramas, David Atienza, et al, Proceedings of *ParCo '05*, pp. 140-147.