Dynamic Memory Management for Embedded Systems

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Presentation

New multimedia and wireless network applications are interactive and dynamic in nature. Therefore, the minimum/maximum power consumption levels can be significantly different. Also, they include thread-level parallelism, and portable devices run several applications concurrently. All these factors cannot be overlooked to design a low-power system from a memory efficient point of view. In addition, latest embedded systems are implemented using very high-level abstraction languages (e.g. C++ or Java) to achieve modularity, and platform-dependent optimizations are only applied much later, in the final mapping phase. Thus, these implementations are usually over-dimensioned in most of the cases and will hence waste cost and power, so the most common solution is to select a cheaper implementation that will occasionally suffer performance problems or not handle dynamic memory and rely on automatic garbage collection mechanisms in Java.

Goal

The goal of this research line is to develop the necessary new methodologies to overcome the aforementioned present design limitations and to suitably implement this highly dynamic new multimedia applications, e.g. MPEG-4 video systems, Quality of Service (QoS) 3D rendering, 3D games, etc., in current embedded and portable consumer devices. Therefore, we refine the systems and applications at different abstraction levels starting from high-level (C++, Java), to the final hardware/software implementation on embedded devices. Key steps include optimization of the dynamic data types used by the algorithm to interact with the OS and refinement of dynamic memory managers at the OS level.
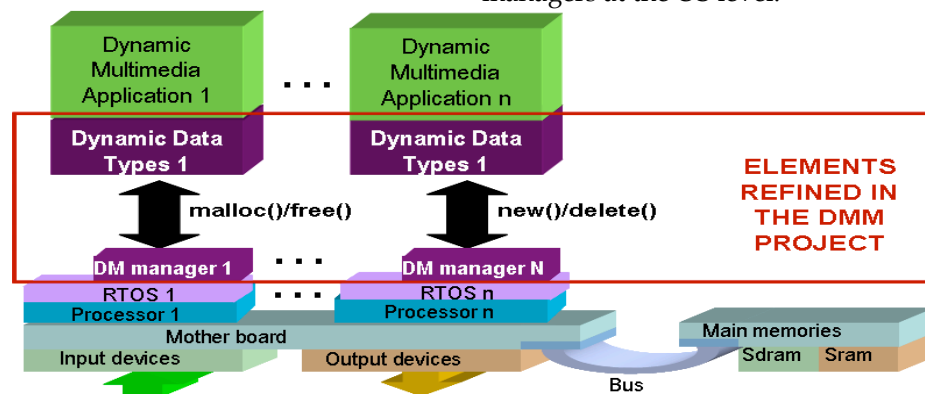
Publications:

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- **"Systematic Dynamic Memory Management Design Methodology for Reduced Memory Footprint"**, David Atienza, et al., *ACM TODAES*, 11(2), pp. 465-489, 2006.
- **"Energy Characterization of Garbage Collectors for Dynamic Applications on Embedded Systems"**, Jose Manuel Velasco, David Atienza, et al. Proceedings *PATMOS*, pp. 69-78, 2005.
- **"Memory-Access-Aware Data Structure Transformations for Embedded Sw with Dynamic Data Accesses"**, E. G.Daylight, David Atienza, et al., *IEEE Trans. on VLSI*, pp.269-280, 2004.