École Polytechnique Fédérale de Lausanne
Distributed Electrical Systems Laboratory
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http://desl-pwrs.epfl.ch

# Student project proposal

*Project title*
Deployment of a synchrophasor estimation algorithm into an FPGA

*Project type* ☒ MSc thesis ☐ BA semester project ☒ MSc semester project

*Project responsible and e-mail*
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*Project description*
As largely documented by the existing literature, the continuous development of stochastic and low-inertia renewable energy sources can significantly impact the fundamental operational aspects of modern powers systems. In such a context, an accurate and reliable measurement infrastructure is vital to ensure the secure operation of this vital infrastructure. Indeed, the essential power systems applications like: wide area monitoring, state estimation, control and protection do require time-synchronised measurements provided by Phasor Measurement Units (PMUs). As known, these devices estimate the magnitude, phase angle, frequency, and Rate-Of-Change-Of-frequency (ROCOF) of the so-called *synchrophasors* associated to AC voltage and current waveforms. The aim of this project is to deploy a novel synchrophasor estimation algorithm into an FPGA-based PMU prototype.

The algorithm employs a second-order generalized integrator (SOGI) quadrature signal generator (QSG) filter to attenuate the self-interference of the fundamental tone within the acquired sampled voltage/current signal delivering a reduction in the total computational cost. The method combines such a filter with a three-point IpDFT and a three-cycle Hanning window to further address the effects of short- and long-range spectral leakage. Deployment of the algorithm in a commercial NI FPGA and designing an optimal distribution of the method tasks and subroutines is key to comply with the PMU standard latency requirements for P-class devices. Moreover, it is vital to guarantee that an adequate level of accuracy is kept when the method is migrated to the embedded device and programmed with FXP precision not compromising its total computational cost and speed.

*Tasks of the student*
- Deploy an existing synchrophasor estimation algorithm into an FPGA
- Conduct experimental validation of the experimental results and compare them to a simulated benchmark.

*Requirements*
- Good LabVIEW programming skills.
- Good Matlab programming skills or at least capability to read/understand Matlab code.
- Familiarity with embedded systems is a plus.
- Previous experience with cRIO hardware is a merit.

*Literature*
Details on previous related projects can be found here:
- https://infoscience.epfl.ch/record/200060
- https://infoscience.epfl.ch/record/279450