MS Diploma and Semester Projects offered at the Biomedical and Neuromorphic Microelectronic Systems research group during the fall/winter of 2026-2027

Students are asked to contact the project responsible to register. The majority of the projects are proposed as MS Diploma and Semester or BS semester, and the amount of work will be adapted. Also, some projects can be carried out in groups of two students.

Projects are proposed in six categories in the following pages.

- Analog and mixed-signal circuits
- Digital circuits and modeling
- Bio-electronic interfaces and biomedical applications
- Fabrication technologies
- Industrial projects / external projects (for MSc diploma)
- Application development (software development)

Please contact us if you have your own idea, wish to propose a collaborative project topics e.g. in industry, or wish to start an external collaboration, e.g., internship

List of projects

Analog and mixed-signal circuits and modeling

A1 **Reservoir computing for robust generation of complex temporal patterns**

Reservoir computing is a neuromorphic model that supports modeling of some cortical areas. In a simple model, nonlinear units (neurons) are organized in a sparsely recursively connected topology forming a reservoir to which a single input is provided. Several units deliver a single output to a single output unit. Only the connection strengths to the output neurons are modified by a learning algorithm, such as the FORCE learning algorithm. As a result, a reservoir has the capacity of synthesizing nonlinear functions, within a certain range of complexity. These signals can be used to the purpose of controlling biological or engineered systems.

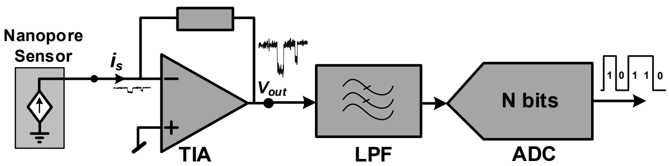
The robustness of the entire system to faults (single or multiple event faults), as well as variations is studied in this project. A model of reservoir is developed in C/Matlab/Python language. Fault models are introduced. A strategy to counter the effect of faults is developed. An analysis study of the results using various waveforms (applications) is presented.

Project breakdown:
Literature survey: 20%
Software modeling and simulations(C/Matlab/Python language): 80%

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A2 **An Integrator-Differentiator Transimpedance Amplifier for Nanopore Sensing Systems**

Nanopore recording systems have recently become highly attractive for single molecule detection and DNA sequencing. This is due to their advantages, which include label-free operation, ultralong read lengths, high throughput, low material requirements, and low cost. In these systems, an ionic current flows through the nanopore by applying a bias voltage across it. When a molecule passes through a nanopore, the current is disrupted in picoampere level. The molecule characteristics can be studied by recording the fluctuation of the current. The recording system consists of a low-noise transimpedance amplifier, a low-pass filter, and an analog-to-digital converter.
In this project, the student will first study the concept of low-noise transimpedance amplifiers and do a literature review. The main task of the project is to design a low-noise and highly-linear integrator-differentiator transimpedance amplifier circuit and verify its performance by transistor-level simulations in a CMOS technology. The students will gain considerable hands-on experience in analog circuit design and the Cadence environment.



Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

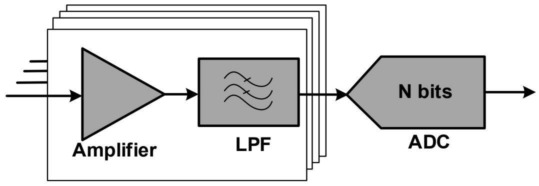
Project Breakdown:
• 30% Literature review
• 60% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A3

A Low-Power Multi-Channel Front-End Circuit for Biological Recording Systems

Multi-channel front-end recording systems are widely used in biomedical, biological, and sensor recording systems. Typically, each channel of the system consists of a low-noise amplifier, a low-pass filter, and an analog-to-digital converter (ADC). However, some blocks (e.g., the ADC) can be shared between the channels to improve the efficiency of the system.



In this project, the student will first study the concept of multi-channel front-end recording systems and do a literature review. The main task of the project is to design a low-power 8-channel interface circuit and verify its performance by transistor-level simulations. The students will gain considerable hands-on experience in analog circuit design and the Cadence environment.

Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

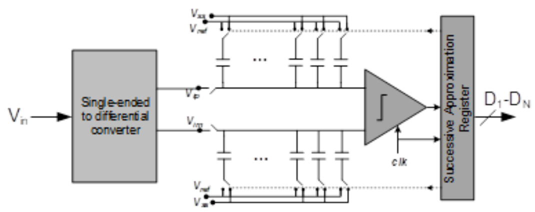
Project Breakdown:
• 30% Literature review
• 60% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A4

A Non-binary Search Successive Approximation Analog-to-Digital Converter for Biological Recording Systems

Successive approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in low-power moderate-resolution and moderate-speed applications such as implantable biomedical devices due to their minimal active analog circuit requirements and low power consumption. The conventional structure of a SA-ADC consists of a sample-and-hold (S/H) circuit, a comparator, a digital successive approximation register (SAR), and a digital-to-analog converter (DAC). Using a binary/non-binary search algorithm, the DAC output voltage, which is the analog voltage corresponding to the output digital code, successively approximates the sampled input voltage.



The aim of this project is to design a non-binary and power-efficient SA-ADC for biomedical and life science applications. The student will first study the concept of successive approximation ADCs, then will do a literature review. The main task of the project is to design a highly-linear low-power SA-ADC and verify its performance by pre-layout and post-layout simulations. The student will gain considerable hands-on experience in analog and mixed-signal circuit design and the Cadence environment.

Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

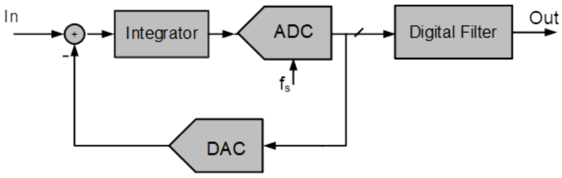
Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A5

A High-Resolution Delta-Sigma ADC for Sensor-Interface Applications

Delta-sigma ADC is one of the most popular ADC architectures for high-resolution and low-to-medium speed applications like sensors and instrumentation. A delta-sigma ADC, which utilizes oversampling and noise shaping techniques, consists of an integrator, a comparator, a digital-to-analog converter (DAC), and a digital decimation filter.



The project aims to design a high-resolution, low-power, first/second-order delta-sigma ADC for life science applications. The work will begin with a comprehensive study of delta-sigma converters and a detailed literature review. The main task of the project is to design a high-resolution delta-sigma ADC and verify its performance by transistor-level pre-layout and post-layout simulations in a CMOS technology. The student will gain considerable hands-on experience in analog and mixed-signal circuit design and the Cadence environment.

Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

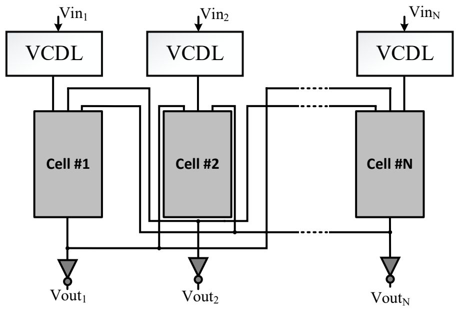
Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

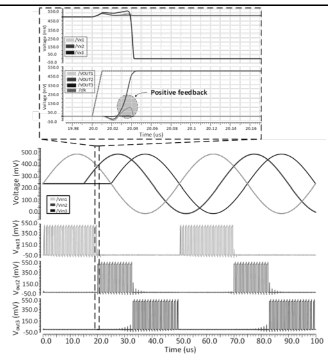
Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A6

A Low-Power Digital Winner-Take-All (WTA) Circuit

Winner-take-all (WTA) circuits a voltage-mode (current-mode) WTA circuit determines the largest voltage (current) signal among multiple inputs are widely used parallel signal processing, such as artificial neural networks, fuzzy systems, image processing, sensor fusion, and flash memories. In WTA circuits, all cells driven by the input signals compete simultaneously to set the voltage of a common node, and consequently the output is determined by the largest (i.e., winner) input signal. In digital structures, depending on the values of the input signals, only the output signal corresponding to the winner input goes to the logic level *High*, while the other outputs related to the loser cells remain *Low*.





In this project, the student will first study the concept of WTA circuits and do a literature review. The main task of the project is to design a low-power digital WTA circuit and verify its performance by transistor-level simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment.

Prerequisites: Acquaintance with circuit design in Cadence along with layout design.

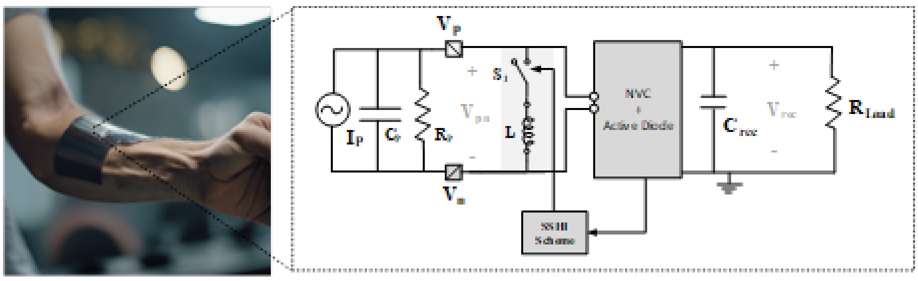
Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A7

A High-Effectiveness Piezoelectric Energy Harvesting Interface Circuit

Piezoelectric Energy Harvesters (PEHs) are widely used in wireless sensor nodes to lower the cost of battery replacement. In several applications, such as road EH systems, human motion Energy Harvesting (EH) systems, and wind EH systems, the PEH encounters varying levels of vibration intensity, and consequently the energy efficiency of the conventional energy harvesting interface circuits considerably reduce.



In this project, the student will first study the concept of energy harvesting interface circuits and do a literature review. The main task of the project is to design a high-effectiveness piezoelectric interface circuit and verify its performance by transistor-level simulations. The student will gain considerable hands-on experience in analog circuit design with emphasize on energy-harvesting systems and the Cadence environment.

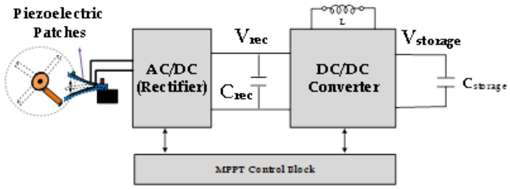
Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

<table>
<tr><td></td><td>Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid</td></tr>
<tr><td>A8</td><td>

A Board-Level Energy Harvesting Interface Circuits

In piezoelectric energy harvesting systems, it is necessary to match the input impedance of the interface circuit with the output impedance of the PEH using the Maximum Power Point Tracking (MPPT) technique to extract the power effectively.



In this project, we design a board-level energy harvesting interface circuit to extract maximum power from a piezoelectric harvester. The main task of the project is to design and implement a high-performance piezoelectric energy harvesting circuit and verify its performance by measurement results. The student will gain considerable experience in energy harvesting interface circuit design and measurement techniques.

Prerequisites: Acquaintance with analog circuit design.

Project Breakdown:
• 15% Literature review
• 75% Circuit design and measurement
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

</td></tr>
</table>

Digital circuits and modeling

D1	**Design and implementation of a digital reservoir computing system** Reservoir computing is a neuromorphic model that supports modeling of some cortical areas. In a simple model, nonlinear units (neurons) are organized in a sparsely recursively connected topology forming a reservoir to which a single input is provided. Several units deliver a single output to a single output unit. Only the connection strengths to the output neurons are modified by a learning algorithm, such as the FORCE learning algorithm. As a result, a reservoir has the capacity of synthesizing nonlinear functions, within a certain range of complexity. These signals can be used to the purpose of controlling biological or engineered systems. A digital system dedicated to efficient computation of the reservoir computing model is developed in this project. A study of the appropriate topology and architecture are carried out, and a processor is developed. A prototype is developed on an FPGA. Project breakdown: Literature survey: 10% Algorithm modeling (C/Matlab/Python language): 20% VHDL, FPGA synthesis: 70% Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
D2	**Patient-specific implantable detection of seizure** A modern therapy of pharmaco-resistant epilepsy consists of delivering electrical stimulation to deep-brain targets. Closed-loop stimulation involves cortical recording and detection of a seizure prior to delivering stimulation. Many algorithms have been developed showing various success rates, e.g., depending on the patient, its condition and the evolution of the disease. Consequently, the features that are used to detect the onset of a seizure vary from patient to patient and also along the lifetime of a patient. Based on a selection method developed in a completed MSc diploma project, we want to develop a processor that implements various feature extractors and classifiers, and allows to reliably adapt the global algorithm to a patient's specific condition. In a first part, the method must be adapted to hardware integration. Next, a processing unit architecture will be developed on FPGA that encompasses several feature extractor accelerators. Finally, a test methodology must be developed. Project breakdown: Literature survey: 10% Algorithm modeling (Matlab): 30% VHDL, FPGA synthesis: 70% Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
D3	

Bio-electronic interfaces and biomedical applications

<table>
<tr>
<td>B1</td>
<td>

A Board-Level Switched-Capacitor Stimulation Circuit

The aim of this project is to design a board-level switched-capacitor stimulation circuit. The main task of the project is to design and implement an energy-efficient switched-capacitor stimulation circuit using at the board level and verify its performance by measurement results. The student will gain considerable experience in board-level circuit design and measurement techniques.

Prerequisites: Acquaintance with analog circuit design and microcontrollers.

Project Breakdown:
• 15% Literature review
• 75% Circuit design and measurement
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

</td>
</tr>
<tr>
<td>B2</td>
<td>

A Multi-Phase High-Frequency Switched-Capacitor Neuro-Stimulation Circuit

Implantable stimulators are widely used to treat or improve neurological diseases such as Parkinson’s disease, epilepsy, and dystonia. In battery-powered implantable devices, it is necessary to reduce power consumption and minimize the device size along with providing charge balancing safety. Switched-capacitor stimulation systems, which employ a capacitor to deliver a specific amount of charge into the nerve tissue, takes the advantage of the high efficiency of voltage-mode stimulation (VMS) and the safety of current-mode stimulation (CMS). However, this method demands large off-chip capacitors for sufficient charge delivery, limiting its applications.

The aim of this project is to design an implantable energy-efficient switched-capacitor stimulation circuit. The student will first study the concept of the switched-capacitor stimulators, then will do a literature review. The main task of the project is to design an energy-efficient switched-capacitor stimulation circuit at the transistor level and verify its performance by simulations. The student will gain considerable hands-on experience in transistor-level circuit design and the Cadence environment.

Prerequisites: Acquaintance with circuit design in Cadence along with layout design.

Project Breakdown:
• 25% Literature review
• 65% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

</td>
</tr>
</table>

B3	**Wireless Power Transfer for Ventricular Assist Devices (VADs) and Total Artificial Heart Systems (TAHs)** Project Description Implantable cardiac assist devices, such as ventricular assist devices (VADs) and total artificial heart systems (TAHs), require a reliable supply of electrical power while operating inside the human body. Wireless power transfer (WPT) can provide a solution by transmitting energy from an external transmitter to an implanted receiver through an inductive link. In this project, the student will first study the principles of inductive WPT for implantable medical devices (IMDs) and perform a literature review. The main task of the project is to design and optimize an inductive wireless power transfer link for an implanted cardiac assist device. The student will investigate the influence of coil geometry, operating frequency, coupling distance, coil misalignment, resonant compensation and load conditions on the power transfer performance. The proposed system will be investigated through electromagnetic simulations and equivalent-circuit analysis of the inductive link, focusing on the transmitter and receiver coils, mutual coupling, and resonant compensation networks. A prototype system may subsequently be fabricated and experimentally characterized to validate the simulation results. The project will provide experience in electromagnetic simulation, resonant inductive coupling, wireless power transfer system design, resonant compensation networks and experimental measurements. Project Breakdown: • 20% Literature review and system requirement • 50% Electromagnetic and circuit-level design and optimization • 20% System performance analysis and optimization • 10% Reporting results Prerequisites Basic knowledge of electromagnetic fields, electrical circuits and resonant systems. Experience with electromagnetic simulation tools (e.g., CST, HFSS, etc.) is advantageous but not mandatory Contact person: Junlong Liu (junlong.liu@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
B4	**Wireless Power Transfer for Implantable Pacemakers at 2 GHz** Project Description Implantable pacemakers and other miniature biomedical devices require a reliable and efficient supply of electrical power while operating inside the human body. Wireless power transfer (WPT) at microwave frequencies offers a potential solution for delivering energy to deeply implanted devices while enabling compact implantable receivers. In this project, the student will first study the principles of microwave WPT for implantable biomedical applications and perform a literature review. The main task of the project is to design and optimize a wireless power transfer link for an implantable pacemaker operating at approximately 2 GHz. The student will investigate the design of compact transmitting and receiving antennas, the influence of the propagation environment and implantation depth, and the effect of antenna alignment and positioning on the received power. The proposed system will be investigated using full-wave electromagnetic simulations and RF system-level analysis. The project will focus on the design and optimization of the microwave power-transfer link, including the transmitting and receiving antennas (coils) and their electromagnetic coupling. The system performance will be evaluated in terms of received power, power-transfer efficiency, operating distance, robustness to misalignment and electromagnetic exposure constraints. A prototype system may subsequently be fabricated and experimentally characterized, depending on the progress and scope of the project. The project will provide experience in microwave electromagnetic simulation, antenna (coil) design, RF wireless power transfer, electromagnetic coupling and system-level performance evaluation. Project Breakdown: • 20% Literature review and system requirement • 50% 50% Electromagnetic design and optimization of the microwave wireless power-transfer link

	• 20% System performance analysis and optimization • 10% Reporting results Prerequisites Basic knowledge of electromagnetics, RF and microwave engineering, and electrical circuits. Experience with full-wave electromagnetic simulation tools and microwave system design is advantageous but not mandatory Contact person: Junlong Liu (junlong.liu@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
B5	**Design of a Microwave Class-E Power Amplifier with Microstrip-Line-Based RF Networks for Wireless Power Transfer Applications** Project Description Efficient power amplification is an important component of microwave wireless power transfer (WPT) systems, as the transmitter must generate a high-frequency excitation signal with sufficient output power while maintaining high power-conversion efficiency. Class-E power amplifiers (PA) are particularly attractive for WPT applications because of their high theoretical efficiency and suitability for resonant operation. In this project, the student will first study the principles of Class-E PA and their applications in microwave WPT systems and perform a literature review. The main task of the project is to design and optimize a microwave Class-E PA operating at a selected frequency, for example around 2 GHz. The amplifier may be developed for wireless powering of miniature implantable biomedical devices, such as pacemakers. The student will investigate the influence of the operating frequency, load network, switching conditions, device parameters, matching network and input power on the amplifier performance. The proposed amplifier will be designed and evaluated using circuit-level simulations, with particular emphasis on the design of the RF matching and output networks using microstrip transmission lines. The performance will be evaluated in terms of output power, power-conversion efficiency, switching behavior, harmonic content and robustness to variations in the load and operating conditions. Depending on the progress and scope of the project, the final design may subsequently be implemented using a printed-circuit-board microstrip-line structure and experimentally characterized. The project will provide experience in microwave power amplifier design, Class-E switching operation, RF matching networks, microstrip transmission-line design, circuit simulation and performance evaluation for wireless power transfer applications. Project Breakdown: • 20% Literature review and system requirement • 60% Microwave Class-E power amplifier design and circuit-level optimization • 10% Performance analysis and optimization • 10% Reporting results Prerequisites Basic knowledge of electrical circuits, electronics and RF/microwave engineering. Experience with circuit simulation tools, microwave power amplifier design or microstrip transmission-line design is advantageous but not mandatory. Prerequisites Basic knowledge of electromagnetic fields, electrical circuits and resonant systems. Experience with electromagnetic simulation tools (e.g., CST, HFSS, etc.) is advantageous but not mandatory Contact person: Junlong Liu (junlong.liu@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid

Fabrication technologies

N1	(void)

(no project at this moment)

Industrial projects / External projects (MSc diploma/Internships)

IE1

Self-Supervised fine-tuning of DNN in Edge AI processor

Project in collaboration with IMEC Holst Center, Neuromorphic Group.
The expected length of the project dictates that the MSc project and internship should be devoted to the project.

Intake form student assignments

Please complete this form to have your project posted on our website. If you have questions concerning the use of this form, please contact Recruitment

General information	
Daily Supervisor imec-NL	**Manolis Sifalakis**
Second supervisor imec-nl *(optional)*	**Federico Corradi, Amirreza Yousefzadeh**
Department *(pick one)*	IoT
Team	**NLICDESIGN**
Interviewers for this project *(at least Project Lead/Hiring manager and a team member)*	M.S., F.C., A.Y., M.K. (R&D Manager)

Assignment	
Title	**Self-Supervised fine-tuning of DNN in Edge AI processor**
Small introduction project *This text will be visible on the homepage of the thesis opportunities*	We are searching for optimized hardware efficient algorithms for self-supervised fine-tuning of deep neural networks in our neuromorphic processor for optimized adaptivity in edge applications.
Duration assignment *(note: BSc projects are max 6 months)*	☐ 9 to 12 months ☐

Student profile	
Level of education	☐ M.Sc.
Required program *(choose programs)*	☐ Electrical/Computer Engineering ☐ Computer Science

Project description (a clear description of the project)
[To be considered for this position: The European candidates must be enrolled in a Master program. Non-European master students who are enrolled in a Dutch university are also welcomed to apply] In the neuromorphic group of Imec (Holst-Centre), we design neuromorphic processors and near/in sensor solutions to implement Edge AI applications with (online) learning and adaptation mechanisms. Since continuous learning and adaptability is one of the differentiators of neuromorphic technology, this project will aim at an exploration of possible learning/adaptation strategies in applications domains in which online learning is required, such as predicting sensor (audio/video/radar) signals and denoising images (real-time medical imaging), anomaly detection, biomedical signal processing, etc. A starting point for example can be a vanilla randomly initialized network or an already generic pre-trained neural network that gets further refined [1] for more customised inference. The core of the student project is in the research of effective and efficient online learning/fine-tuning methods, and the objective will be that the algorithm(s) of choice will be suited to run on (our) neuromorphic processors. This fine-tuning should result in competitive accuracy for the specific task or enable more efficient inference by increasing spatio-temporal sparsity during inference. A particular niche area of interest lies in **exploring self-supervised learning algorithms** [2].

public

One of our target neuromorphic processors contains several RISC-V cores connected through an interconnected network. A key feature of our hardware is its event-driven operations (a process in a RISC core only triggers an event). Additionally, the different cores work independently from each other. These two constraints impose the implementation of an **event-driven, distributed, and local learning mechanism**. Another neuromorphic architecture is based on digital ASIC technology with in-processor distributed memory featuring a combination of multi-layer perceptrons and liquid state-machines with basic IF/LIF neurons interacting asynchronously with each other and across layer. Under sparse operation the tiny microprocessor consumes only pJ of energy [3], which makes it ideal as a sensor payload. The goal would be to equip it with a fine-tuning capability that would allow it to self-customise in-situ and perform well across deployments.

The project duration is 9 to 12 months (optionally combining internship and M.SC. thesis). The results of the project may be published in high-impact journals and may as well be patented.

We are welcoming collaboration with laboratories that can help us bridge the gap among neuromorphic technologies and applications in biomedical signal processing, neuromorphic and machine learning integration methods, circuits and systems non-conventional computing and learning architectures.

We seek motivated candidates with a relevant background in one or more of the fields of neuromorphic computing/engineering, optimization for neural network learning, statistical inference and probabilistic learning models. The candidate must have good programming skills in Python (with desired experience TensorFlow and/or PyTorch) and embedded C++ programming (for RISC-V programming). The interested applicants should submit their CV, the academic transcripts (including the scores and the courses).

References:

[1] Deep Learning using Transfer Learning (https://towardsdatascience.com/deep-learning-using-transfer-learning-python-code-for-resnet50-8acdfb3a2d38)
[2] Self-supervised learning: could machines learn like humans? (https://youtu.be/7I0Qt7GALVk)
[3] µBrain: An Event-Driven and Fully Synthesizable Architecture for Spiking Neural Networks (https://www.frontiersin.org/articles/10.3389/fnins.2021.664208/full)

Tasks (specific)

- Literature review on neuromorphic architecture and relevant learning algorithms
- Identifying 1-2 suitable algorithms and applications for (self/partially-)supervised learning/fine-tuning (potentially extending existing work in the topic)
- Implementation / validation of the selected learning algorithm in python
- Application of the algorithm on the neuromorphic platform and testing
- Thesis writing and documentation in Imec Holst-Centre

Required skills *(the lines that are already added are mandatory)*

- Very good/excellent in python (desired experience in TensorFlow/PyTorch) and embedded C (++) programming
- Knowledge of (Deep) Neural Networks training algorithms internals (some experience in optimization, statistical inference and probabilistic learning, or statistical signal processing, is a plus)
- A structured way of reporting, both orally and written
- Motivated student eager to work independently and expand knowledge in the field
- Good written and verbal English skills

public

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or above IMEC supervisors
EPFL responsible supervisor (IS-Academia registration): Alexandre Schmid

IE2	**Event-based (Neuromorphic) radar signal encodings**

Event-based (Neuromorphic) radar signal encodings

Project in collaboration with IMEC Holst Center, Neuromorphic Group.
The expected length of the project dictates that the MSc project and internship should be devoted to the project.

General information	
Daily Supervisor IMEC-NL	**Manolis Sifalakis**
Second supervisor IMEC-NL *(optional)*	**Federico Corradi, Amirreza Yousefzadeh**
Department *(pick one)*	IoT
Team	**NLICDESIGN**
Interviewers for this project *(at least Project Lead/Hiring manager and a team member)*	M.S., F.C., A.Y., M.K. (R&D Manager)

Assignment	
Title	**Event-based (Neuromorphic) radar signal encodings**
Small introduction project *This text will be visible on the homepage of the thesis opportunities*	At Imec's Holst-center lab in Eindhoven we are developing a novel neuromorphic radar sensor backend called event-radar that targets always-on low-power sensing, sparse data streaming, and on-sensor processing. In-line with this work we seek for a motivated student to undertake a project, which will focus on exploring and developing temporally and spatially sparse (event based) encodings of radar signals for short-range radar application tasks (gesture recognition, vital sign detection, room activity classification). The objective will be that these signals can be generated and used for inference right at the sensor (low-power budget and real-time application inference).
Duration assignment *(note: BSc projects are max 6 months)*	☐ 9 to 12 months ☐

Student profile	
Level of education	☐ M.Sc.
Required program *(choose programs)*	☐ Electrical/Computer Engineering ☐ Computer Science ☐ Neuromorphic engineering

Project description (a clear description of the project)
[To be considered for this position: The European candidates must be enrolled in a Master program. Non-European master students who are enrolled in a Dutch university are also welcomed to apply] Typically, most sensors today (camera/microphone/radar/etc.) generate a lot of data that need to be communicated for processing/inference by a model. This allows the sensor to do little processing work at the expense of the bandwidth that is needed to communicate the data to the downstream processing pipeline.

public

By contrast neuromorphic sensors (dynamic vision sensor [1], cochlea audio sensor [2], e-skin sensor [3]), inspired by sensory processing principles in the brain, consume significantly less power, and generate sparser temporal signals. A big advantage of this paradigm is that it leaves resources for application-related processing right at the sensor as well. Towards a similar objective in the neuromorphic group of IMEC (Holst-Centre lab, Netherlands), we have been developing an analogous neuromorphic radar-sensor backend, for indoor or short distance sensing applications (think of gesturing commands, human activity, vital signs, etc in an office space, or automotive application).

The goal of this project will be to explore various temporal encodings and sparse distributed representations of the radar signals, their suitability for embedded low-power processing and their efficacy in machine learning related application tasks.

For example, a baseline exploration point can be a **differential encoding** (delta or sigma-delta modulator), and one may move on to introduce reverberating dynamics with neural networks such as **echo-state networks** (liquid state machines) that can be "nudged" to resonate according to the radar front-end detections, or move to trainable **sparse signature representations** [4]of the activity taking place in front of the sensor.

The results of this exploration will be compared with more common-place traditional radar DSP pipelines (e.g., FFT based) and evaluated in various application tasks such as those listed above.

Project duration is set to 9 or 12months (e.g., internship and MSc project) and depending on outcomes, there will be opportunity to patent or publish the results in high-visibility conference or journal in the field.

While the work is primarily algorithmic, depending on competence and interest, the student may also have the opportunity to work directly with the radar sensor hardware prototype and novel neuromorphic accelerators, for collecting data and running experiments.

Candidates are expected to be highly motivated, with relevant background in one or more of the following fields: sensor signal processing, neuromorphic computing/engineering, optimization and learning in neural networks, statistical pattern recognition / probabilistic learning models. The candidate must have good programming skills in Python and reasonable exposure to C/C++ (there will not be opportunity to learn elementary programming during the project). Interested applicants are welcome to submit their CV, and academic transcripts (courses taught, and scores or level attained wherever applicable).

References:
[1] Galego et al. (2020). Event-based vision: a Survey. IEEE transactions on Pattern Analysis and Machine Intelligence.
[2] S.Liu et al. (2014). Asynchronous Binaural Spatial Audition Sensor With 2x64x4 Channel Output. IEEE Transactions on Biomedical Circuits and Systems.
[3] F.Bergner et al. (2020). Design and Realization of a Resistive Efficient Large-Area Event-Driven E-Skin. MDPI Sensors.
[4] W. Brendel et al (2020). Learning representations spike-by-spike. PLOS Computational Biology,

Tasks (specific)

- Literature review on neuromorphic sensing and processing
- Plan exploration for a small set of designed encodings/representations (define criteria of interest and application of interest)
- Implementation of resp. representation algorithms

- Performance testing and evaluation, comparison with contemporary radar DSP pipelines
- Thesis writing and documentation in IMEC Holst-Centre

Required skills *(the lines that are already added are mandatory)*

• Very good/excellent programming in python and at least intermediate programming in C/C++
• Good background in one or more of:
    ○ Sensor digital signal processing (radar DSP preferable)
    ○ Neuromorphic computing/engineering
    ○ Optimization for learning in Neural networks
    ○ Statistical pattern recognition
• A structured way of reporting, both orally and written
• Motivated student eager to work independently and expand knowledge in the field
• Good written and verbal English skills

•

public

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or above IMEC supervisors
EPFL responsible supervisor (IS-Academia registration): Alexandre Schmid

<table>
<tr>
<td>IE3</td>
<td>

Internship at Kandou Bus SA

- Signal processing and modeling: the students will help model complex analog circuits using signal processing techniques. Knowledge of analog circuits is a plus, but we will be able to teach them the required knowledge if they have a firm knowledge of signal processing. Programming skills in Python, C, or C++ is a big plus.
- Digital circuit design: the students will help with the design of control circuitry for very high speed serial links. Knowledge of standard tools from Cadence or Synopsys is a must.
- Analog circuit design: the students will help the Advanced R&D lab members design very high speed and very low power serial links. Knowledge of standard tools from Cadence or Synopsys is a must.

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or Kandou Bus SA supervisors, Aminn Shokrallahi, Armin Tajalli, Chloe Joubert (amin@kandou.com, armin.tajalli@kandou.com, joubert@kandou.com)

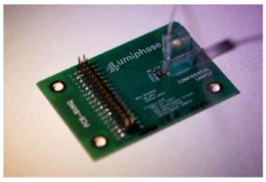
</td>
</tr>
<tr>
<td>IE4</td>
<td>

Internship at Lumiphase AG, Firmware and electronics development

Project available as MSc diploma or internship

Project 4: Firmware and electronics development

The goal of this project is to develop the electronics of different setups used to analyze the performance of Pockels-enhanced silicon photonics circuits.



The work during the internship is technology-driven and includes:

- Firmware development on a microcontroller, and development of an API to interact with it from a computer;
- Designing, testing and improving PCBs, used for example to interface the microcontroller with the rest of the setup and with our devices;
- Implementing and characterizing control methods to stabilize our device at the desired operating point;
- Working on a customized electrical/optical setup, including the design and assembly of hardware components;
- The duration of the project work will be determined in accordance with the regulations of your university but needs to be at least 6 months.

The ideal candidate should bring:

- Strong interest in simulation and experimental work with integrated photonics and nano/microelectronics;
- Good programming knowledge, ideally in C.
- Small experience with microcontrollers (lecture, lab courses, ...)

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or Lumiphase AG supervisors Caroline Rossier (caroline.rossier@lumiphase.com)

</td>
</tr>
</table>

Application development (software development)

SW1	**Peripherals for an FPGA development environment** Diverse analog and digital interfaces are classical peripherals used in modern consumer electronics. Physical devices are used in all practical implementations. The latter may consist of sensors or actuators that obey certain protocols or signal timings. Increasingly, such interfaces are offered in a virtual implementation, that is as a dynamic image on a touchscreen. This project aims at creating such an environment to the terasic DE10-Lite on-board peripherals such as an accelerometer, VGA display connectors, UART interface and integrate the new system into the logisim-evolution design flow. As a result, the environment should present the new peripherals both available in logisim-evolution. For example, based on the achievements in past projets, we want to create a graphical environment on PC based on Python3 and Qt or TK that displays data collected at the FPGA sensors and transmitted through UART. Project breakdown 20% documentation study, procedure development 50% software development (VHDL) 30% logisim-evolution inclusion Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
SW2	**Peripherals for a AVR STK-300 environment** The AVR-based STK-300 development system is used in several courses in EPFL supporting microcontrollers classes. Along to existing peripheral boards, additional are being developed. Software libraries must be developed at assembly level to support e.g., Duinopeak 1,8" Color TFT (ST7735R controller), FT232RL (FTDI RS232 to USB). For example, based on the achievements in past projets, we want to create a graphical environment on PC based on Python3 and Qt or TK that displays data collected at the MCU sensors and transmitted through UART. Project breakdown: • Literature review (10%) • Assembly development (80%) • Documentation (10%) Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid