MS Diploma and Semester Projects offered at the Biomedical and Neuromorphic Microelectronic Systems research group during the spring/summer of 2023

Students are asked to contact the project responsible to register. The majority of the projects are proposed as MS Diploma and Semester or BS semester, and the amount of work will be adapted. Also, some projects can be carried out in groups of two students.

Projects are proposed in six categories in the following pages.

- Analog and mixed-signal circuits
- Digital circuits and modeling
- Bio-electronic interfaces and biomedical applications
- Fabrication technologies
- Industrial projects / external projects (for MSc diploma)
- Application development (software development)

Please contact us if you have your own idea, wish to propose a collaborative project topics e.g. in industry, or wish to start an external collaboration, e.g., internship

List of projects

Analog and mixed-signal circuits and modeling

A1	**Reservoir computing for robust generation of complex temporal patterns** Reservoir computing is a neuromorphic model that supports modeling of some cortical areas. In a simple model, nonlinear units (neurons) are organized in a sparsely recursively connected topology forming a reservoir to which a single input is provided. Several units deliver a single output to a single output unit. Only the connection strengths to the output neurons are modified by a learning algorithm, such as the FORCE learning algorithm. As a result, a reservoir has the capacity of synthesizing nonlinear functions, within a certain range of complexity. These signals can be used to the purpose of controlling biological or engineered systems. The robustness of the entire system to faults (single or multiple event faults), as well as variations is studied in this project. A model of reservoir is developed in C language. Fault models are introduced. A strategy to counter the effect of faults is developed. An analysis study of the results using various waveforms (applications) is presented. Project breakdown: Literature survey: 20% Software modeling and simulations(C language): 80% Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
A2	**CMOS DC-DC Converter for Biomedical Implants** Wireless power and data communication systems in implantable medical devices (IMDs) are developed to control and report acquired biological data from an implanted device to an external stage in several medical applications. Inductive power transfer (IPT) is one of the most commonly used techniques due to its robustness, simplicity, safety, and capability for simultaneous and bidirectional data and power transmission. The essential purpose of power transmission to IMDs is to provide the energy needed to send and receive data, including commands or recorded biological data from or to the body or brain for biomedical applications. However, some blocks, such as the stimulation unit, require a higher voltage level than the usual voltage level (1.8 V). In order to enable the chip to work correctly, a CMOS DC-DC voltage converter should be designed. This project aims to CMOS DC-DC converter for IMDs. The student will first study the concept of inductive power transmission and DC-DC converter, then will do a literature review. The main task of the project is to design a system with the maximum power transfer efficiency through inductive powering at the transistor level and verify its performance by simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment. Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design. Recommended Skills: LaTeX, Origin Pro Project for: 1 M.Sc. diploma student , 2 M.Sc. semester project students. Project Breakdown: • 10% Literature review • 80% Circuit design and verification • 10% Reporting results Supervisors: Mohammad Javad Karimi, mohammad.karimi@epfl.ch Responsible supervisor (IS-Academia registration): Alexandre Schmid

A3	**A Capacitor-less Low-DropOut (LDO) Voltage Regulator for Biomedical Implants** Wireless power and data communication systems in implantable medical devices (IMDs) are developed to control and report acquired biological data from an implanted device to an external stage in several medical applications. Inductive power transfer (IPT) is one of the most commonly used techniques due to its robustness, simplicity, safety, and capability for simultaneous and bidirectional data and power transmission. The essential purpose of power transmission to IMDs is to provide the energy needed to send and receive data, including commands or recorded biological data from or to the body or brain for biomedical applications. The unregulated DC voltage output of the rectifier should be converted to a stable voltage supply by a voltage regulator because the performances of the implant's electronics are optimized for a specific DC supply voltage. Moreover, the effects of misalignment between coils and small ripples of the rectifier output voltage are filtered by voltage regulators. Low drop out (LDO) regulators are used in the literature frequently. This project aims to design a capacitor-less voltage regulator. The student will first study the concept of inductive power transmission and LDOs and do a literature review. The main task of the project is to design LDO to maximize efficiency and minimize power consumption through inductive powering at the transistor level and verify its performance by simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment. Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design. Recommended Skills: LaTeX, Origin Pro Project for: 1 M.Sc. diploma student , 2 M.Sc. semester project students. Project Breakdown: • 10% Literature review • 80% Circuit design and verification • 10% Reporting results Supervisors: Mohammad Javad Karimi, mohammad.karimi@epfl.ch Responsible supervisor (IS-Academia registration): Alexandre Schmid
A4	**Wireless Power Transmission For Multiple Biomedical Implants Through Inductive Links** Wireless power and data communication systems in implantable medical devices (IMDs) are developed to control and report acquired biological data from an implanted device to an external stage in several medical applications. Inductive power transfer (IPT) is one of the most commonly used techniques due to its robustness, simplicity, safety, and capability for simultaneous and bidirectional data and power transmission. The essential purpose of power transmission to IMDs is to provide the energy needed to send and receive data, including commands or recorded biological data from or to the body or brain for biomedical applications. In order to create the conditions for data acquisition or stimulation, power should be remotely transferred to multiple patches distributed over the body or brain. To this end, cross-talk between devices and implants should be studied. This project aims to simulate inductive power transfer by using ANSYS HFSS/MAXWELL tools to study the behavior of wireless power transmission, coupling coefficient, and body health monitoring to make sure safe and sufficient power will be delivered to the implants. Power transfer efficiency (PTE) also should be studied and analyzed. Prerequisites: Acquaintance with ANSYS HFSS/MAXWELL and circuit theory. Recommended Skills: LaTeX, Origin Pro, Cadence Virtuoso Project for: 1 M.Sc. diploma student , 2 M.Sc. semester project students. Project Breakdown: • 10% Literature review • 80% System design and simulation • 10% Reporting results

	Supervisors: Mohammad Javad Karimi, mohammad.karimi@epfl.ch Responsible supervisor (IS-Academia registration): Alexandre Schmid
A5	**A Power Amplifier for Biomedical Implants** Wireless power and data communication systems in implantable medical devices (IMDs) are developed to control and report acquired biological data from an implanted device to an external stage in several medical applications. Inductive power transfer (IPT) is one of the most commonly used techniques due to its robustness, simplicity, safety, and capability for simultaneous and bidirectional data and power transmission. The essential purpose of power transmission to IMDs is to provide the energy needed to send and receive data, including commands or recorded biological data from or to the body or brain for biomedical applications. To this end, the required power should be sent from the external unit through the sinusoidal signal to the inductive link and will be received and rectified in the implants. The aim of this project is to design a power amplifier (PA) to send power as sine waves with the inputs of Clock and Data. It can be designed in CMOS technology or with discrete components in the PCB. The student will first study the concept of inductive power transmission and PAs and do a literature review. The main task of the project is to design PA to maximize efficiency and minimize power consumption through inductive powering at the transistor level and verify its performance by simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment. Prerequisites: Acquaintance with analog circuit design in Cadence along with PCB design. Recommended Skills: LaTeX, Origin Pro, Altium Project for: 1 M.Sc. semester project student. Project Breakdown: • 10% Literature review • 80% Circuit design and verification • 10% Reporting results Supervisors: Mohammad Javad Karimi, mohammad.karimi@epfl.ch Responsible supervisor (IS-Academia registration): Alexandre Schmid
A6	**A PLL and Clock Generator for Biomedical Implants** Wireless power and data communication systems in implantable medical devices (IMDs) are developed to control and report acquired biological data from an implanted device to an external stage in several medical applications. Inductive power transfer (IPT) is one of the most commonly used techniques due to its robustness, simplicity, safety, and capability for simultaneous and bidirectional data and power transmission. The essential purpose of power transmission to IMDs is to provide the energy needed to send and receive data, including commands or recorded biological data from or to the body or brain for biomedical applications. To this end, the required power should be sent from the external unit through a sinusoidal signal to the inductive link and will be received and rectified in the implants. This sine wave comes from a generated clock (e.g., 13.56 MHz). Also, a PLL will be used in the implant for data demodulation. The aim of this project is to design a clock generator (cross-coupled or ring oscillator) to generate the required clock and then design a PLL for the implant in CMOS technology. The student will first study the concept of inductive power transmission and clock generators and do a literature review. The main task of the project is to design a clock generator and PLL with minimum power consumption and minimum accuracy and verify its performance by simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment.

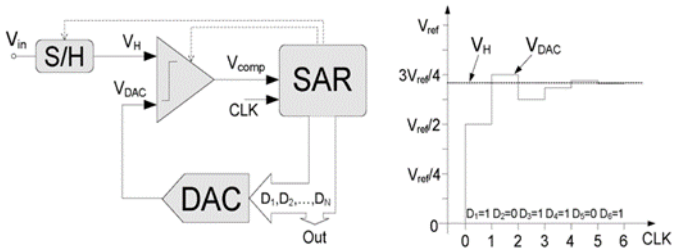
Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.
Recommended Skills: LaTeX, Origin Pro

Project for: 1 M.Sc. diploma student, 2 M.Sc. semester project students.

Project Breakdown:
• 10% Literature review
• 80% Circuit design and verification
• 10% Reporting results
Supervisors:
Mohammad Javad Karimi, mohammad.karimi@epfl.ch
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A7 **Successive Approximation Analog-to-Digital Converter for Biological and Biomedical Recording Systems**

Successive approximation analog-to-digital converters (SA-ADCs) have recently become very attractive in low-power moderate-resolution and moderate-speed applications such as implantable biomedical devices due to their minimal active analog circuit requirements and low power consumption. The conventional structure of an SA-ADC, consists of a sample-and-hold (S/H) circuit, a comparator, a digital successive approximation register (SAR), and a digital-to-analog converter (DAC). Using a binary search algorithm, the DAC output voltage successively approximates the sampled input voltage and in each clock cycle one bit of the digital output word is obtained.



The aim of this project is to design a power-efficient SA-ADC for low-power applications. The student will first study the concept of successive approximation ADCs, then will do a literature review. The main task of the project is to design a highly-linear low-power SA-ADC and verify its performance by transistor-level simulations. The student will gain considerable hands-on experience in analog and mixed-signal circuit design and the Cadence environment.

Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

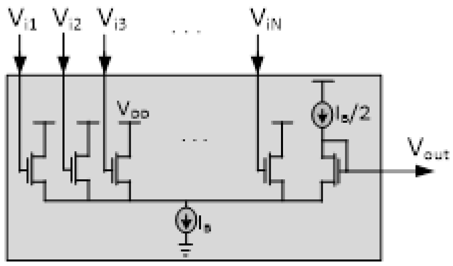
Project for: 1 M.Sc. diploma student, 2 M.Sc. semester project students.

Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A8 **A High-Precision and Low-Power Winner-Take-All (WTA) Circuit**

Winner-take-all (WTA) circuits which determine the maximum value among multiple inputs are widely used in parallel signal processing systems (e.g., in multichannel recording systems). The conventional structure of a WTA circuit typically employs N identical input cells driven by the voltage/current input signals and connected to a common low-impedance node. In this way, the input voltage/current signals compete to set the voltage at the common low-impedance node which is fed back to the input cells such that the output signal is determined by the largest input signal. Although the structure of these circuits is simple, however, both the speed and the accuracy of the circuit are degraded with increasing the number of inputs.



In this project, the student will first study the concept of WTA circuits and do a literature review. The main task of the project is to design a high-precision and low-power WTA circuit and verify its performance by transistor-level simulations. The student will gain considerable hands-on experience in analog and digital circuit design and the Cadence environment.

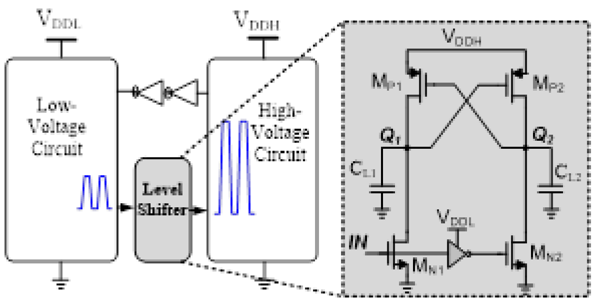
Prerequisites: Acquaintance with circuit design in Cadence along with layout design.
Project for: 1 M.Sc. diploma student, 2 M.Sc. semester project students.

Project Breakdown:
• 20% Literature review
• 70% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

A9 **An Energy-Efficient Wide-Range Voltage Level Shifter**

In merging embedded applications such as biomedical devices, lowering the power dissipation is necessary to have a lengthen battery life. One of the most effective ways to reduce the power consumption of the digital circuits is lowering the supply voltage. This method is especially effective if the value the supply voltage is chosen below the threshold level of CMOS devices (so-called sub-threshold design). However, reducing the supply voltage increases the delay of the circuits. Hence, employing a dual supply voltage technique, which the critical blocks are powered at a higher supply voltage (i.e., VDDH) whereas other noncritical parts operate at a lower supply voltage (i.e., VDDL) is advantageous from the power dissipation viewpoint. This allows to conveniently trade off performance versus power consumption of low and high supply voltages. Furthermore, even if the whole core of a chip could work in the sub-threshold domain, an above-threshold supply voltage would still be needed for the digi tal input/output (I/O) pad cells. In these systems, voltage level shifters are required to translate the logical levels of (0, VDDL) to (0, VDDH) with minimum power consumption and propagation delay.



The aim of this project is to design a CMOS voltage level shifter. The student will first study the concept of voltage level shifters, then will do a literature review. The main task of the project is to design a wide-rand and low power voltage level shifter at the transistor level and verify its performance by simulations. The student will gain considerable hands-on experience in transistor-level digital circuit design and the Cadence environment.

Prerequisites: Acquaintance with circuit design in Cadence along with layout design.

	Project for: 1 M.Sc. diploma student, 2 M.Sc. semester project students. Project Breakdown: • 30% Literature review • 60% Circuit design and verification • 10% Reporting results

Digital circuits and modeling

D1	**e-Health system based on a WBAN for epilepsy detection** Personalized medicine and e-Heath systems prescribe the development of wireless body area networks as a solution to continuous monitoring the health condition of patients. The general concept can be adapted to support diagnosis and also deliver treatment in the form of electrical stimulation. Patients suffering from some neurological disorders may benefit from such systems that would extend over the capabilities of current systems that operate individually (Parkinson's disease, epilepsy, sleep disorders). In this project, we use a wireless infrastructure developed in an earlier project and extend it with a set of sensors aiming at epilepsy seizure detection/prediction. The system architecture must be determined and developed including a terminal node (tablet/cell phone or PC). The central system gathers data from the sensors and executes seizure detection/prediction algorithms to trigger the delivery of therapy. Integrated wireless sensor nodes must be developed and deployed. The connections to our implantable epilepsy control hardware will be considered. Project breakdown: Literature review: (10%) Architecture and development of the terminal software: 45% Development of peripheral sensor nodes (HW/SW): 40% Algorithm developments (MATLAB or Python): 10% Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
D2	**FPGA implementation of a spectral domain biomedical signal processing and Machine learning classification for epileptic seizure detection** Epilepsy is a common neurological disorder and approximately 1% of world population suffer from some forms of epilepsy during their life span. Epilepsy is caused by abnormal and excessive activity of the brain neurons. EEG signals are used to monitor human's brain activity which are used by neurologists or detect the onset of a seizure by an automatic seizure detection system. Digital signal processing techniques are applied on EEG signals to extract beneficial features for accurate seizure detection. In this project, the raw EEG data will be converted from the time-domain to the frequency domain using short-term Fourier transform (STFT) or Fast Fourier transform (FFT) units. Subsequently, spectral features of the signal are extracted in various frequency bands and they are given to an SVM classifier to discriminate between seizure and non-seizure neural signals. The project consists of software and hardware implementations. Initially, the performance of the seizure detection system is evaluated by software simulation in MATLAB. Then, the algorithm will be implemented on a FPGA. Main fields of this project: Hardware design, FPGA implementation, VHDL programing, Digital signal processing. Project breakdown: • Literature review: 10% • Software implementation (MATLAB): 25% • VHDL implementation: 40% • FPGA test : 25% Contact person: Keyvan Farhang Razi (keyvan.farhangrazi@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid

D3	**Design and implementation of a digital reservoir computing system** Reservoir computing is a neuromorphic model that supports modeling of some cortical areas. In a simple model, nonlinear units (neurons) are organized in a sparsely recursively connected topology forming a reservoir to which a single input is provided. Several units deliver a single output to a single output unit. Only the connection strengths to the output neurons are modified by a learning algorithm, such as the FORCE learning algorithm. As a result, a reservoir has the capacity of synthesizing nonlinear functions, within a certain range of complexity. These signals can be used to the purpose of controlling biological or engineered systems. A digital system dedicated to efficient computation of the reservoir computing model is developed in this project. A study of the appropriate topology and architecture are carried out, and a processor is developed. A prototype is developed on an FPGA. Project breakdown: Literature survey: 20% Algorithm modeling (C language): 30% VHDL, FPGA synthesis: 50% Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
D4	**FPGA implementation of a time-frequency domain epileptic seizure detector using KNN classifier for biomedical implants** Epilepsy is a brain non-communicable disorder which affects more than 65 million people worldwide. Epilepsy is characterized by recurrent seizures which are the results of the uncoordinated electrical discharges generated mainly in cerebral cortex. Digital signal processing techniques, called feature extraction, are applied on iEEG signals to extract the characteristics of the brain signal which are more relevant to the seizure events. The extracted features are fed to a K-nearest neighbor (KNN) classifier to discriminate between seizure and normal states of a patient. This project involves feature extraction in time-frequency domain by decomposing the signal into various frequency bands related to the seizure activities using Discrete Wavelet Transform (DWT). Then, statistical features of DWT coefficients are extracted and feed a KNN classifier. The project consists software implementation of the seizure detection algorithm using MATLAB or Python and the hardware implementation on an Intel Altera FPGA. Main field of the project: VLSI design, Biomedical signal processing, Machine learning, FPGA implementation. Project breakdown: • Literature review: 10% • Software implementation (MATLAB or Python): 20% • VHDL implementation: 40% • Hardware test (FPGA): 30% Contact person: Keyvan Farhang Razi (keyvan.farhangrazi@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
D5	(void)
D6	(void)
D7	

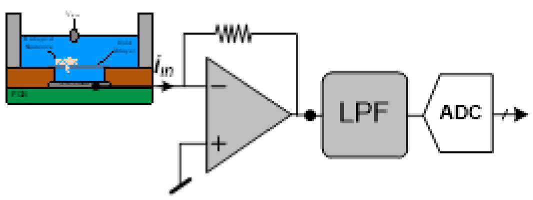
D8	
D9	
D10	

Bio-electronic interfaces and biomedical applications

B1

Low-Noise Font-End Circuit for Nanopore Sensing Systems

The nanopore recording systems, that can be used for the recognition of the size and composition of individual protein, DNA, RNA, and peptides, recently become very attractive due to their label free, ultralong reads, high throughput, low material requirement, and low cost. In these systems, an ionic current flows through the nanopore by applying a bias voltage across it. When a molecule passes through a nanopore, the electric resistance and therefore the current is disrupted in picoampere level. The molecule characteristics can be studied by recording the fluctuation of the current. The recording system consists of a low-noise transimpedance amplifier, a low-pass filter, and an analog-to-digital converter.



In this project, the student will first study the concept of low-noise transimpedance amplifier and low-pass filters and do a literature review. The main task of the project is to design a low-noise and highly-linear transimpedance amplifier followed by a low-pass filter circuit and verify their performance by transistor-level simulations. The student will gain considerable hands-on experience in analog circuit design and the Cadence environment.

Prerequisites: Acquaintance with analog circuit design in Cadence along with layout design.

Project for: 1 M.Sc. diploma student, 2 M.Sc. semester project students.

Project Breakdown:
• 40% Literature review
• 50% Circuit design and verification
• 10% Reporting results

Contact person: Mehdi Saberi (mehdi.saberi@epfl.ch)
Responsible supervisor (IS-Academia registration): Alexandre Schmid

B2

Board-level Femtoampere Current Recording Platform Design
(Project in collaboration with EPFL Cao Lab)

Nanopore technology is a novel method developed to address questions in life science and diagnosis at the single-molecule level. Molecules flowing through the nanopore deliver information related to their nature enabling application including DNA sequencing or data storage readout. A board-level system implementing the front-end readout electronics, as well as some microcontroller interfacing with an external PC has been developed. The prototype will be improved in a revised version and adapted to interfacing with a commercial microcontroller. Embedded microcontroller software will be developed to enable real-time recording of the nanopore extremely low-current output.

Qualifications we are looking for
Hands-on experience in high-speed PCB design and assembly, test and measurements.
Basic experience in the field of electronics design for data recording and communication based on microcontroller
Experience in microcontroller programming (C or C++). Proven knowledge of other logic devices such as DSPs and FPGA would be an advantage.
Experience with USB2.0 communication between microcontroller and PC would be an advantage.

Project breakdown:

	20% literature review and documentation 40% board-level developments (e.g., filters, voltage shifters) and full PCB development 40% embedded software for real-time recording and data transfer to an external PC Contact person: Chan Cao (chan.cao@epfl.ch), Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): TBD
B3	**Biomedical digital signal processing for real-time low-power epilepsy control system** Processing iEEG signals, which are recorded via multiple number of electrode channels in the brain, has already demonstrated promising results in detection of neural disorders such as Epilepsy, Alzheimer and Parkinson. Various signal processing techniques in time domain, frequency domain and wavelet domain will be studied to enable precise and rapid epileptic seizure detection. A critical issue in developing real-time seizure detection algorithms for implantable devices is the high computational complexity of the system which is imposed by extracting multiple features from several electrode channels. This project focuses on developing a method to limit the number of required electrode channels and the number of required features for accurate seizure detection. Main fields of the project: Biomedical signal processing, Machine learning classification, Feature ranking. Project breakdown: • Literature review: 10% • Feature selection algorithm (MATLAB or Python): 35% • Channel selection algorithm (MATLAB or Python): 35% • Testing the seizure detector on human iEEG (MATLAB or Python): 20% Contact person: Keyvan Farhang Razi (keyvan.farhangrazi@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid

Fabrication technologies

N1	(void)
N2	(void)
N3	(void)
N4	(void)
N5	(void)
N6	(void)

Industrial projects / External projects (MSc diploma/Internships)

IE1

Self-Supervised fine-tuning of DNN in Edge AI processor

Project in collaboration with IMEC Holst Center, Neuromorphic Group.
The expected length of the project dictates that the MSc project and internship should be devoted to the project.

Intake form student assignments

Please complete this form to have your project posted on our website. If you have questions concerning the use of this form, please contact Recruitment

General information	
Daily Supervisor imec-NL	**Manolis Sifalakis**
Second supervisor imec-nl *(optional)*	**Federico Corradi, Amirreza Yousefzadeh**
Department *(pick one)*	IoT
Team	**NLICDESIGN**
Interviewers for this project *(at least Project Lead/Hiring manager and a team member)*	M.S., F.C., A.Y., M.K. (R&D Manager)

Assignment	
Title	**Self-Supervised fine-tuning of DNN in Edge AI processor**
Small introduction project *This text will be visible on the homepage of the thesis opportunities*	We are searching for optimized hardware efficient algorithms for self-supervised fine-tuning of deep neural networks in our neuromorphic processor for optimized adaptivity in edge applications.
Duration assignment *(note: BSc projects are max 6 months)*	☐ 9 to 12 months ☐

Student profile	
Level of education	☐ M.Sc.
Required program *(choose programs)*	☐ Electrical/Computer Engineering ☐ Computer Science

Project description (a clear description of the project)
[To be considered for this position: The European candidates must be enrolled in a Master program. Non-European master students who are enrolled in a Dutch university are also welcomed to apply] In the neuromorphic group of Imec (Holst-Centre), we design neuromorphic processors and near/in sensor solutions to implement Edge AI applications with (online) learning and adaptation mechanisms. Since continuous learning and adaptability is one of the differentiators of neuromorphic technology, this project will aim at an exploration of possible learning/adaptation strategies in applications domains in which online learning is required, such as predicting sensor (audio/video/radar) signals and denoising images (real-time medical imaging), anomaly detection, biomedical signal processing, etc. A starting point for example can be a vanilla randomly initialized network or an already generic pre-trained neural network that gets further refined [1] for more customised inference. The core of the student project is in the research of effective and efficient online learning/fine-tuning methods, and the objective will be that the algorithm(s) of choice will be suited to run on (our) neuromorphic processors. This fine-tuning should result in competitive accuracy for the specific task or enable more efficient inference by increasing spatio-temporal sparsity during inference. A particular niche area of interest lies in **exploring self-supervised learning algorithms** [2].

public

One of our target neuromorphic processors contains several RISC-V cores connected through an interconnected network. A key feature of our hardware is its event-driven operations (a process in a RISC core only triggers an event). Additionally, the different cores work independently from each other. These two constraints impose the implementation of an **event-driven, distributed, and local learning mechanism**. Another neuromorphic architecture is based on digital ASIC technology with in-processor distributed memory featuring a combination of multi-layer perceptrons and liquid state-machines with basic IF/LIF neurons interacting asynchronously with each other and across layer. Under sparse operation the tiny microprocessor consumes only pJ of energy [3], which makes it ideal as a sensor payload. The goal would be to equip it with a fine-tuning capability that would allow it to self-customise in-situ and perform well across deployments.

The project duration is 9 to 12 months (optionally combining internship and M.SC. thesis). The results of the project may be published in high-impact journals and may as well be patented.

We are welcoming collaboration with laboratories that can help us bridge the gap among neuromorphic technologies and applications in biomedical signal processing, neuromorphic and machine learning integration methods, circuits and systems non-conventional computing and learning architectures.

We seek motivated candidates with a relevant background in one or more of the fields of neuromorphic computing/engineering, optimization for neural network learning, statistical inference and probabilistic learning models. The candidate must have good programming skills in Python (with desired experience TensorFlow and/or PyTorch) and embedded C++ programming (for RISC-V programming). The interested applicants should submit their CV, the academic transcripts (including the scores and the courses).

References:

[1] Deep Learning using Transfer Learning (https://towardsdatascience.com/deep-learning-using-transfer-learning-python-code-for-resnet50-8acdfb3a2d38)
[2] Self-supervised learning: could machines learn like humans? (https://youtu.be/7I0Qt7GALVk)
[3] µBrain: An Event-Driven and Fully Synthesizable Architecture for Spiking Neural Networks (https://www.frontiersin.org/articles/10.3389/fnins.2021.664208/full)

Tasks (specific)

- Literature review on neuromorphic architecture and relevant learning algorithms
- Identifying 1-2 suitable algorithms and applications for (self/partially-)supervised learning/fine-tuning (potentially extending existing work in the topic)
- Implementation / validation of the selected learning algorithm in python
- Application of the algorithm on the neuromorphic platform and testing
- Thesis writing and documentation in Imec Holst-Centre

Required skills *(the lines that are already added are mandatory)*

- Very good/excellent in python (desired experience in TensorFlow/PyTorch) and embedded C (++) programming
- Knowledge of (Deep) Neural Networks training algorithms internals (some experience in optimization, statistical inference and probabilistic learning, or statistical signal processing, is a plus)
- A structured way of reporting, both orally and written
- Motivated student eager to work independently and expand knowledge in the field
- Good written and verbal English skills

public

Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or above IMEC supervisors
EPFL responsible supervisor (IS-Academia registration): Alexandre Schmid

IE2	**Event-based (Neuromorphic) radar signal encodings**

Project in collaboration with IMEC Holst Center, Neuromorphic Group.
The expected length of the project dictates that the MSc project and internship should be devoted to the project.

General information	
Daily Supervisor IMEC-NL	**Manolis Sifalakis**
Second supervisor IMEC-NL *(optional)*	**Federico Corradi, Amirreza Yousefzadeh**
Department *(pick one)*	IoT
Team	**NLICDESIGN**
Interviewers for this project *(at least Project Lead/Hiring manager and a team member)*	M.S., F.C., A.Y., M.K. (R&D Manager)

Assignment	
Title	**Event-based (Neuromorphic) radar signal encodings**
Small introduction project *This text will be visible on the homepage of the thesis opportunities*	At Imec's Holst-center lab in Eindhoven we are developing a novel neuromorphic radar sensor backend called event-radar that targets always-on low-power sensing, sparse data streaming, and on-sensor processing. In-line with this work we seek for a motivated student to undertake a project, which will focus on exploring and developing temporally and spatially sparse (event based) encodings of radar signals for short-range radar application tasks (gesture recognition, vital sign detection, room activity classification). The objective will be that these signals can be generated and used for inference right at the sensor (low-power budget and real-time application inference).
Duration assignment *(note: BSc projects are max 6 months)*	☐ 9 to 12 months ☐

Student profile	
Level of education	☐ M.Sc.
Required program *(choose programs)*	☐ Electrical/Computer Engineering ☐ Computer Science ☐ Neuromorphic engineering

Project description (a clear description of the project)
[To be considered for this position: The European candidates must be enrolled in a Master program. Non-European master students who are enrolled in a Dutch university are also welcomed to apply] Typically, most sensors today (camera/microphone/radar/etc.) generate a lot of data that need to be communicated for processing/inference by a model. This allows the sensor to do little processing work at the expense of the bandwidth that is needed to communicate the data to the downstream processing pipeline.

public

By contrast neuromorphic sensors (dynamic vision sensor [1], cochlea audio sensor [2], e-skin sensor [3]), inspired by sensory processing principles in the brain, consume significantly less power, and generate sparser temporal signals. A big advantage of this paradigm is that it leaves resources for application-related processing right at the sensor as well. Towards a similar objective in the neuromorphic group of IMEC (Holst-Centre lab, Netherlands), we have been developing an analogous neuromorphic radar-sensor backend, for indoor or short distance sensing applications (think of gesturing commands, human activity, vital signs, etc in an office space, or automotive application).

The goal of this project will be to explore various temporal encodings and sparse distributed representations of the radar signals, their suitability for embedded low-power processing and their efficacy in machine learning related application tasks.

For example, a baseline exploration point can be a **differential encoding** (delta or sigma-delta modulator), and one may move on to introduce reverberating dynamics with neural networks such as **echo-state networks** (liquid state machines) that can be "nudged" to resonate according to the radar front-end detections, or move to trainable **sparse signature representations** [4]of the activity taking place in front of the sensor.

The results of this exploration will be compared with more common-place traditional radar DSP pipelines (e.g., FFT based) and evaluated in various application tasks such as those listed above.

Project duration is set to 9 or 12months (e.g., internship and MSc project) and depending on outcomes, there will be opportunity to patent or publish the results in high-visibility conference or journal in the field.

While the work is primarily algorithmic, depending on competence and interest, the student may also have the opportunity to work directly with the radar sensor hardware prototype and novel neuromorphic accelerators, for collecting data and running experiments.

Candidates are expected to be highly motivated, with relevant background in one or more of the following fields: sensor signal processing, neuromorphic computing/engineering, optimization and learning in neural networks, statistical pattern recognition / probabilistic learning models. The candidate must have good programming skills in Python and reasonable exposure to C/C++ (there will not be opportunity to learn elementary programming during the project). Interested applicants are welcome to submit their CV, and academic transcripts (courses taught, and scores or level attained wherever applicable).

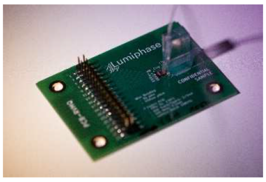
References:

[1] Galego et al. (2020). Event-based vision: a Survey. IEEE transactions on Pattern Analysis and Machine Intelligence.
[2] S.Liu et al. (2014). Asynchronous Binaural Spatial Audition Sensor With 2x64x4 Channel Output. IEEE Transactions on Biomedical Circuits and Systems.
[3] F.Bergner et al. (2020). Design and Realization of a Resistive Efficient Large-Area Event-Driven E-Skin. MDPI Sensors.
[4] W. Brendel et al (2020). Learning representations spike-by-spike. PLOS Computational Biology,

Tasks (specific)

- Literature review on neuromorphic sensing and processing
- Plan exploration for a small set of designed encodings/representations (define criteria of interest and application of interest)
- Implementation of resp. representation algorithms

	- Performance testing and evaluation, comparison with contemporary radar DSP pipelines - Thesis writing and documentation in IMEC Holst-Centre **Required skills** *(the lines that are already added are mandatory)* - Very good/excellent programming in python and at least intermediate programming in C/C++ - Good background in one or more of: - Sensor digital signal processing (radar DSP preferable) - Neuromorphic computing/engineering - Optimization for learning in Neural networks - Statistical pattern recognition - A structured way of reporting, both orally and written - Motivated student eager to work independently and expand knowledge in the field - Good written and verbal English skills public Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or above IMEC supervisors EPFL responsible supervisor (IS-Academia registration): Alexandre Schmid
IE3	**Internship at Kandou Bus SA** - Signal processing and modeling: the students will help model complex analog circuits using signal processing techniques. Knowledge of analog circuits is a plus, but we will be able to teach them the required knowledge if they have a firm knowledge of signal processing. Programming skills in Python, C, or C++ is a big plus. - Digital circuit design: the students will help with the design of control circuitry for very high speed serial links. Knowledge of standard tools from Cadence or Synopsys is a must. - Analog circuit design: the students will help the Advanced R&D lab members design very high speed and very low power serial links. Knowledge of standard tools from Cadence or Synopsys is a must.

	Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or Kandou Bus SA supervisors, Aminn Shokrallahi, Armin Tajalli, Chloe Joubert (amin@kandou.com, armin.tajalli@kandou.com, joubert@kandou.com)
IE4	**Internship at Lumiphase AG, Firmware and electronics development** Project available as MSc diploma or internship **Project 4: Firmware and electronics development** The goal of this project is to develop the electronics of different setups used to analyze the performance of Pockels-enhanced silicon photonics circuits.  The work during the internship is technology-driven and includes: • Firmware development on a microcontroller, and development of an API to interact with it from a computer; • Designing, testing and improving PCBs, used for example to interface the microcontroller with the rest of the setup and with our devices; • Implementing and characterizing control methods to stabilize our device at the desired operating point; • Working on a customized electrical/optical setup, including the design and assembly of hardware components; • The duration of the project work will be determined in accordance with the regulations of your university but needs to be at least 6 months. The ideal candidate should bring: • Strong interest in simulation and experimental work with integrated photonics and nano/microelectronics; • Good programming knowledge, ideally in C. • Small experience with microcontrollers (lecture, lab courses, ...) Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) or Lumiphase AG supervisors Caroline Rossier (caroline.rossier@lumiphase.com)

Application development (software development)

SW1	**Peripherals for an FPGA development environment** Diverse analog and digital interfaces are classical peripherals used in modern consumer electronics. Physical devices are used in all practical implementations. The latter may consist of sensors or actuators that obey certain protocols or signal timings. Increasingly, such interfaces are offered in a virtual implementation, that is as a dynamic image on a touchscreen. This project aims at creating such an environment to the terasic DE10-Lite on-board peripherals such as an accelerometer, VGA display connectors and integrate the new system into the logisim-evolution design flow. As a result, the environment should present the new peripherals both available in logisim-evolution. Project breakdown 20% documentation study, procedure development 50% software development (VHDL) 30% logisim-evolution inclusion Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
SW2	**Implementation of a GCC-based compiler compatible with a RISC processor for biomedical applications** The goal of this project is designing a compiler for a novel RISC processor suitable for biomedical implants. A compiler is responsible for decomposing a basic language code such as C or C++ to run on a CPU. The efficiency of a compiler is often determined by how much it condenses the code and instruction in the output executable file. The designed compiler will be based on GNU compiler collection (GCC) to compile a C program on a target RISC processor. The compiler consists of three main parts; a front end, a middle end and a back end. The front end is used to convert the C program to RTL format. Compiler optimization is performed in the Middle-end unit. Finally, the back end transforms the RTL format to the proper binary code which is executable for the RISC processor. GCC compiler is a free and open source software which will be used in this project. The front end and middle end of the compiler will be based on the GCC architecture. Some modifications should be applied to the back-end stage to generate appropriate machine codes for a RISC processor designed for biomedical implants. Main fields of the project: C and C++ programming, GCC compiler, software engineering, RISC processor Project breakdown: • Literature review (10%) • Front-end stage of the GCC compiler (20%) • Middle-stage of the GCC compiler (20%) • Back-end design compatible with RISC processor (40%) • Executing sample programs on RISC processor (10%) Contact person: Keyvan Farhang Razi (keyvan.farhangrazi@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid
SW3	**Peripherals for a AVR STK-300 environment** The AVR-based STK-300 development system is used in several courses in EPFL supporting microcontrollers classes. Along to existing peripheral boards, additional are being developed. Software libraries must be developed at assembly level to support e.g., Duinopeak 1,8" Color TFT (ST7735R controller), FT232RL (FTDI RS232 to USB). Project breakdown: • Literature review (10%)

	• Assembly development (80%) • Documentation (10%) Contact person: Alexandre Schmid (alexandre.schmid@epfl.ch) Responsible supervisor (IS-Academia registration): Alexandre Schmid