Cryogenic Transistor Model for CMOS Electronics Used in Quantum Applications

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Rhonexum, an incubated startup project in AQUA lab, drives the development of cryogenic electronics to meet the rising demand for fault-tolerant quantum computing. The so-called Cryo-CMOS chips serve as the solution to interconnection issues in large-scale systems. The lack of transistor compact models validated at cryogenic temperatures challenges low-temperature electronics design to meet the strict requirements. This issue leads to a costly and inefficient engineering iteration, where circuit performance in cryogenic environments cannot be verified before tape-out. Overcoming these obstacles with adequate technology will enable the emergence of the next generation of electronics waiting to be harnessed. In this context, Rhonexum aims to address this obstacle by introducing SPICE-compatible models that capture unique cryogenic transistor behavior, enabling circuit simulation down to 4 K.

Rhonexum prototypes a modeling service, called RX-Model, which involves transistor compact modeling and parameter extraction. The compact model of RX-Model stems from the simplified EKV (sEKV) MSFET charge-based model, which is a design-oriented model guiding designers to make the trade-offs within the analog design octagon. The transistor compact model is written in Verilog-A hardware language and compiled in SPICE simulators.

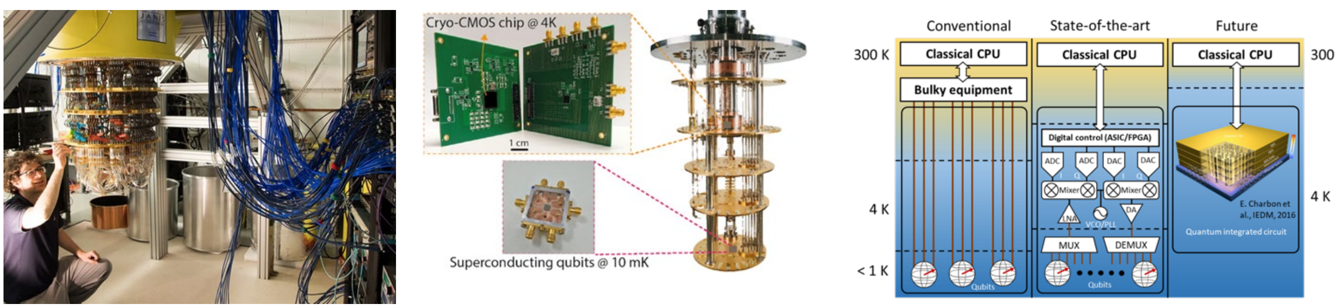

Figure 1. *Left: Google's quantum computer in 2019 has interconnection issues for large-scale systems [link]. Middle: Cryo-CMOS integrated into a dilution fridge at 4 K and manipulating multiple superconducting qubits residing at mK level [link]. Right: Progress in implementing quantum machines, envisioning the monolithically integrated quantum process in the future.*

The proposed thesis project involves the development of transistor compact modeling at cryogenic temperatures. The student will implement the SEKV compact model in Verilog-A with using Python to capture the dynamic behavior of transistors at room temperature and 4 K. With model parameters extracted, the student will perform transistor-level simulations based on the developed model and verify the result with the experimental data. The project will include the completion of the following tasks:

- **Extend the SEKV transistor compact model from DC to AC and RF domains**, which enables the circuit simulation to a broader operating regime.
    - Prototyping the compact model in Python.
    - Converting the model into Verilog-A.
- **Run transistor-level simulations using Ngspice or other software** to verify the SPICE compatibility.
- **Extract model parameters from measurement or PDK simulation** to capture the AC and RF behavior.
- **Verify the SEKV model with extracted parameters** by comparing the s to the experimental data.
- **Document the model developed in this project**.

This project aims to achieve a SPICE-compatible transistor model validated at cryogenic temperatures, allowing for circuit simulation. This project will encompass semiconductor physics and solid-state electronics expertise. Proficiency in Python programming will be essential for model development. Additionally, a basic understanding of Git will be beneficial for effective project management.