RTL implementation for real time FLIM measurements

Professor: Prof. Edoardo Charbon Office Mc A3.303 e-mail edoardo.charbon@epfl.ch
Lab deputy: Dr. Claudio Bruschini Office MC A3.307 e-mail: claudio.bruschini@epfl.ch

Scientific Assistant Contacts: Paul Mos Office MC A3.257 e-mail paul.mos@epfl.ch

Project Type: Master Thesis Section: Microengineering

Official Start Date: Anytime
Submission of Final Report: TBD
Presentations at Group Meeting:TBD

The concept of Fluorophore Lifetime Imaging Microscopy (FLIM) is widely used nowadays. It enables doctors to use minimal invasive methods to detect cancer and potentially, to operate surgeries in early stages. FLIM uses the lifetime response of fluorophores, which are excited with a laser with known wavelength and have a response in a fluorophore specific wavelength. Carcinogenic cells absorb the fluorophore and upon light excitation, they emit light with a different wavelength with a certain exponential decay, showing the location of the carcinogenic cells.

At AQUA lab state-of-art Single Photon Avalanche Diode (SPAD) sensors are developed. Such is SwissSPAD2, a gated binary frame imager. This chip has a resolution of 512x512 and a frame rate of up to 97kHz. Having a gated architecture makes it ideal to be used together with a picosecond pulsed laser. For FLIM application, this sensor is used to capture the exponential decay of targeted samples with known fluorophores and use phasor method to compute their lifetimes. Making real-time FLIM is the next logical step in cancer detection and would be of great help in clinical studies.

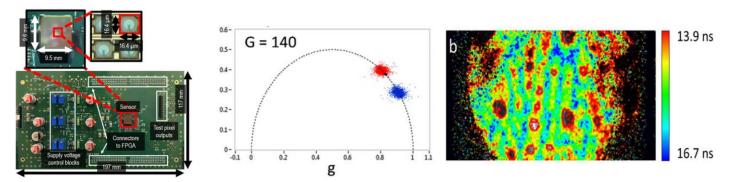


Figure 1. Left Camera module [1]. Center: Phasor scatter plots for the R6G and Cy3B. [2] Right: Color-coded phase lifetime maps

The student will learn about FLIM concept, lifetime computation with phasor algorithm. The student will do RTL design for a Xilinx FPGA that should process the phasor algorithm in the FPGA. To make the design time more time efficient, the student will use Vivado High Level Synthesis tool to translate C/C++ code into VHDL/Verilog and attend a training to quickly learn the tool. The algorithm consists of pile-up correction, background correction, phasor calculation, Instrument Response Function (IRF) deconvolution and phase lifetime calculation, with the prospects of adapting to two lifetimes applications.

The student will be familiarized with Xilinx FPGA, RTL coding and high-level synthesis concepts. Furthermore, student will learn about the FLIM applications and phasor method.

^[1] Arin Ulku et al 2020 Methods Appl. Fluoresc. 8 024002

^[2] A. C. Ulku et al., "A 512 x 512 SPAD Image Sensor With Integrated Gating for Widefield FLIM," in IEEE Journal of Selected Topics in Quantum Electronics, vol. 25, no. 1, pp. 1-12, Jan.-Feb. 2019, Art no. 6801212, doi: 10.1109/JSTQE.2018.2867439..