ASIC design engineer in microelectronics for the FLARE project: FADC for the CTA (m/f/d)

Description of the project

The project aims to design a fast ADC (FADC) to be employed with cameras for gamma-ray telescopes. Over the next years, a new camera based on silicon photosensors (SiPM) will be developed with the scope of offering a future solution to equip the large telescopes (LST) of CTA (https://www.cta-observatory.org). The use of SiPM combined with the development of innovative readout electronics will not only increase the duration of observations while increasing the robustness of the camera, but also improve performance over the entire energy spectrum.
The Aqua group at EPFL, in Neuchâtel, has a mission to model and develop hardware/software systems based on quantum devices. Emphasis is on high-speed 2D/3D optical sensing, embedded & reconfigurable processing architectures, single photon avalanche devices (SPAD) and design optimization techniques. In this project, Aqua participates to the research and development for these innovative cameras within the LST collaboration, both for the front-end and the readout electronics.
The challenge of this project is to achieve the high speed that is required, while reducing the overall power needed by the 8'000 channels of the whole system. The project includes the design and production of a dedicated ASIC.

Job description

As a research engineer specialized in ASIC design, she/he is involved in the specification, design and schematic, layout, test and qualification of the FADC chip, within the framework of the FLARE (FADC).
She/he imagines, proposes and develops new solutions considering theoretical, technical, and technological aspects, to be evaluated and coordinated with various internal and external partners. She/he details and justifies the preferred alternatives and presents them in a documented way to the internal partners as well as to the external partners.

Functions

As a research engineer specialized in ASIC design, she/he performs ASIC development and prototyping for the front-end electronics of the FLARE (FADC):

- Planning of the project
- Definition of specifications
- Circuit design and layout
- Simulation
- Testing and verification
- Writing of the technical documentation
- Participation in teamwork and in meetings

As a part of the Aqua group, with the help of the other engineers, she/he participates in the development of the following:

- HDL firmware writing, to target an FPGA, to configure and interact with the FADC
- PCB design, to test and characterize the FADC
- follow-up of the project
- redaction of the documentation and publications

- presentations of the work done

Qualifications

- Engineering degree or equivalent with additional training and relevant experience oriented towards electronics, computer science and development of ASIC
- A few years of professional experience in the development of complex ASICs
- Good knowledge of electronics and excellent knowledge of computer tools for ASIC design and simulation (Cadence)
- Mastery of VHDL and/or Verilog and FPGA development
- Knowledge of PCB design or else a strong desire to learn it
- Written and oral proficiency in English
- Mastery of office tools (Word, Excel, PowerPoint, etc.)

Soft skills

- Conciliation and negotiation
- Manage, plan, and anticipate tasks
- Organize large international projects
- Manage multiple tasks in parallel
- Follow, acquire, and master the high-tech

Language skills

Fluency in written and spoken English is required, as well as the ability to understand and speak English in professional context. A good command of French is desirable.

Advantages

Varied activity in a stimulating laboratory of the EPFL.
Pleasant working atmosphere.

Additional information

The place of work will be the Aqua group laboratory, at Microcity, in Neuchâtel, Switzerland.
The salary depends on experience and qualification.
It is a full-time job, that can start immediately
Applications should be done on the portal:
https://www.epfl.ch/about/working/working-at-epfl/job-openings/
Please, also send a mail to both of the person below to inform them about your application:
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