**Development of Megapixel SPAD camera**

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*Project Type: Semester Project Section: Microengineering*

*Official Start Date: TBD*

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*Presentations at Group Meeting: TBD*

Large scale SPAD cameras are successfully used in various applications. Its single photon sensitivity and CMOS compatibility make it possible to implement SPAD sensors with in-pixel circuits.

At AQUA lab, state-of-art SPAD sensors are developed. MegaX [1], the first megapixel SPAD camera with gating circuits, allows us to register only the photons impinging the detector within a certain gate window. Recent results in Figure 1 show promising performance for applications that require accurate timing, such as Fluorescence-lifetime imaging microscopy (FLIM) [2] and multidimensional imaging [3]. These results are achieved by gating operation of the camera.

In order to achieve higher photon detection efficiency and higher resolution, share pixel readout were also designed for this camera.

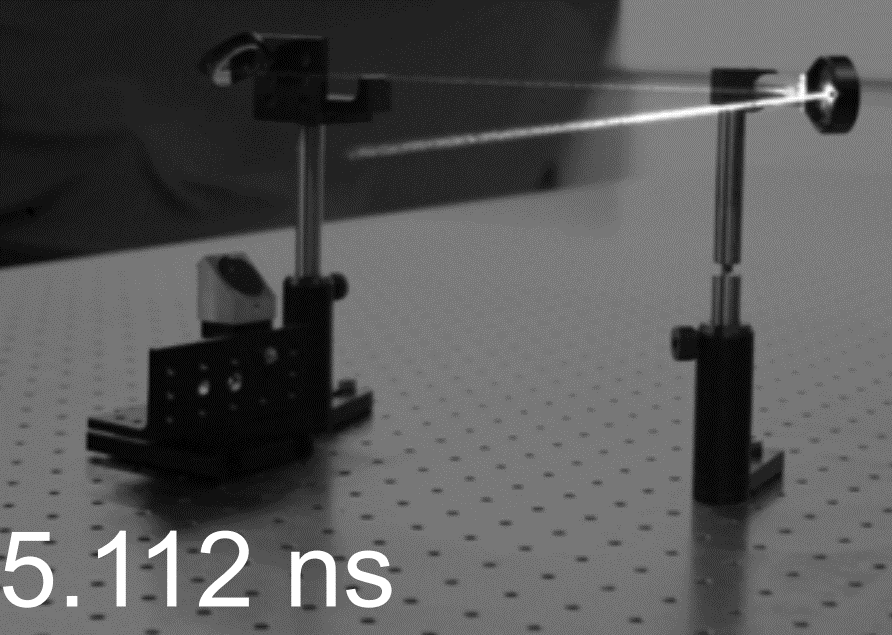
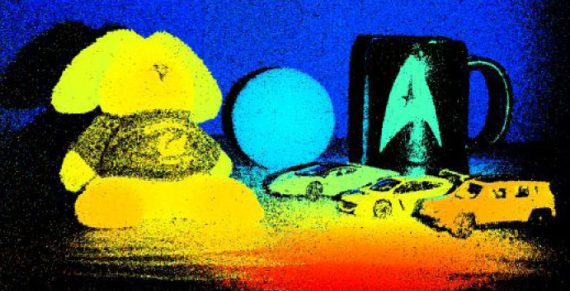
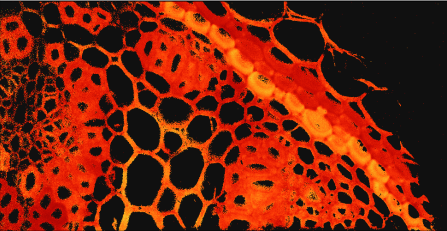
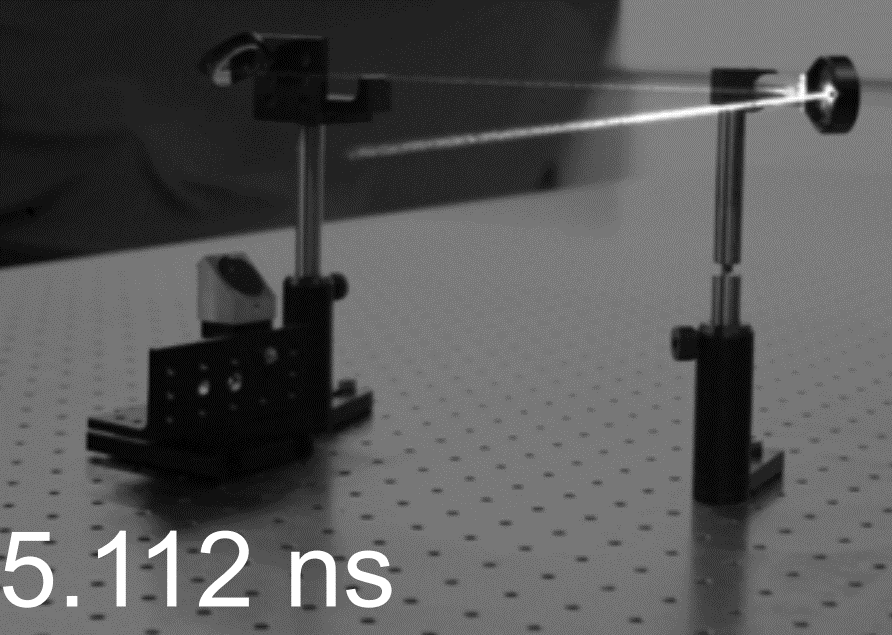


Figure 1. 3D mapping [[[1]](#footnote-1)]. Center: FLIM [2]. Right: 4D imaging[3].

The student will learn about SPAD operation and how large scale SPAD camera works. The student will do HDL design for a Xilinx FPGA. The student will develop and optimize the gating mode firmware for share pixel readout architecture. The student will also learn about how to apply the developed camera on different applications, and explore new applications if time permits.

The student will be familiarized with Xilinx FPGA, and HDL design through working with a large scale SPAD camera.



**Description**:

Large scale SPAD cameras are successfully used in various applications such as Lidar, Fluorescence-lifetime imaging microscopy (FLIM) and multidimensional imaging. It’s single photon sensitivity and CMOS compatibility make it possible to implement SPAD sensors with in-pixel circuits. MegaX, the first megapixel SPAD camera with gating circuits, allows us to register only the photons impinging the detector within a certain gate window for accurate timing.

**Objective**:

In order to achieve higher photon detection efficiency and higher resolution, share pixel readout were also designed for this camera. The student will learn about SPAD operation and how large scale SPAD camera works. The student will do HDL design for a Xilinx FPGA. The student will develop and optimize the gating mode firmware for shared pixel readout architecture. The student will also learn about how to apply the developed fully-operating Megapixel SPAD gating camera on different applications, and explore new applications if time permits.

The student will be familiarized with Xilinx FPGA, and HDL design through working with a large scale SPAD camera.

Project Type: Semester project

Official Start Date: ASAP  
Submission of Final Report: TBD  
Presentations at Group Meeting: TBD

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1. [] Morimoto, Kazuhiro, et al., Optica 7.4 (2020): 346-354.

   [2] Zickus, Vytautas, et al., Scientific Reports 10.1 (2020): 1-10.

   [3] Morimoto, Kazuhiro, et al., Physical Review X 11.1 (2021): 011005. [↑](#footnote-ref-1)