M.Sc. Project Proposal

Testing of a 512×1 Event-Driven Linear SPAD Array

General Information:

Laboratory: Advanced Quantum Architecture Laboratory (AQUA)
Partners: EPFL
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Location: Microcity, Neuchâtel (travel and lunch allowance - lump sum)
Starting date: ASAP
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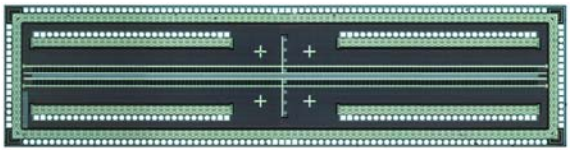
Project type: M.Sc. project (4 months full time)

Background:

Single-photon avalanche diodes (SPADs) are photon-counting detectors that can be combined with CMOS electronics in a single integrated circuit. Thanks to their picosecond timing resolution and low dark count, SPAD arrays have gained popularity in time-resolved imaging applications such as LIDAR, PET, low-light-level imaging, super-resolution microscopy, and fluorescence lifetime imaging microscopy (FLIM). Linear SPAD sensors are particularly useful in 3D time-of-flight imaging, thanks to their ability to scan a wide field of view by moving in a single direction. Fully integrated readout electronics, while increasing overall camera speed and allowing more compactness, do not allow much flexibility in programming the operation settings. Therefore, these conventional approaches can limit the range of applications of these sensors. In-pixel electronics also reduce the fill factor in monolithic processes, therefore limiting the single-photon sensitivity of these sensors. To overcome these problems, we have designed a 512×1 SPAD array with minimal on-chip electronics. The control and readout blocks will be implemented on an FPGA, starting from existing firmware; the FPGA can be reconfigured on demand.



Objectives:

The objective of this project is to characterize and test the 512×1 linear SPAD array. The detector and system performance parameters to be measured are dark count rate, photon detection probability, dead time, and maximum excess bias. The first task towards this goal is to develop a camera module based on a commercial FPGA board. The part to be designed is a sensor board with the chip mounted on it, which is compatible with the FPGA board. The second task is to develop the readout block of the sensor, starting from existing firmware. The lack of on-chip electronics resulting from the reconfigurable structure requires the implementation of readout modules on an FPGA, using VHDL. The firmware needs to send the control signals to the chip for the desired operational settings, and collect the detected photons with their address in the array and timing delay from the laser pulse, in an event driven configuration. Finally, the information needs to be stored in the on-board DDR3 RAM blocks, and transferred to the PC via USB 3.0. Further specifications of the control and readout modules will be finalized depending on the details of the target application.

Tasks:

- Literature research
- Chip-on-board/package bonding plan for the sensor board
- Design of the sensor board using a PCB drawing software

- Development of the firmware in VHDL to perform 3D time-of-flight imaging
- Testing of the detector and system performance
- Demonstration time-of-flight imaging