Multi-Processor Platform based on URLAP

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Outline

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  - The GP Interface
  - The Communication Layer
  - The Support Layer
- Planned tasks
- Future tasks and cooperation's

Motivation

- Due to the developments in technology, we are able to integrate very large systems on chip.
- Currently used communication media are not able any more to meet the requirements
- Due to large integration, power consumption is a major issue
- Process variability starts to become an important issue
- All these developments lead into the search for new methodologies, like:
  - Network on Chips (NoC)
  - Self Calibrating Circuitry (SCC)
  - Distributed on Chip Processing

Motivation (1)

- Each of these methodologies can be validated by simulation, but:
  - URLAP in simulation: about 40 kHz on a P4 3.2 GHz
  - URLAP in real life: 140 MHz
- Hence there are several orders of magnitude of difference between simulation and real operation
- Even more severe, in case of a complete system, simulation would take too much time to be of use
- A real-time or semi-real-time validation platform is required
- A reconfigurable platform can serve our purposes

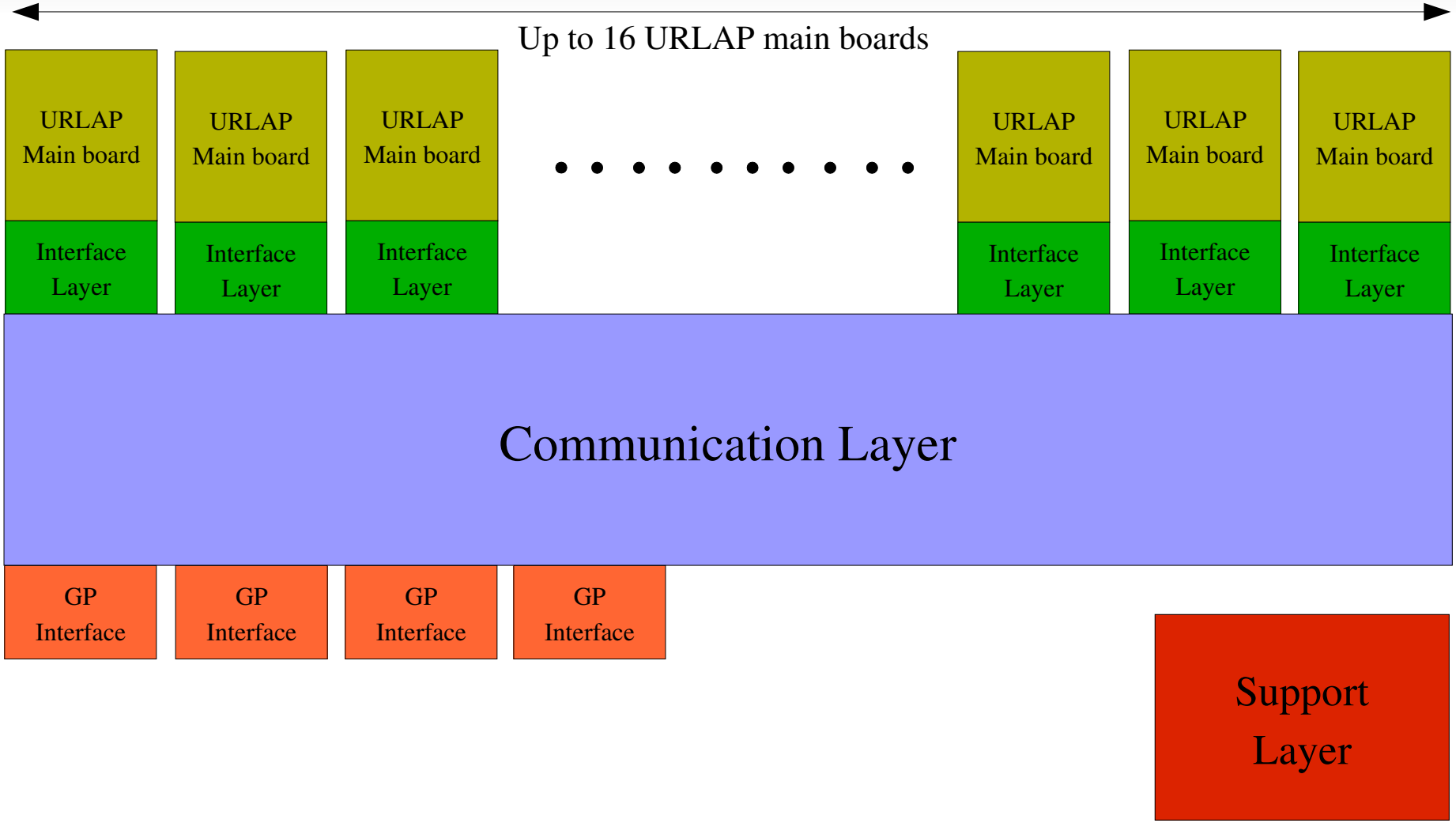
Motivation (2)

- Currently available reconfigurable platforms are FPGA based with up to 4 integrated processors (PowerPC or ARM)
- Each of the available development boards provide or too much features, and/or lack an important feature
- The integrated processors are fixed, and cannot be easily modified (e.g. they all run at a fixed clock and voltage)
- Often for systems interest, the FPGA devices are too small, hence optimization or reduction is required
- Current industrial system on chips contain a large number of processors and ASU's

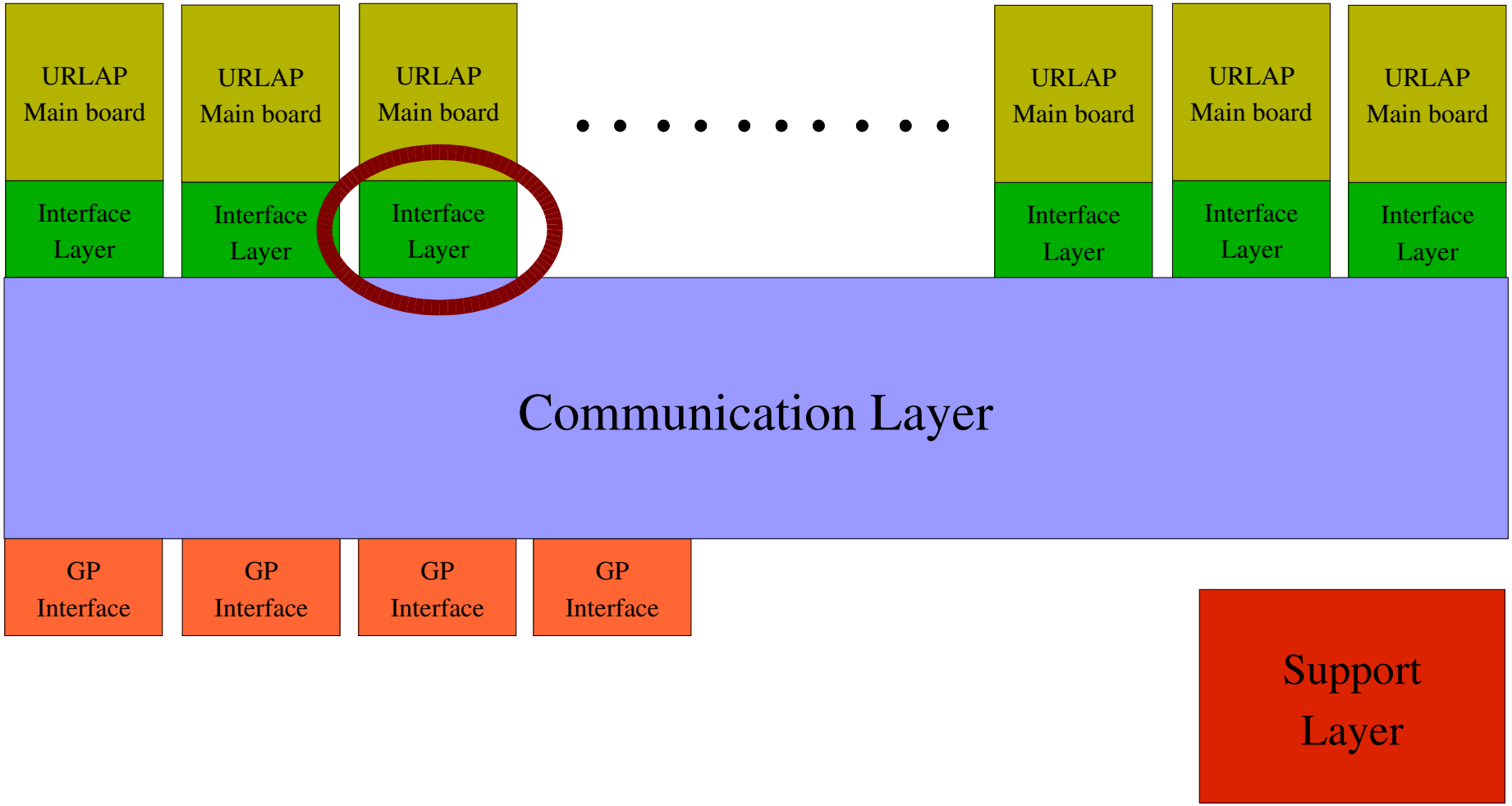
Motivation (3)

- To be able to circumvent the given restrictions of the available boards, we started the URLAP multi-processor platform, providing:
  - A well known and modifiable industrial strength processor (URLAP)
  - A modular FPGA architecture providing the means of implementing large communication arrays and reconfigurable Application Specific Units or processors
  - A fast interface to a standard PC for debugging, profiling, observation and (partial re-) configuration
  - A clocking scheme, which allows for complete synchronous, Global Asynchronous Local Synchronous and/or global and local Dynamic Frequency Scaling

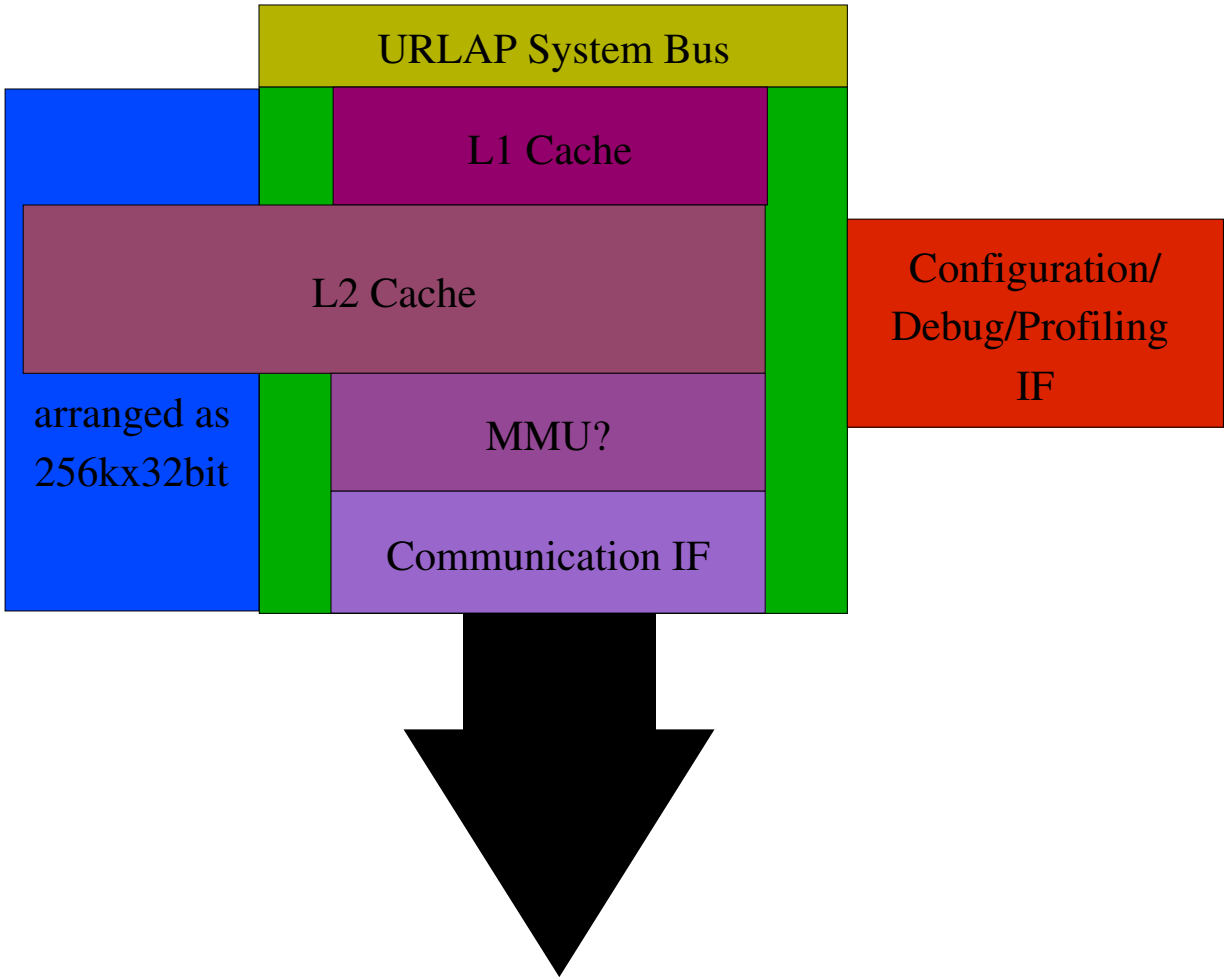
Architecture



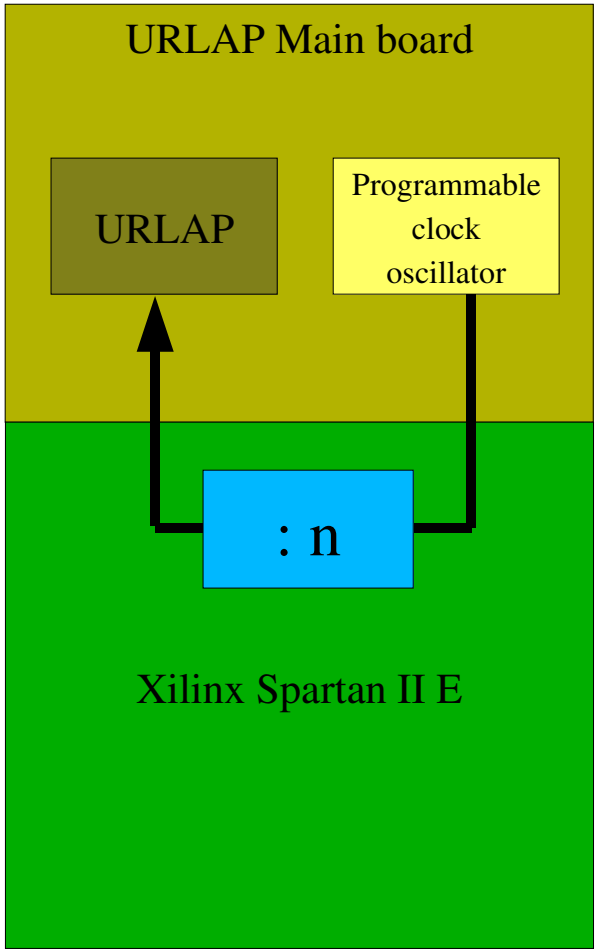
Interface Layer



The Interface Layer

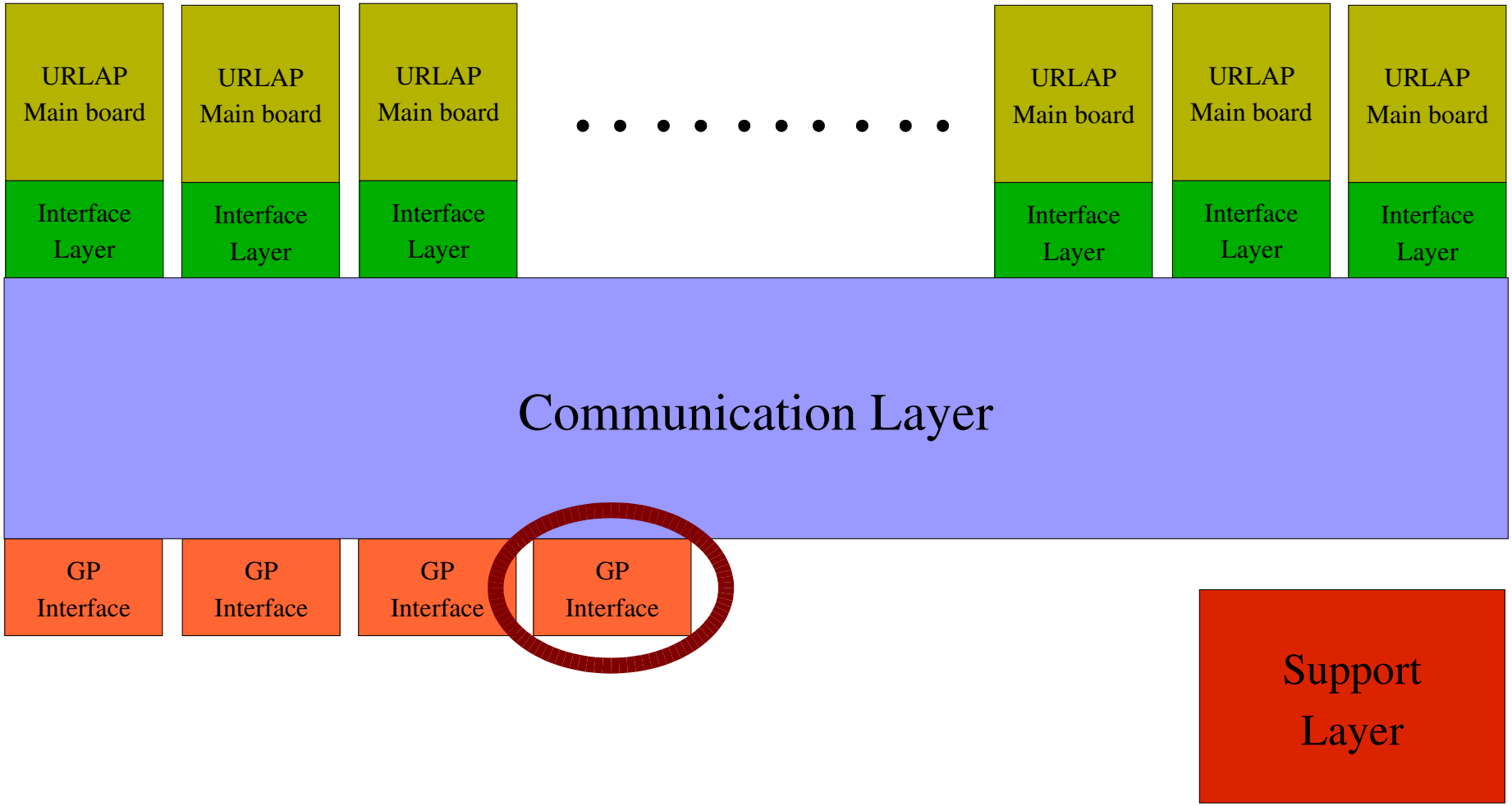


URLAP Clocking



- Two Clocking schemes:
  - Slowly changeable: Programming the I2C on-board clock oscillator (60Hz -> 200 MHz)
  - Fast changeable: Implement a divide by n clock divider (linear regulation of frequency)
- Stalls are handled by "stretching" the clock

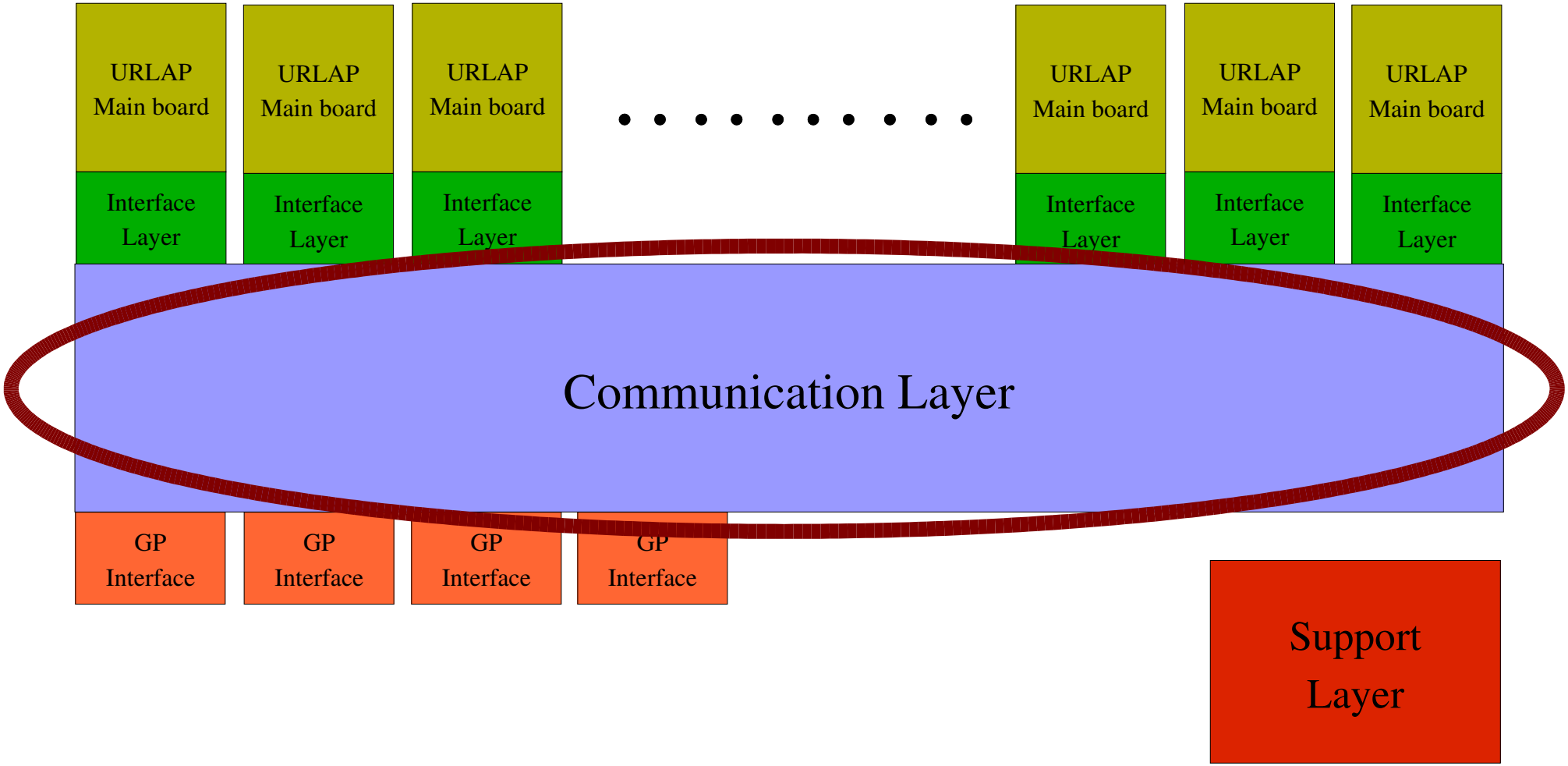
The General Purpose Interface



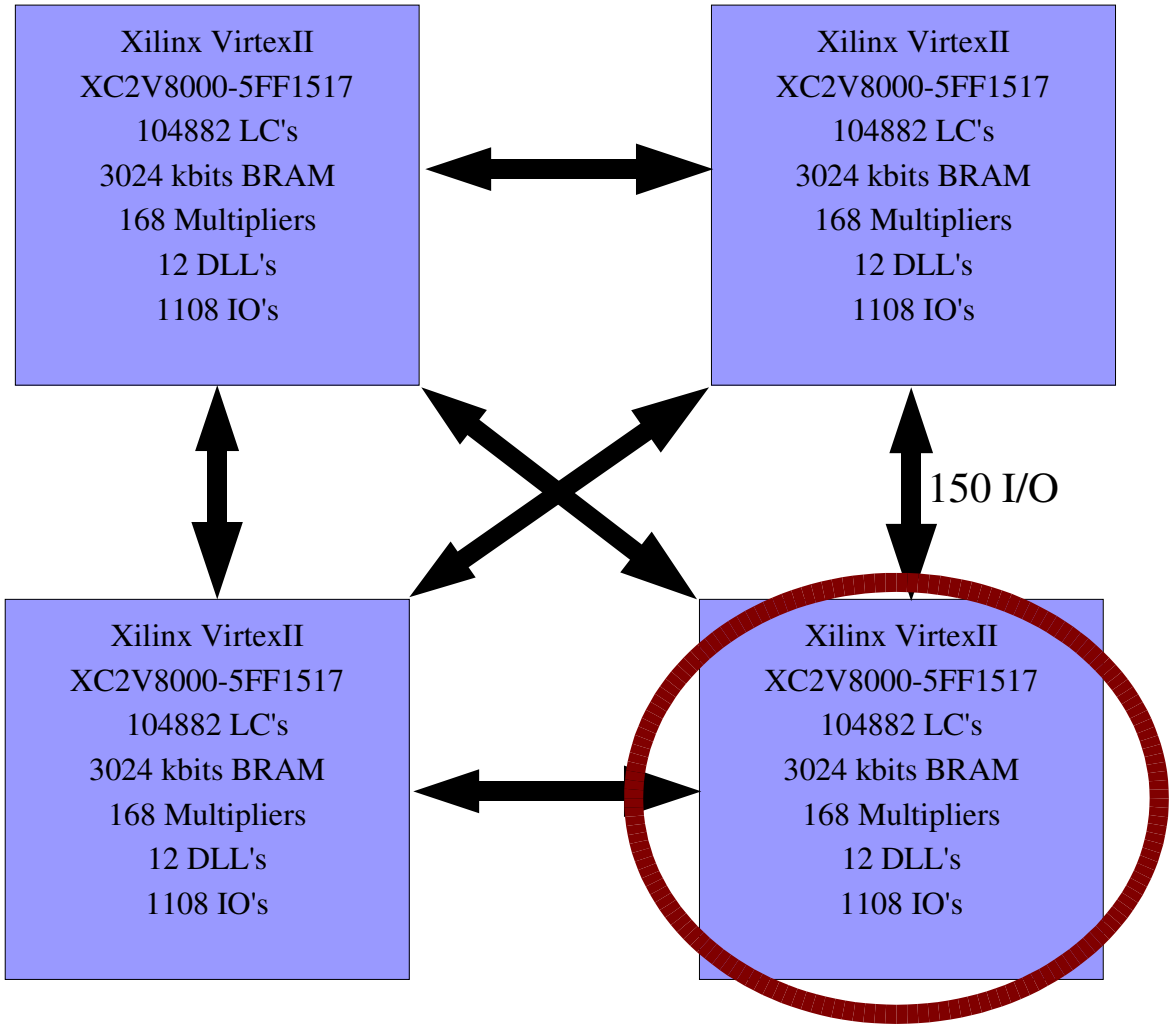
The General Purpose Interface

- The GP Interface uses the same interconnect as the URLAP main board
- The GP Interface can hold:
  - Another URLAP Board
  - A board with another processor
  - An Ethernet interface (10Mb/100Mb/1Gb)
  - General Input/Output cards (AD/DA, Camera's , etc.)
  - ...

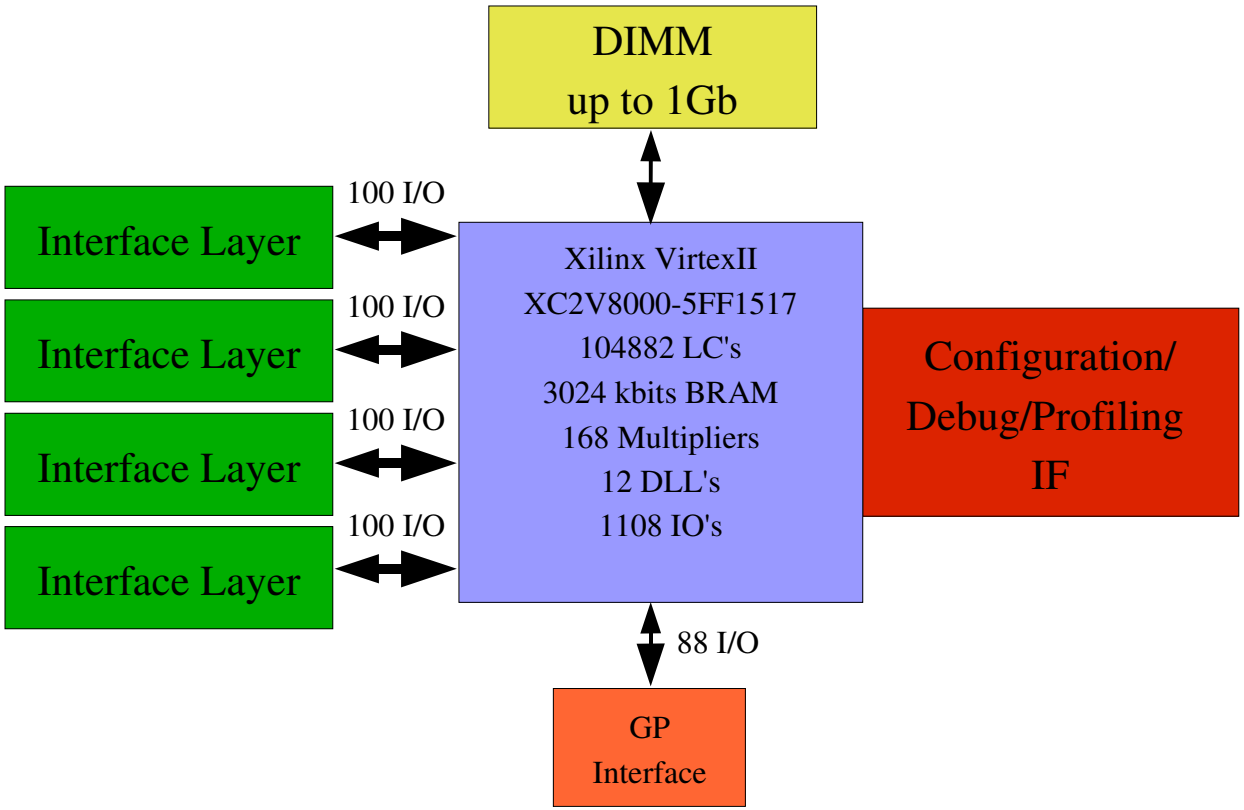
Communication Layer



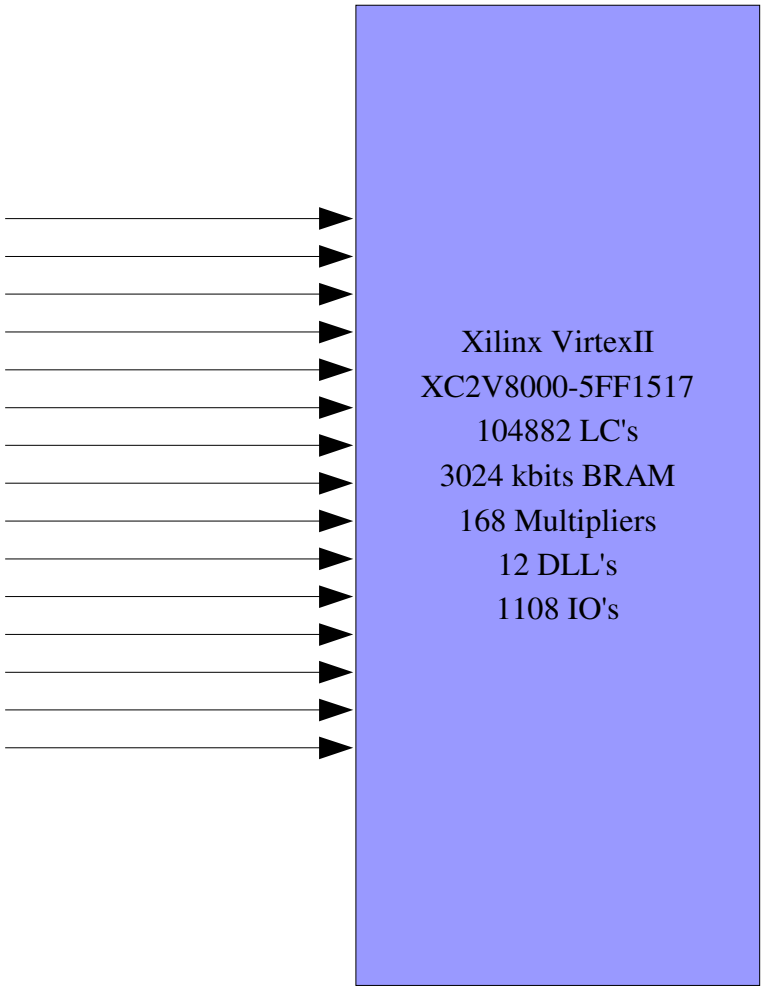
Communication Layer (1)



Communication Layer (2)

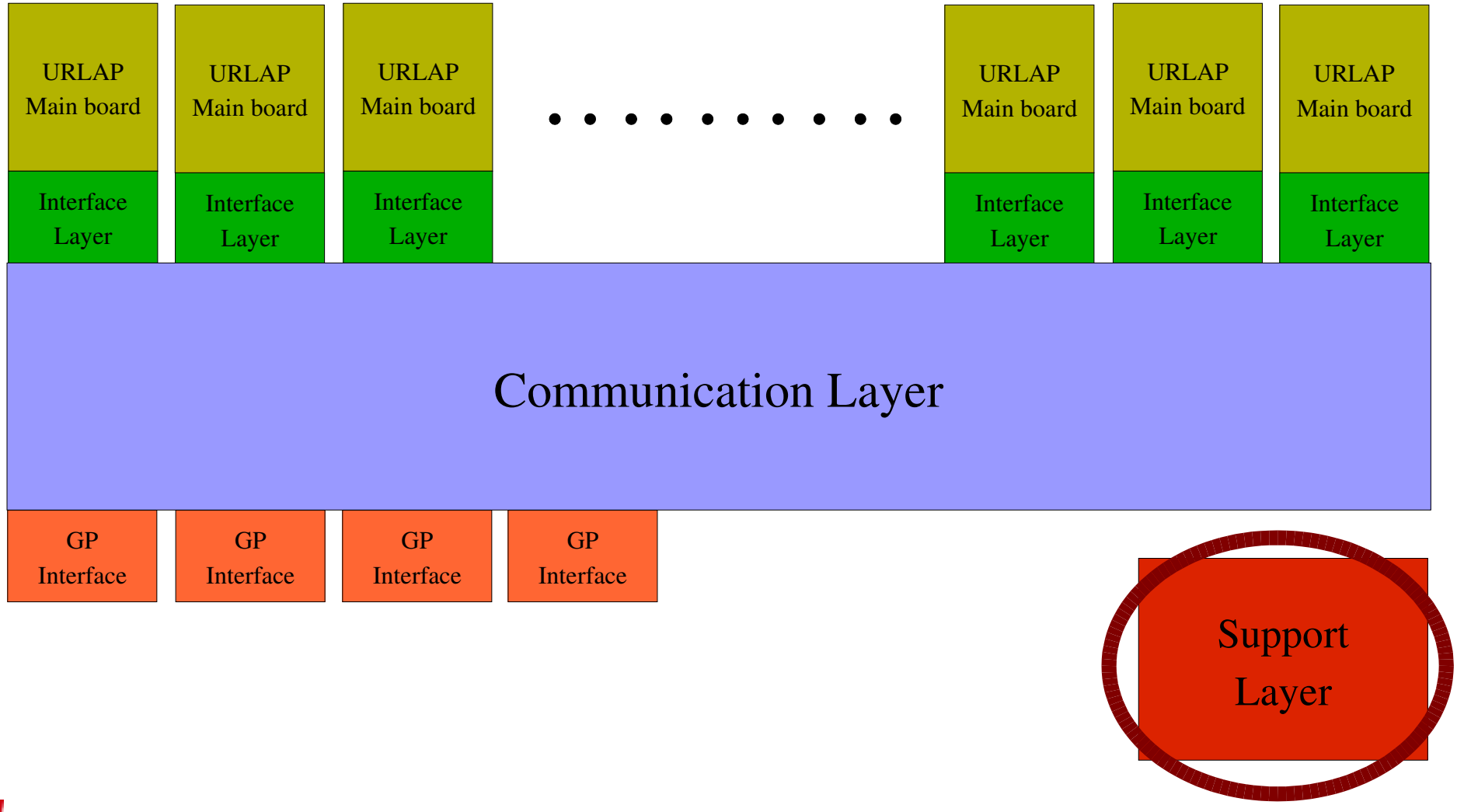


Clocking



- The Programmable Clock oscillator on each URLAP Main board can generate six (semi) independent clocks (67kHz .. 200MHz)
- 15 URLAP Main board will provide 15 independent clocks to each of the Virtex devices in the communication layer

Support Layer

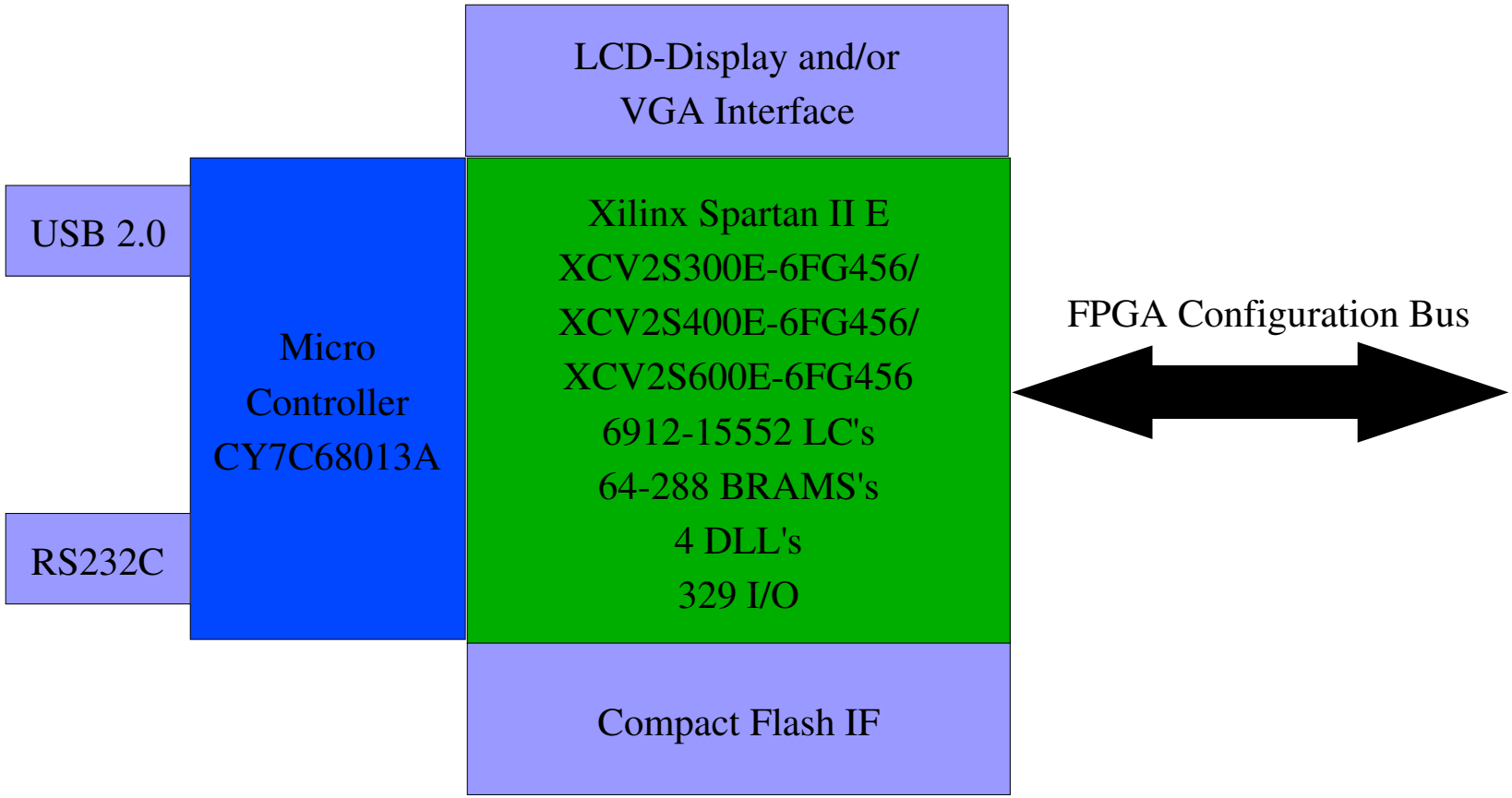


Support Layer (1)

- Required tasks:
  - Provide Fast communication to PC
  - Provide Boot Up configuration
  - Provide Debug capabilities
  - Provide Profiling capabilities
- Nice to have:
  - Provide partial reconfiguration of FPGA support
  - Provide DVS capabilities
  - Provide Power consumption monitoring

Note: DFS is already provided as presented earlier

Support Layer (2)



Donation

- Xilinx academic program donates:
  - 17 x XCV2S600E-6C FG456
  - 4 x XC2V8000-5C FF1517
- A total worth of $45,266

Planned Tasks

- PCB Design (Beatrice Forster, Theo Kluter)
  - Micro-ATX Form Factor
  - Powered by standard ATX Power Supply
- Initial system test (Beatrice Forster, Theo Kluter)
- L1 and L2 Caches in the Interface Layer (Beatrice Forster)
- eCos on URLAP (Claudio Favi)
- Currently planned completion date: 15-10-2005

Current team

- Project Directors:
  - Prof. Paolo Ienne
  - Prof. Edoardo Charbon
- Project Advisor's:
  - Rene Beuchat
- Project Supervisors:
  - Theo Kluter (Architectural [HW])
  - Claudio Favi (Architectural [SW])
- Project Students:
  - Beatrice Forster

Future

- We need a communication layer (NoC?)
- We need debugging and profiling support
- We need I/O support (MPEG streams, Camera Data, etc.)
- We need novel ideas to be tested real-time on this platform
- We can go for real power-aware computing (as far as DFS is concerned)
- We want a bigger team, as this platform provides opportunities for REAL research
- We have the complete knowledge of the platform as well as the processors, let's use it!

Future

Time for
DISCUSSION