Solid-State Imaging: Architectures and Techniques

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Imaging A/D Conversion

Courtesy:
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Reading


Objectives

• Provide an introduction to
  • A/D converters for image sensors
  • Motion detectors
  • Adaptive photodetectors
  • Spatial processing
A/D Converters

• Symbols

D    A    A    D

• Parameters
  – Input range (min max input)
  – Resolution (# bits)
  – Conversion time
  – Linearity (INL, DNL)
  – Quantization noise
Conversion Characteristics

- Quantization error
- Output code
- Input
- Differential error
- Resolution $\Delta$
- Ideal characteristic
Quantization Noise

Assume quantization step $\Delta$ and probability distribution function $E_n$ is uniform, s.t. $-\frac{\Delta}{2} < e < \frac{\Delta}{2}$, the noise power of a quantizer $\sigma^2_E$ is given by

$$\sigma^2_E = \frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}.$$

e.g. 8b ADC, 1V rail-to-rail input range, thus $\Delta=1/256\text{V}=4\text{mV}$

$$\sigma^2_E = \frac{\Delta^2}{12} = 1.27\mu\text{V}^2 \rightarrow \sigma_E = 1.12\text{mV}$$
Differential Nonlinearity (DNL)
Integral Nonlinearity (INL)

\[
INL = \int \text{DNL} \, dV. 
\]

*Input*: voltage, charge, current, time
A/D Conversion Strategies

• Chip-wide ADC
  – Slower but simpler
  – Less variability

• Column-wise ADC
  – Faster but more variability
  – More FPN

• Pixel-wise ADC
  – Fastest but
  – Extreme FPN
Flash ADC

- Fast
- Complex
- Limited #bits (usually 8~10b)
- High current consumption
- Accuracy depends on resistance matching

![Flash ADC Diagram]
Successive Approximation ADC

- N cycles required for full conversion (=#bits)
- Matching is good since the same components are recycled at every comparison
Recycling vs. Pipeline

1 bit conversion

Division by 2

1, 2, ..., N

1 bit conversion

M

+ Less hardware
+ Less variability
+ Conversion time

1 bit conversion

1 bit conversion

1 bit conversion

N

N-1

1

MSB

LSB
Single Slope ADC

- a.k.a “counting ADC”
- Speed is limited by settling time of comparator and ramp distribution
- Area and power consumption are low
- Comparator can be in pixel
Dual Slope ADC

- a.k.a ratiometric ADC
- More robust, as the integration time is fix
- Compute ratio betw. $V_{in}$ and $V_{ref}$, not the absolute value of $V_{in}$, thus higher accuracy may be achieved
Implementation

- Longer integration time
- Digital noise can be removed by choosing integration period as an integral multiple of period of interference
- Area and power consumption are low
Sigma-Delta ADC

- Tracks input with multiples of reference via feedback
- Recycle signal through same components
- High immunity to process variations
• Count “1”-s over $2^N$ clock periods, $N=\#\text{bits}$
• To reduce the #clock cycles, increase order of feedback
• Need to oversample signal to “push away” digital noise spectrum
Implementation (1\textsuperscript{st} order)

- **Block diagram**
- **Sampled data equivalent**
Theory

Difference equation

\[ y_i = x_{i-1} + (e_i - e_{i-1}) \]

In-band quantization noise

\[ n_0^2 = e_{rms}^2 \frac{\pi^2}{3} \left( \frac{2f_0}{f_s} \right)^3 = e_{rms}^2 \frac{\pi^2}{3OSR^3}, \]
Ideal 1\(^{st}\) order

\[ OSR > \left( \frac{\sqrt{3}}{\pi 2^N} \right)^{\frac{2}{3}}, \]

Ideal 2\(^{nd}\) order

\[ OSR > \left( \frac{\sqrt{5}}{\pi 2^N} \right)^{\frac{2}{5}}, \]

\( N = \# \) bits

<table>
<thead>
<tr>
<th>Architecture</th>
<th>8-bit</th>
<th>10-bit</th>
<th>12-bit</th>
<th>14-bit</th>
<th>16-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ideal First-Order</td>
<td>60</td>
<td>151</td>
<td>381</td>
<td>959</td>
<td>2418</td>
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<tr>
<td>Ideal Second-Order</td>
<td>17</td>
<td>29</td>
<td>50</td>
<td>88</td>
<td>153</td>
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</table>
## Summary

<table>
<thead>
<tr>
<th>Type</th>
<th>Resolution</th>
<th>Speed</th>
<th>Power</th>
<th>Area</th>
<th>Robustness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sigma-Delta</td>
<td>High</td>
<td>Slow</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Single/dual slope</td>
<td>High</td>
<td>Slow</td>
<td>Low</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Flash</td>
<td>Low</td>
<td>Fast</td>
<td>Very high</td>
<td>High</td>
<td>Med.</td>
</tr>
</tbody>
</table>
Imaging ADCs

• Commonly used: column-parallel ADCs
• Successive approx. ADCs generally best compromise betw. Resolution, speed, power

• Example (JPL):
  – 256 10b S/A ADCs
  – 24um pitch
  – 1/3 chip area
  – 20% power
  – 85kpps

Other Example:
  – 10b single-slope ADCs
  – 10um pitch

Commercial Example:
  – single on-chip ADC
  – 8b flash
Other Examples

- Stanford University has been developing in-pixel ADCs
  - first a $\Sigma$-$\Delta$ ADC per pixel
  - with 22 transistors per pixel
- And then a $\Sigma$-$\Delta$ ADC for a block of 4 pixels
  - with 4.25 transistors per pixel
  - 1 FET for each passive pixel
  - 13 for the ADC
  - and the signal is reconstructed by counting pulses off-chip (e.g. how many “1”s in 8 clock cycles)
  - fill factor 30% for 20x20$\mu$m pixel
  - published ADC read time is 1ms per pixel
Smart Pixels & Smart Readouts
Compression Philosophy

- Similar to focal-plane processing in retinal ganglia
- Conditional replenishment
- Basic idea:
  - Using global read, new pixel value is sampled and compared with stored one
  - If magnitude of difference greater than threshold, it is stored in memory, a flag is set
  - Else nothing is done
Smart Pixel Idea

• Event-driven readout
  – Flag used to activate an analog shift register. It indicates pixel readiness
  – (x,y) coordinate is also read out

• Threshold
  – Constant, thus variable # flagged pixels
  – Variable, thus constant # flagged pixels
  – Optimum conditions depend on motion rate and desired frame rate

• Example
  – 32x32 pixels, 33T 160µm² pixels with FF=1.9%
Motion Detection (MD)

- Objective of MD: determine the optical flow in space and time
  - Employ an algorithm that interprets motion as a whole, rather than just differences btw. Pixels
- Frame subtraction schemes only measure snapshots of the scene at discrete intervals
  - Thus simply differences in illumination and not overall evolution of scene are measured
MD & VLSI

• One of the most difficult tasks in VLSI imaging
  – Temporal intensity variations in the image are generally small and tough to determine reliably
  – Chips tend to be complex because of the storage and delay elements required
  – Analog signal processing is significant
Motion Detectors

- Elementary motion detector
- Delay and correlation techniques
- Real-time differentiation
Elementary Motion Detector (EMD)

\[ \text{velocity } \propto \frac{d}{\Delta t} \]
Correlated Motion Detection (CMD)

- At time 1, the outputs from the detectors are thresholded and the 1s or 0s are stored in the latches.
- At time 2, the latched signals are correlated (multiplied) with the new outputs from the sensors.
CMD (Cont.)

• This method works in one direction (LR). Opposite direction (RL) requires another row

• CMD is essentially EMD whereby non-adjacent pixels can contribute to the overall motion

• If the latch is replaced by a certain delay, a motion at *given* speed is enhanced
Temporal Differentiation

- Features
  - Increase, decrease, equal (encoded in 2b)
  - Adjacent pair of 2b outputs has 9 combinations
  - Two measurements in time give 81 combinations
  - 6 patterns of interest are tracked to follow evolution of low-level motion
Temporal Differentiation (Cont.)

- Critical issue: sensitivity of differentiator
  - E.g. simple RC differentiator needs high rate of change for significant output
  - Requires Amp, thus complexity

\[
U_{in} = \frac{U_{out}}{1 + sCR} \approx \frac{1}{CR} \frac{U_{out}}{s} \quad \Rightarrow \quad u_{out} \approx CR \frac{du_{in}}{dt}
\]
Adaptive Photocircuits

- Two modes of operation:
  - Logarithmic compression (for large DR) and long integration time
  - High gain for high frequency variations and sensitive motion detection
Adaptive Photocircuits (Cont.)

- For slowly varying signals, the response of the circuit is determined by the adaptive element
  - If it’s a large resistor, the circuit gives logarithmic compression, with feedback
  - Essentially similar circuits used by Delbrück and Huppertz et al.

- At higher frequencies, the feedback is dominated by cap divider C1 and C2
  - So the gain is higher for rapidly varying signals

- Thus:
  - High sensitivity for motion detection
  - Wide dynamic range
Spatial Processing

• Most used spatial algorithms
  – Neighbor averaging
  – Demosaicing (see lecture on color)
  – Edge detection

• Mammalian focal plane processing
  – Inhibition of adjacent sensors to increase local contrast
  – Edge detection, etc.
Spatial Processing (Cont.)

• Foveated sensor
  – Use non uniform pixels (e.g. IMEC)
• Parallel processing sensor
  – Column parallel processing (e.g. Linköping Univ.)
Silicon Retinas

• Features
  – Analog processing in 2D to approximate Gaussian weighting function (e.g. C. Mead)
  – Each sensor contributes to the signals at a node on the network and its individual output is modified by the signal at that node
Silicon Retinas (Cont.)

• Here, the unity gain buffer sends the sensor output onto the network

• The differential amplifier (or a comparator) senses the node signal (including the sensor’s own contribution) and modifies the final output of the pixel accordingly
  » thus, strong signals from adjacent pixels will inhibit the output
  » but less so if this pixel also has a strong output itself

• The resistors used in such a network are not likely to be made from passive resistors but rather from an active MOSFET circuit
Silicon Retinas (Cont.)

- As summarized in Moini, other implementations include adaptive sensors, or active circuits to emulate the Gaussian function better.

- Typically, each of these circuits has a few tens of pixels and is designed to imitate a particular aspect of animal vision:
  - Animals often display more complex functionality, such as two separate smoothing systems, some of which have also been implemented electronically.

- As yet, there has been no practical, compact 2-D spatial processing architecture.