Quantum perspectives in computing, sensing, communication, and metrology

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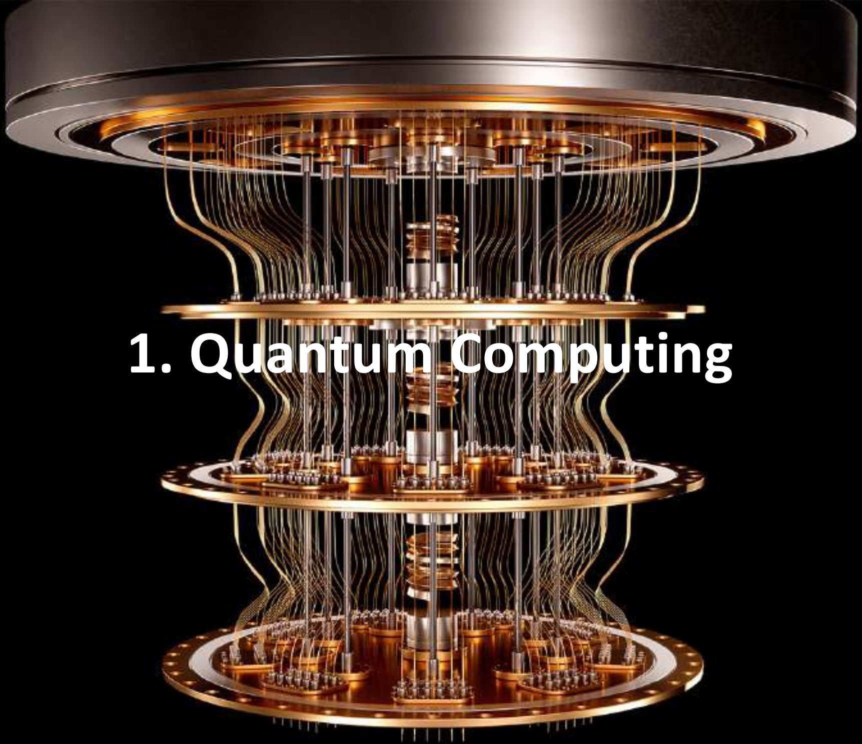
Outline

1. Quantum computing (2 periods)
2. Cryogenic electronics (2 periods)

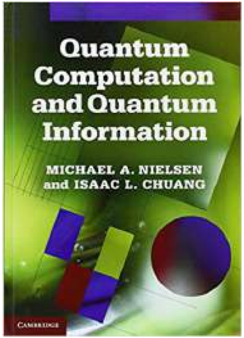
Available in a future class:

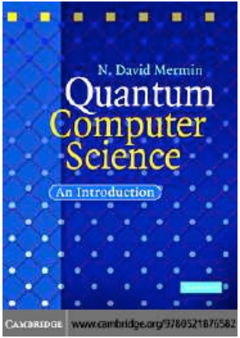
3. Quantum algorithms (2 periods)
4. Quantum imaging and communications (1 period)
5. Quantum metrology (2 periods)



1. Quantum Computing

Suggested Reading





The First Quantum Revolution

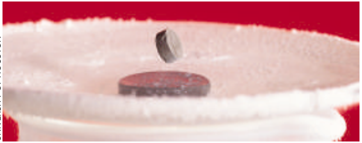
NAMETK Agencytk

1900s | 1910s | 1920s | 1930s | 1940s

Planck Explains Blackbody Radiation (1900)

Einstein Explains Photoelectric Effect (1905)

Discovery of Superconductivity (1911)



TEXAS CENTER FOR SUPERCONDUCTIVITY, UNIVERSITY OF HOUSTON

Bohr's Theory of Atomic Spectra (1913)

Bose-Einstein Condensation Predicted (1924)

Pauli Exclusion Principle (1925)

Schrödinger Equation; Copenhagen Interpretation (1926)

Heisenberg Uncertainty Principle (1927)

Dirac Equation for the Electron (1928)

Anti-Electron Discovered (1932)

Schrödinger's Cat Paper; Einstein-Podolsky-Rosen Paper about Local Realism (1935)

Superfluidity Discovered (1938)

BETTMANN/CORBIS

Atomic Bomb (1945)

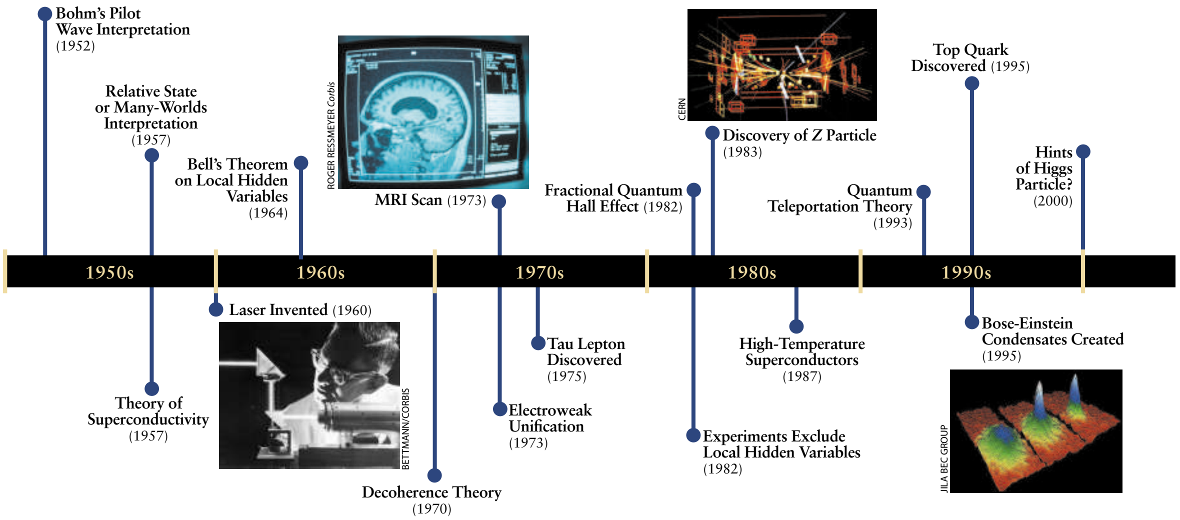
Transistor (1947)

AT&T ARCHIVES

Quantum Electrodynamics and Renormalization (1948)

M. Tegmark & J.A. Wheeler, 2001

The First Quantum Revolution

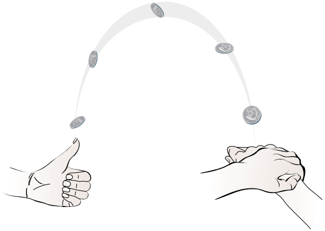


M. Tegmark & J.A. Wheeler, 2001

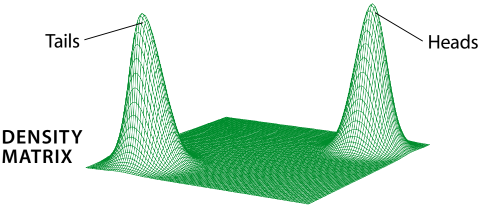
Weird Quantum Properties:
Superposition & Entanglement

Superposition

CLASSICAL UNCERTAINTY

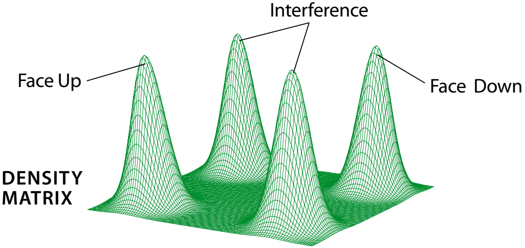


COIN TOSS



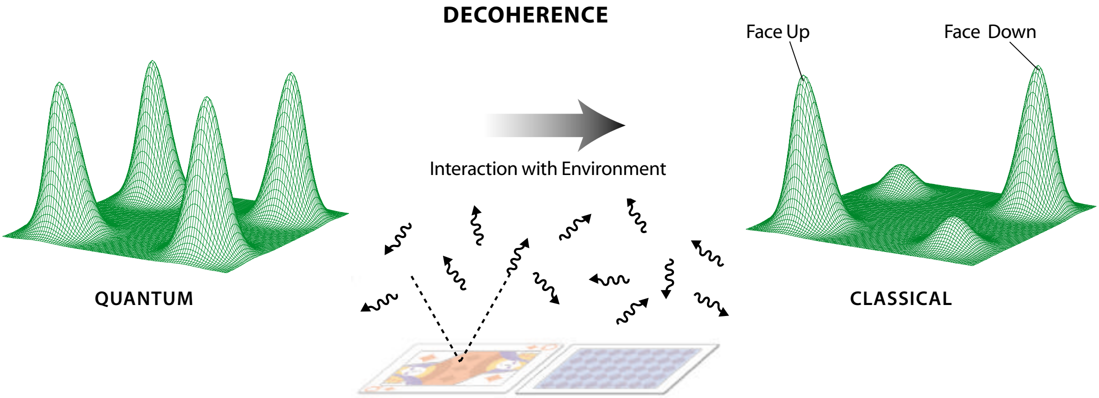
QUANTUM UNCERTAINTY

COHERENT SUPERPOSITION



M. Tegmark & J.A. Wheeler, 2001

Coherence / Decoherence



M. Tegmark & J.A. Wheeler, 2001

Entanglement

Definition: two particles are entangled if the quantum state of one particle cannot be described independently from the quantum state of the other particle.

Intuition: measuring the quantum state of one particle implies knowledge of the quantum state (e.g. momentum, spin, polarization, etc.) of the other entangled particle using the same projection.

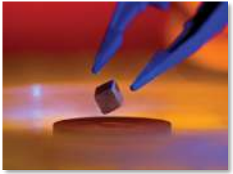
The Second Quantum Revolution

- Spearheaded by many, *in primis* Richard Feynman
- Proposal to use of **entanglement** and **superposition** for computation
- Fundamentals and theory developed in the 1980-2000s

There is plenty of space at the bottom

- Richard Feynman

The Promise of Quantum Computing



Energy

Room-temperature superconductivity

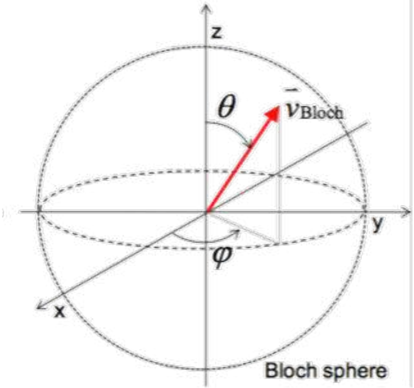
Health

Quantum chemistry

Internet Security

Source: L. Vandersypen, ISSCC 2017

Quantum Bit (Qubit)



$$|\psi\rangle = \alpha_0 |0\rangle + \alpha_1 |1\rangle$$

- Superposition
- Entanglement

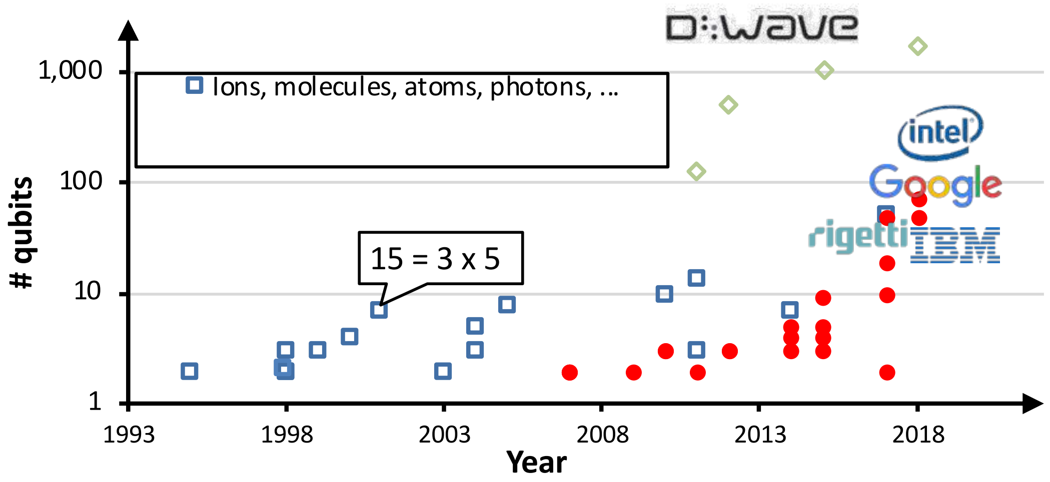
The Power of Superposition

1 qubit...2 states
2 qubits...4 states

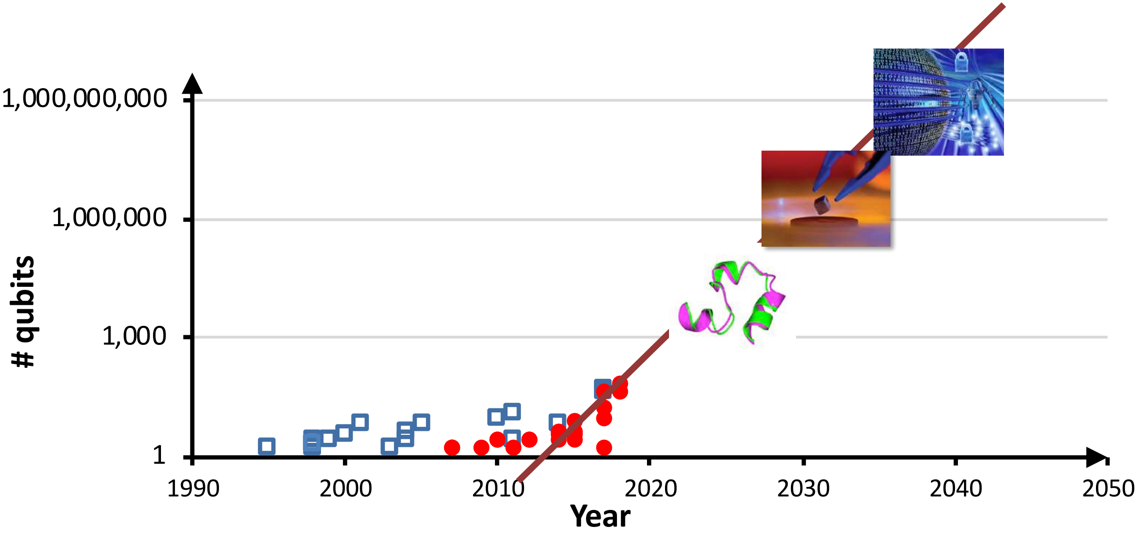
N qubits..2^N states

40 qubits: 10^{12} parallel operations
300 qubits: more than the atoms in the universe

State-of-the-Art



How Far Are We from Something Useful?



Quantum Supremacy or Quantum Advantage

Quantum supremacy is the potential ability of quantum computing devices to solve problems that classical computers practically cannot.

[Wikipedia]

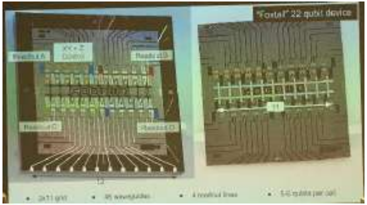
Google claims to have reached quantum supremacy (Financial Times)

Report on a an accepted paper to a peer-reviewed publication

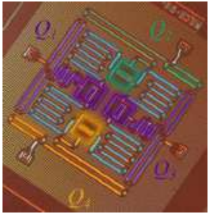
Solid-state Qubit Implementations Today

- Based on superconducting qubits
- First multi-qubit chips announced
- Freely available qubits on line

72-qubit chip announced

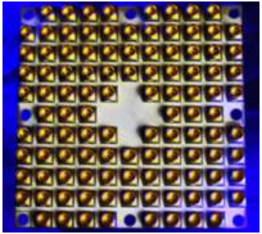


16 Qubits online version

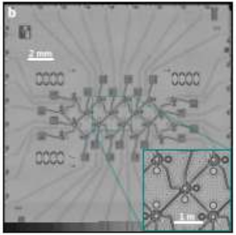


50 qubit chip announced

49 qubit chip

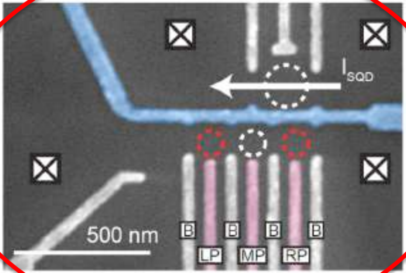


19 qubit chip

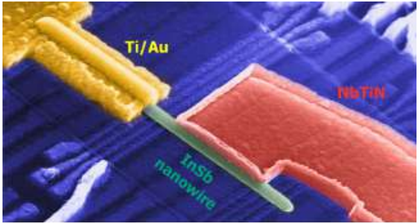


Source: Tristan Meunier

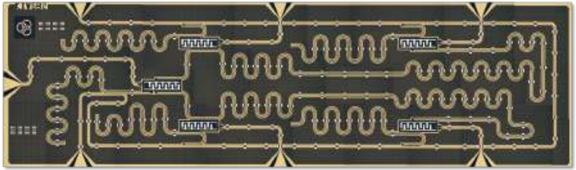
Solid-state Qubit Implementations Today



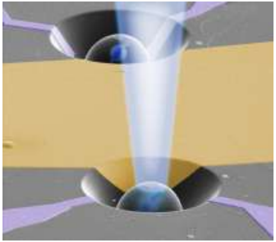
Semiconductor quantum dots



Semiconductor-superconductor hybrids



Superconducting circuits



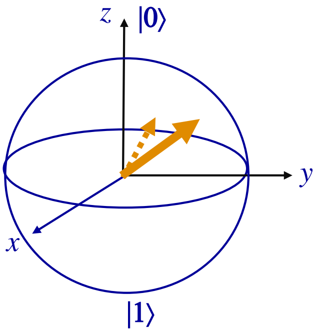
Impurities in diamond or silicon

Source: L. Vandersypen, 2017

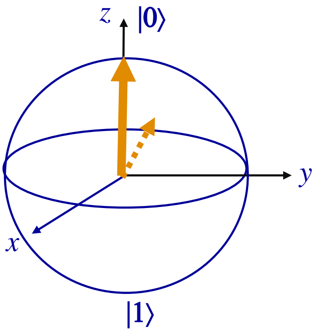
Qubits are Fragile

- Environment can cause decoherence due to dephasing and relaxation
- Fidelity

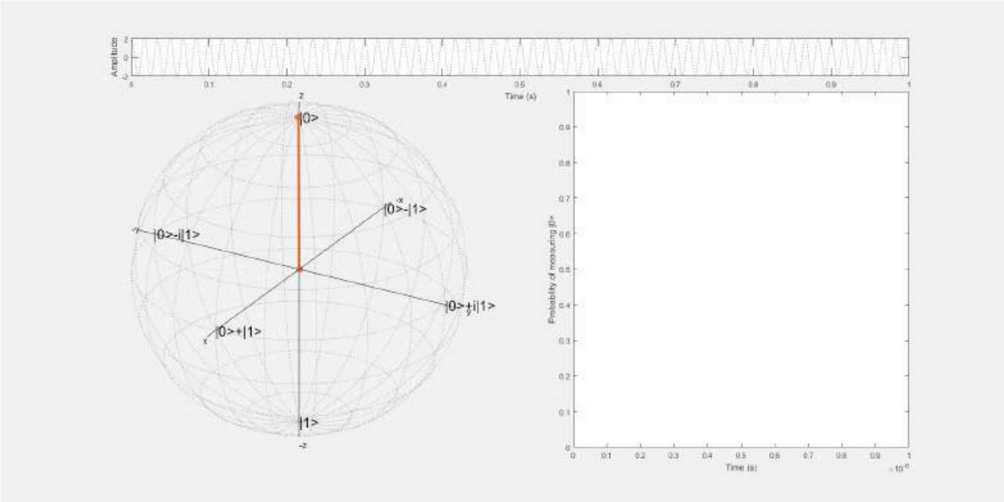
Dephasing



Relaxation



Qubit Transition from |0> to |1>



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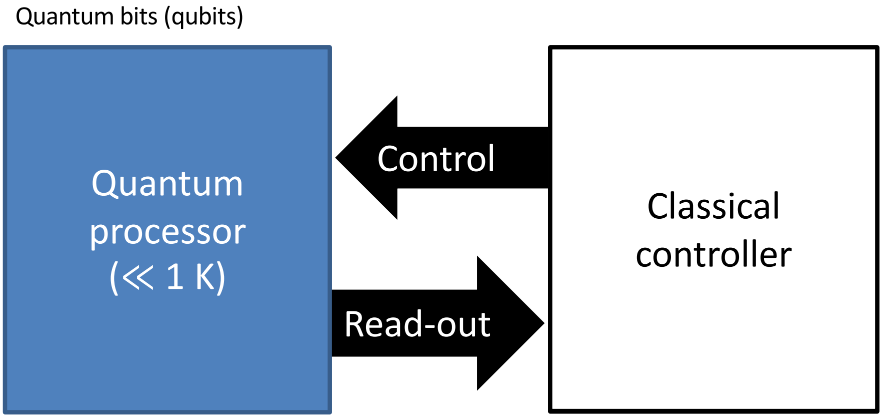
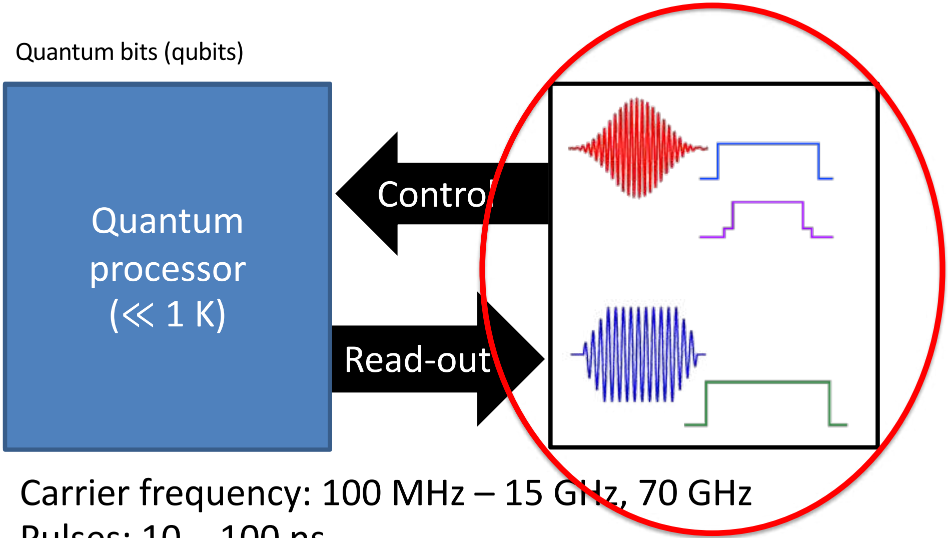
Interfacing Qubits with Classical World



- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns

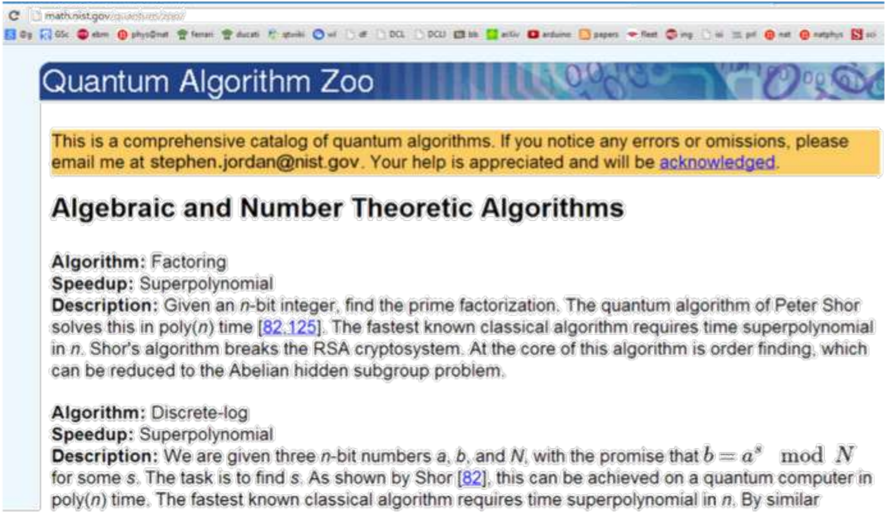
Interfacing Qubits with Classical World



- Carrier frequency: 100 MHz – 15 GHz, 70 GHz
- Pulses: 10 – 100 ns
- Readout techniques for spin qubits: **ESR, EDSR**

ESR: Electron spin resonance – EDSR: Electric dipole spin resonance

Status of Quantum Algorithms



math.nist.gov

Quantum Algorithm Zoo

This is a comprehensive catalog of quantum algorithms. If you notice any errors or omissions, please email me at stephen.jordan@nist.gov. Your help is appreciated and will be acknowledged.

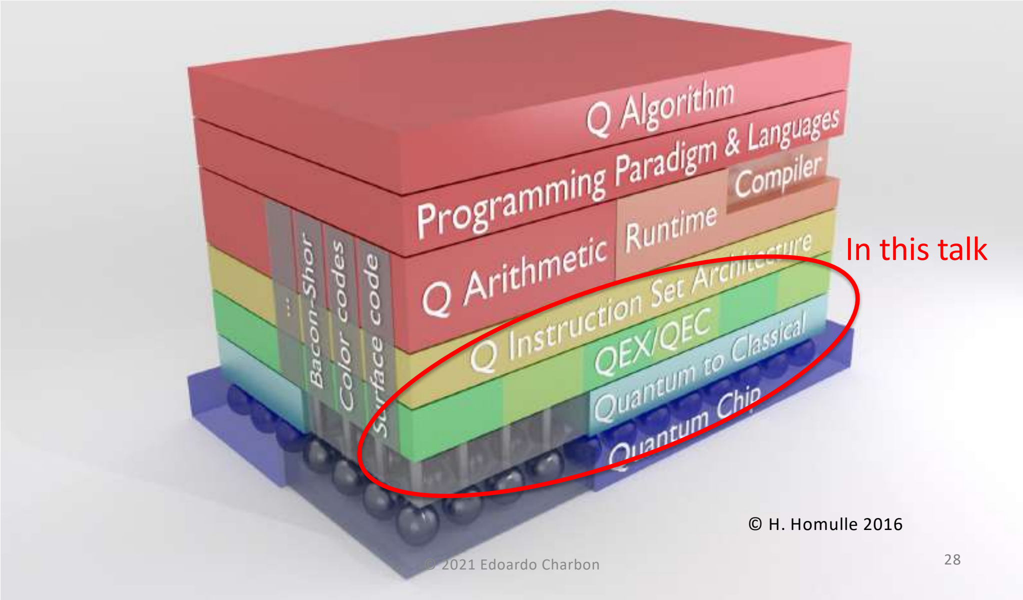
Algebraic and Number Theoretic Algorithms

Algorithm: Factoring
Speedup: Superpolynomial
Description: Given an n-bit integer, find the prime factorization. The quantum algorithm of Peter Shor solves this in poly(n) time [82,125]. The fastest known classical algorithm requires time superpolynomial in n. Shor's algorithm breaks the RSA cryptosystem. At the core of this algorithm is order finding, which can be reduced to the Abelian hidden subgroup problem.

Algorithm: Discrete-log
Speedup: Superpolynomial
Description: We are given three n-bit numbers a, b, and N, with the promise that $b = a^s \mod N$ for some s. The task is to find s. As shown by Shor [82], this can be achieved on a quantum computer in poly(n) time. The fastest known classical algorithm requires time superpolynomial in n. By similar

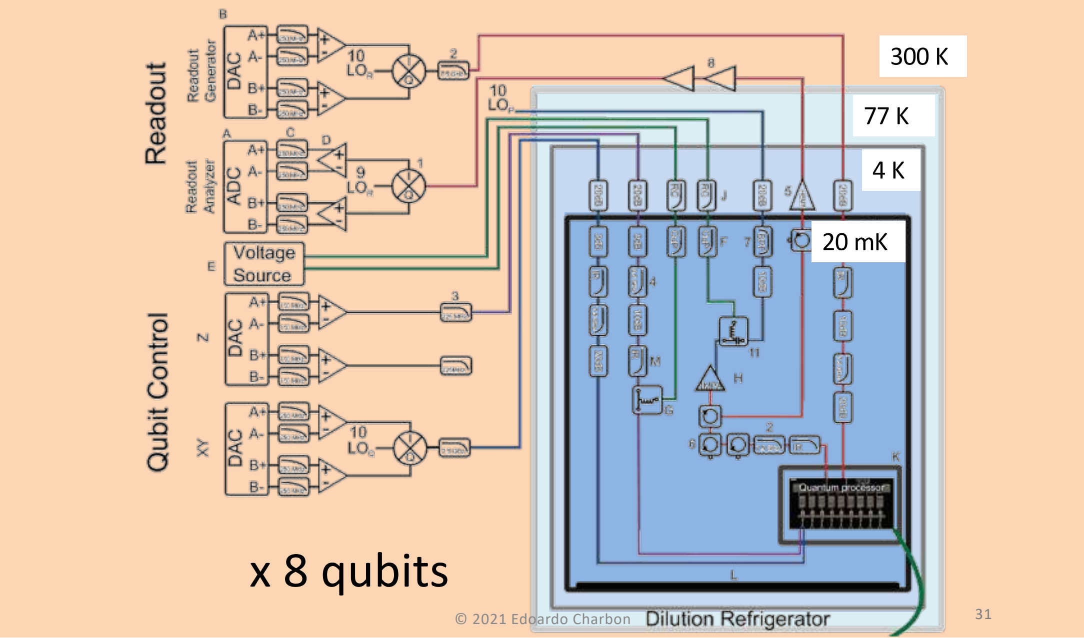
~50 algorithms with quantum speedup, but most people know 2.

Quantum Computing Stack



Quantum Computer Architecture

A Real-life Quantum Computer



x 8 qubits

Today's Solution

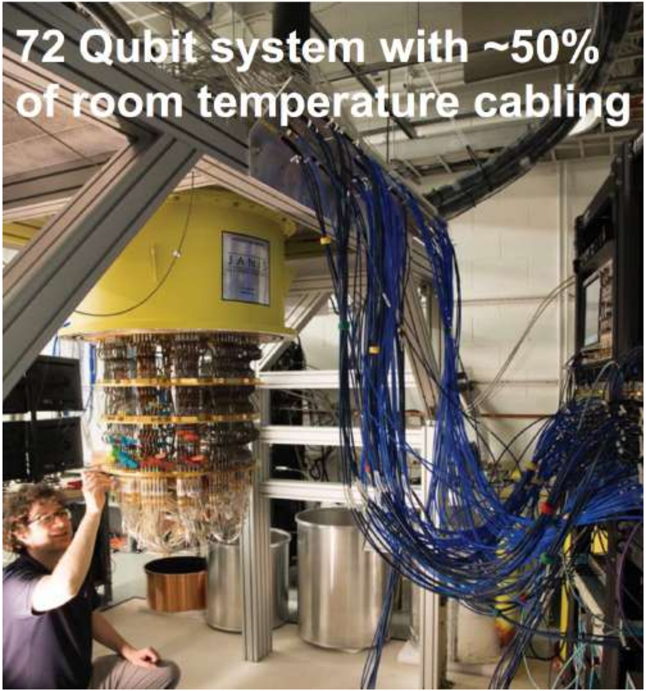
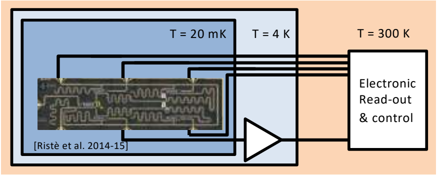
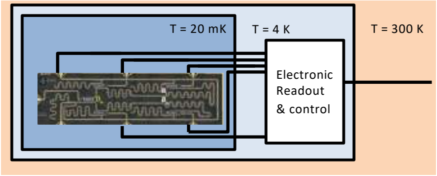


Image: Google Bristlecone. Taken from: J.C. Bardin et al., *"An Introduction to Quantum Computing for RFIC Engineers"* , RFIC Symposium 2019

Our Proposed Solution

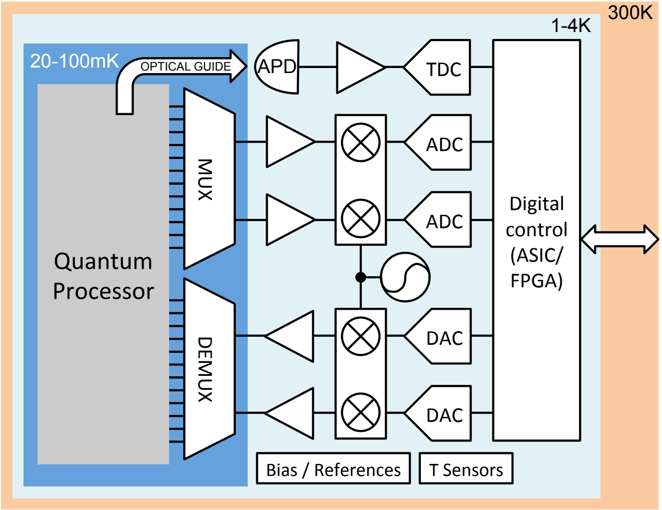
- **Proposed solution**
  - Electronics at 4 K
  - Only connections to 4 K to 20 mK are needed





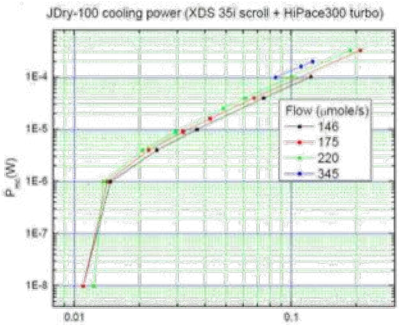
- **Ultimate solution**
  - Qubits at 4 K
  - Monolithic integration

Electronic Readout & Control

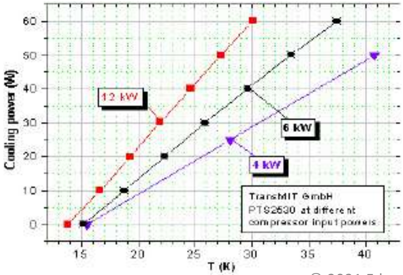


E. Charbon *et al.*, *IEDM* 2016

Cooling Power Issue



T(K)



Dilution refrigerator

300 K

70 K

4 K

100 mK

20 mK

Courtesy: Oxford instruments

Scalability Issue

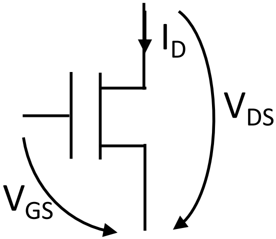
- Noise budget……………………………………………< 0.1nV/√Hz
- Power budget (for scalability)………………… << 2mW/qubit
- Physical dimensions (for scalability)……… 30nm
- Bandwidth (for multiplexing)………………… 1-12GHz
- Kick-back avoidance

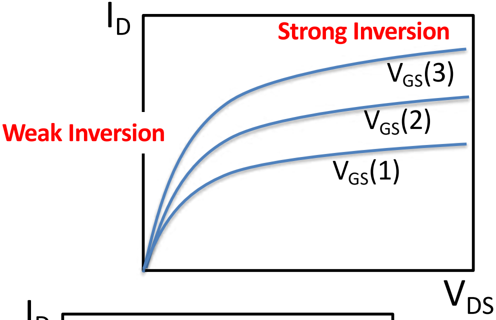
2. Cryogenic Electronics

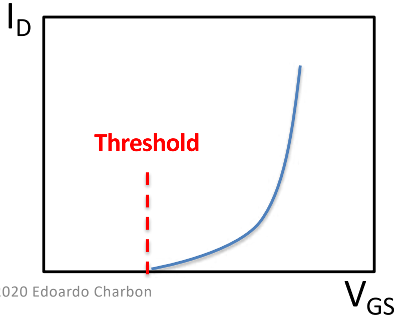
Transistor Modeling at Deep Cryogenic Temperatures

CMOS Modeling: Important Parameters

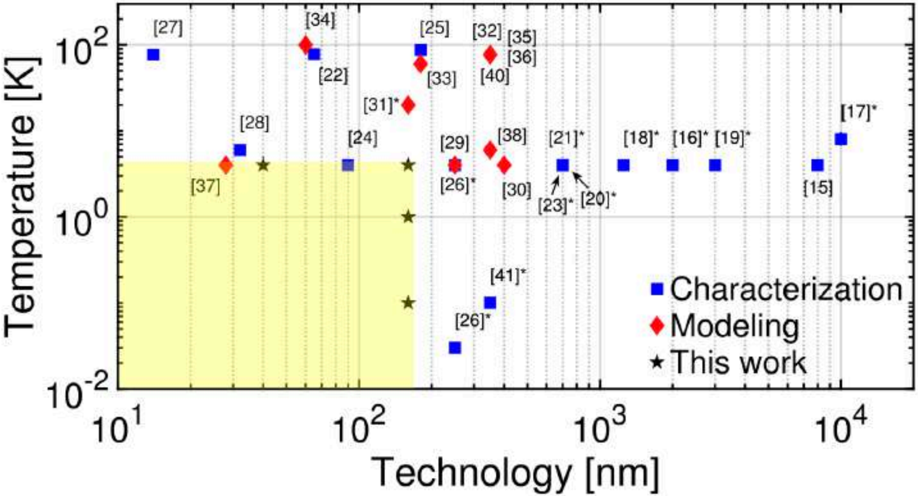
- MOSFET







CMOS Modeling: History



R.M. Incandela et al., *ESSDERC* 2017
R.M. Incandela et al., *J. of EDS 2018*

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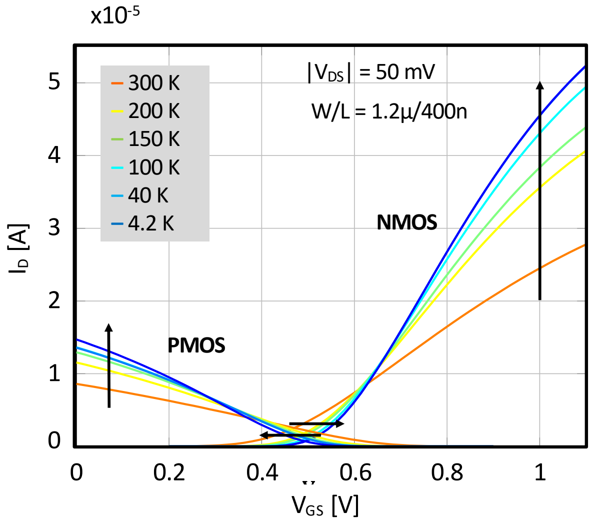
R.M. Incandela et al., *J. of EDS 2018*

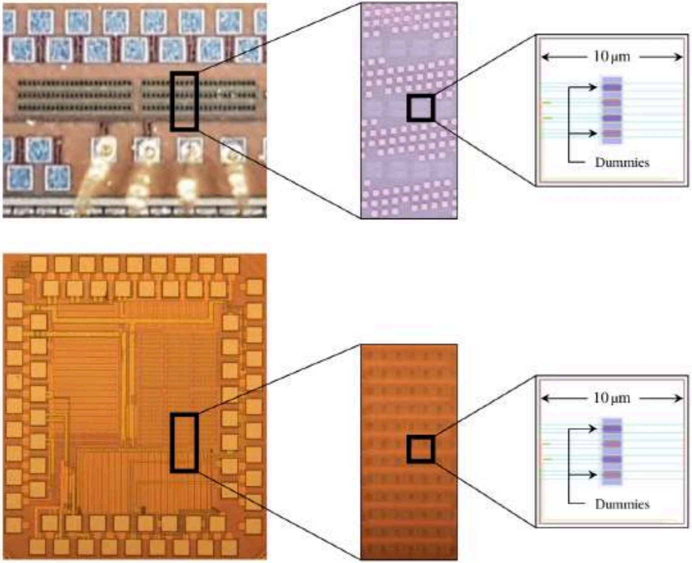
What Happens to CMOS at Cryo?

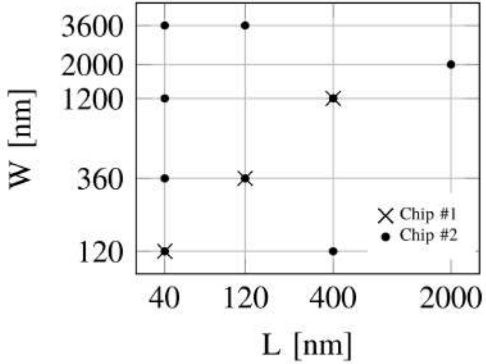


- Threshold voltage increases significantly
- A current kink may appear
- Mismatch in passives and actives is more prominent
- The substrate becomes practically floating
- *The SS is higher but it saturates around 1K*
- Leakage drastically reduces

R.M. Incandela et al., *ESSDERC* 2017
R.M. Incandela et al., *J. of EDS 2018*

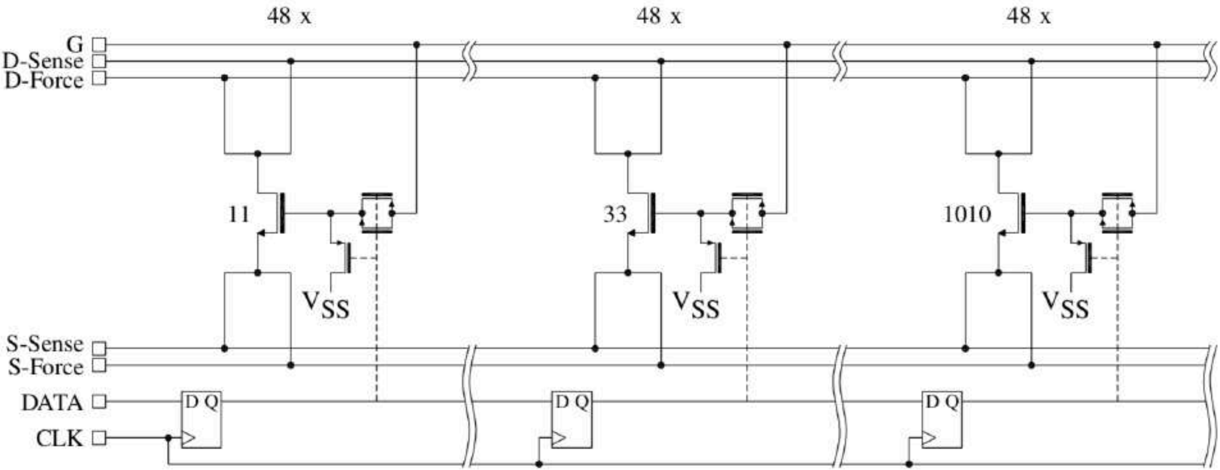
How to Characterize MOS Transistors?





P. ‘t Hart et al., *J. EDS* 2020

CMOS Characterization in Practice



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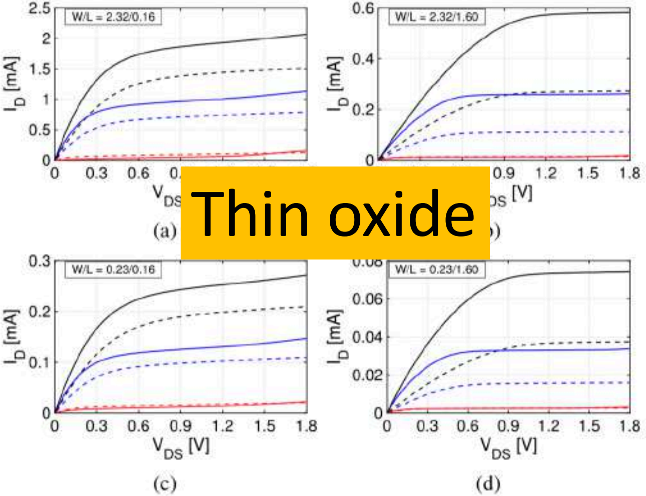
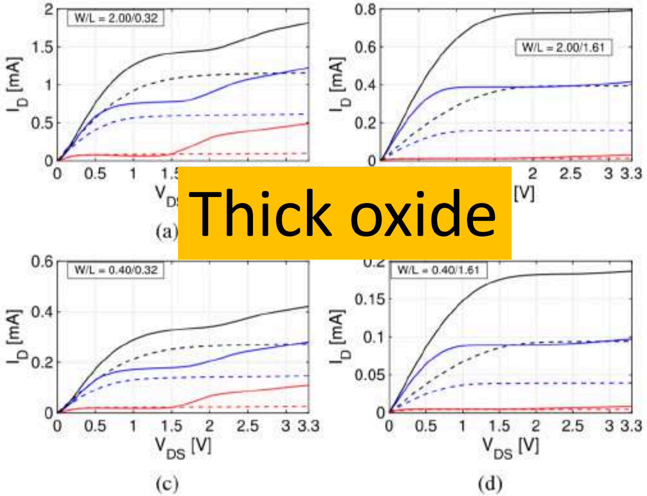
I_D-V_{DS} Characterization (0.16µm)



V_{GS} = [0.68 V; 1.24 V; 1.8 V]. Solid line: 4 K; dashed line: 300 K.



V_{GS} = [1.05 V; 2.17 V; 3.3 V]. Solid line: 4 K; dashed line: 300 K.

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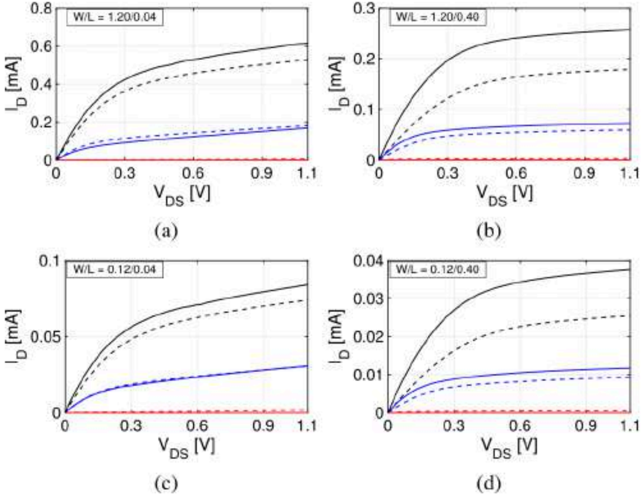
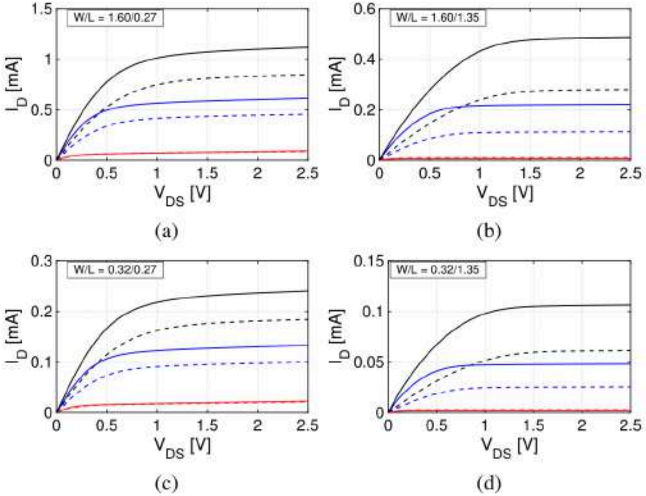
I_D-V_{DS} Characterization (40nm)



V_{GS} = [0.43 V; 0.76 V; 1.1 V]. Solid line: 4 K; dashed line: 300 K.



V_{GS} = [0.85 V; 1.68 V; 2.5 V]. Solid line: 4 K; dashed line: 300 K.

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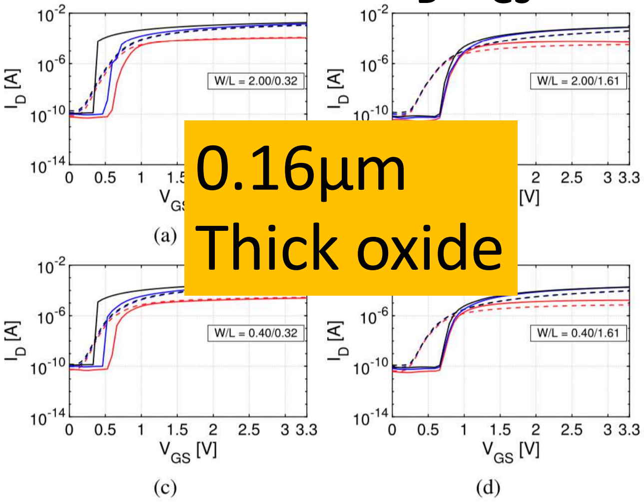
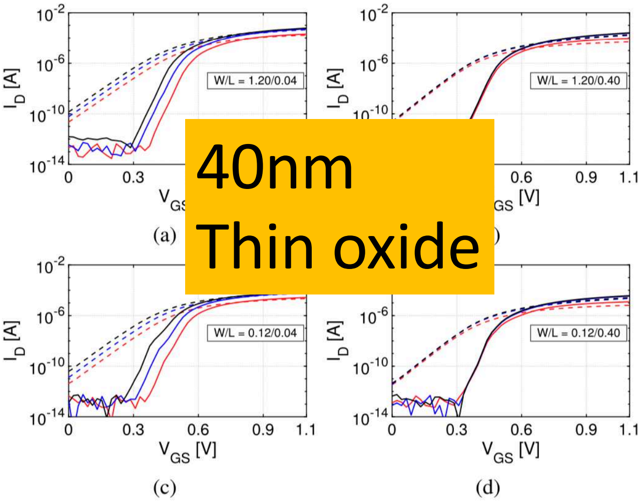
I_D-V_{GS} Characterization



V_{DS} = [0.1 V; 1.7 V; 3.3 V]. Solid line: 4 K; dashed line: 300 K.



V_{DS} = [0.1 V; 0.6 V; 1.1 V]. Solid line: 4 K; dashed line: 300 K.

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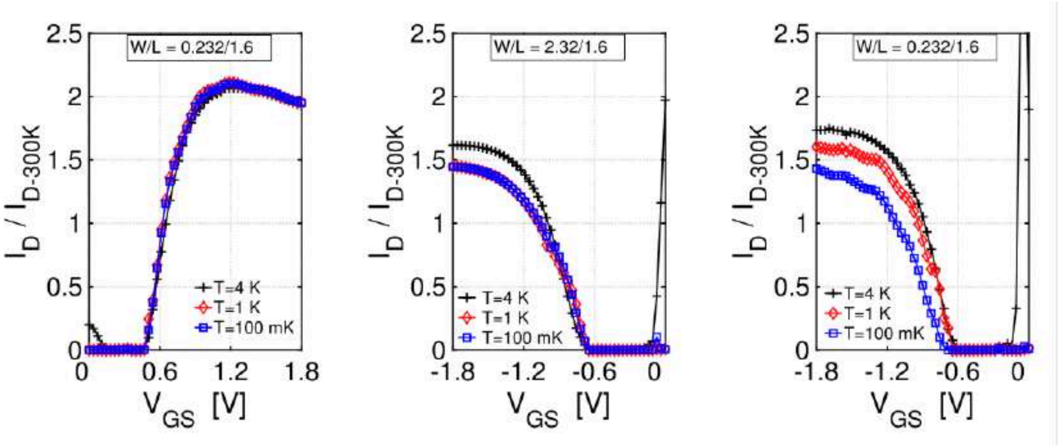
I_D-V_{GS} Characterization in Sub-K Regimes



NMOS
VDS = 1.8V

PMOS
VDS = -1.8V

PMOS
VDS = -1.8V

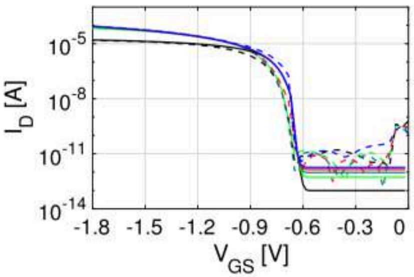
R.M. Incandela et al., *J. of EDS 2018*

CMOS Modeling

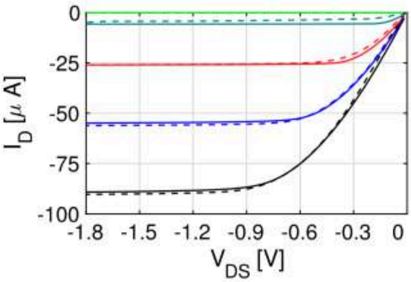
MOS11 parameters for 0.16-μm CMOS					
BETSQR	VFBR	THESRR	SDIBLO	ALPR	KOR
THESATR	THERR	A1R	A2R	A3R	
PSP parameters for 40-nm CMOS					
FACTUO	DELVTO	THEMUO	THESATO	RSW1	CFL
ALPL	MUEO	FBET1			

Model

Measurement

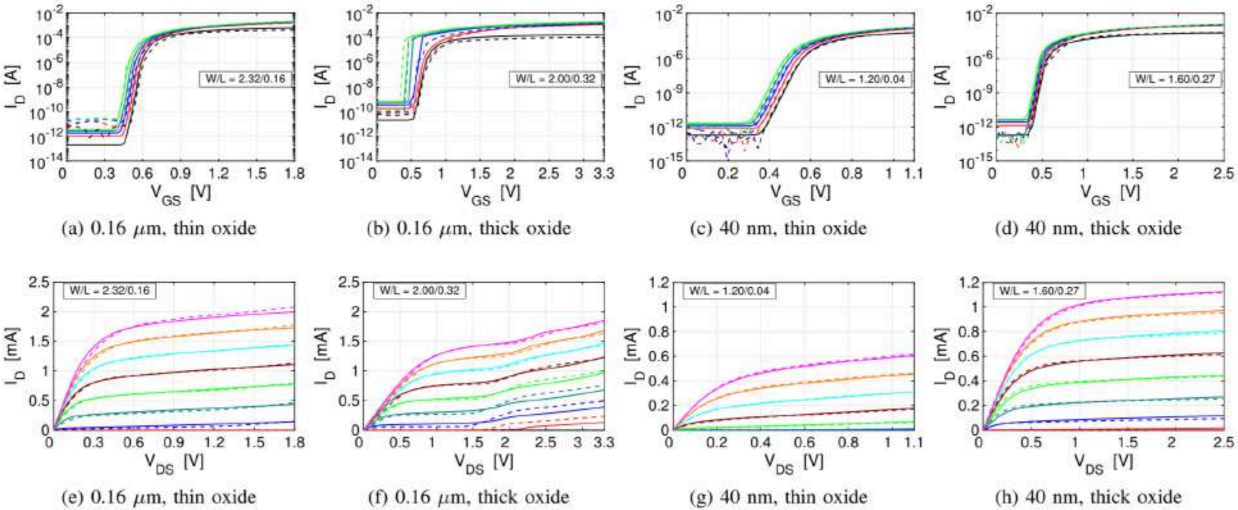


Thin oxide PMOS
V_{DS} = -1.8 – -0.09V



Thin oxide PMOS
V_{GS} = -1.3 – -1.8V

CMOS Modeling



(a) 0.16 μm, thin oxide (b) 0.16 μm, thick oxide (c) 40 nm, thin oxide (d) 40 nm, thick oxide

(e) 0.16 μm, thin oxide (f) 0.16 μm, thick oxide (g) 40 nm, thin oxide (h) 40 nm, thick oxide

Sub-threshold Slope (SS)

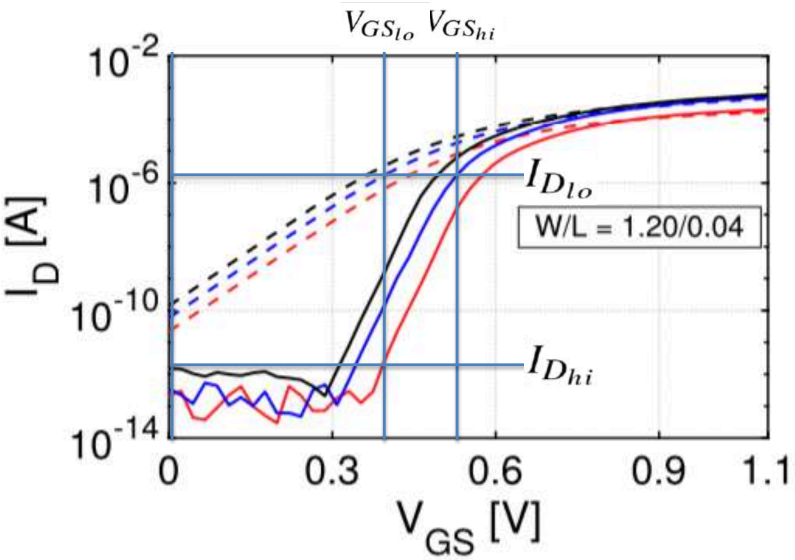
$$SS = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{ox}}\right)$$

C_d = depletion layer capacitance
C_{ox} = gate oxide capacitance

$$SS = \ln(10)\frac{kT}{q} \sim 60\text{mV/dec}$$

$C_d = 0$; $C_{ox} \rightarrow$: thermionic limit

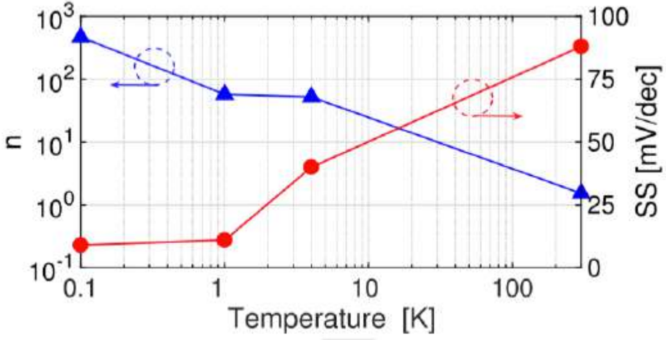
Sub-threshold Slope Characterization(SS)



$$SS^{-1} = \frac{|\log\left(I_{D_{hi}}/I_{D_{lo}}\right)|}{V_{GS_{hi}} - V_{GS_{lo}}}$$

Sub-threshold Slope (SS)

PMOS W/L = 2.32μm / 1.6μm



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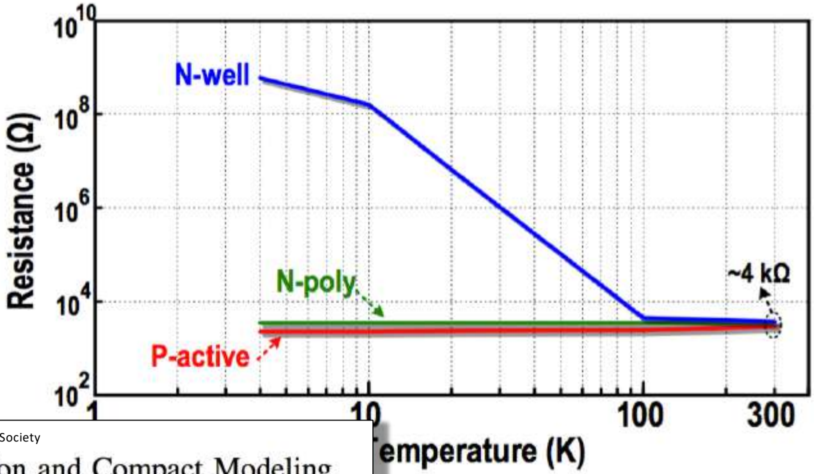
R.M. Incandela et al., *J. of EDS 2018*

Substrate Resistivity



IEEE Journal of the Electron Device Society

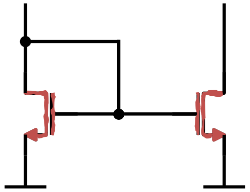
Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures

Rosario M. Incandela, *Student, IEEE,* Lin Song, Harald Homulle, Edoardo Charbon, *Fellow, IEEE,* Andrei Vladimirescu, *Fellow, IEEE,* and Fabio Sebastiano, *Senior Member, IEEE*

ra et al., *JSSC* 2018

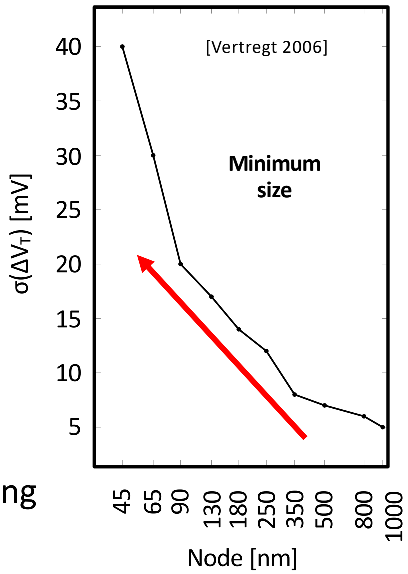
Mismatch Modeling at Cryo

Subthreshold Current Mismatch: Why Do We Care?



- Impacts performance of:
  - ADC/DAC
  - Differential pairs
  - SRAM

- Worsens with technology scaling



Subthreshold Current Model

$$\boxed{I_D = I_0 e^{(V_{GS}-V_{TH})/SS}}$$

Taylor expansion is impractical at cryo due to the instability of ID and the exponential nature of it.

Solve wrt $\log(I_D)$

$$\boxed{\log(I_D) \propto \frac{1}{\ln(10)} \frac{V_{GS}-V_{TH}}{SS}.}$$

Taylor expansion on V_{TH} and SS

$$\boxed{\Delta \log(I_D) = \frac{1}{\ln(10)} \left(-\frac{1}{SS} \Delta V_{TH} - \frac{(V_{GS}-V_{TH})}{SS} \frac{\Delta SS}{SS} \right)}$$

Subthreshold Current Model

$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\left(\frac{\sigma_{\Delta V_{TH}}}{\overline{SS}}\right)^2 + \left(\frac{V_{GS}-V_{TH}}{\overline{SS}}\frac{\sigma_{\Delta SS}}{\overline{SS}}\right)^2 + 2\frac{(V_{GS}-V_{TH})}{\overline{SS}^3}\sigma_{\Delta V_{TH}}\sigma_{\Delta SS}\rho_{\Delta V_{TH},\Delta SS}\right]. \quad (5)$$

The correlation factor ρ between V_{TH} and SS is generally negligible at 300K, 100K, and also at cryogenic temperatures.

Croon Model

$$\sigma^2_{\Delta I_D/I_D} = \ln(10)^2 \sigma^2_{\Delta \log I_D}$$

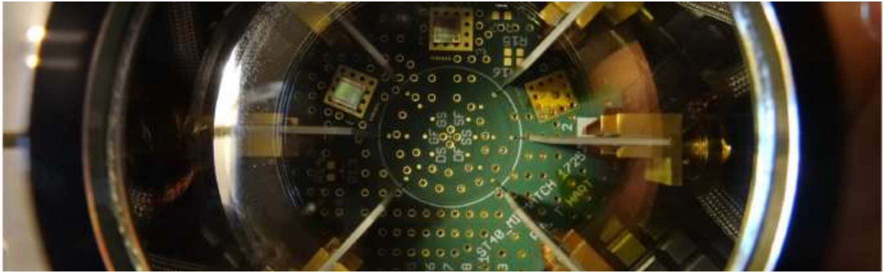
$$\sigma^2_{\Delta \log I_D} = \frac{1}{\ln(10)^2}\left[\sigma^2_{\Delta\beta/\beta} + \left(\frac{\bar{g}_m}{\bar{I}_D}\right)^2 \sigma^2_{\Delta V_{TH}}\right], \qquad (7)$$

Pelgrom Scaling Law

$$\sigma_{\Delta V_{TH}} = \frac{A_{VT}}{\sqrt{WL}} \qquad \sigma_{\Delta\beta/\beta} = \frac{A_{\beta}}{\sqrt{WL}} \qquad \sigma_{\Delta SS/SS} = \frac{A_{SS}}{\sqrt{WL}}$$

A_{VT} : area scaling parameter for V_{T}
A_{β} : area scaling parameter for β
A_{SS} : area scaling parameter for SS
W, L: transistor geometry parameters

How to Characterize Mismatch?



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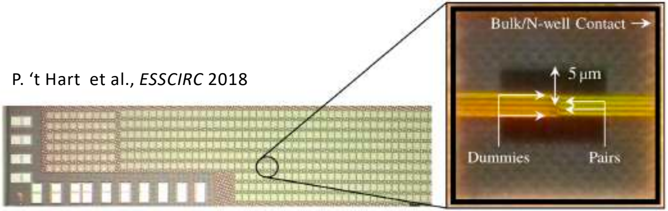
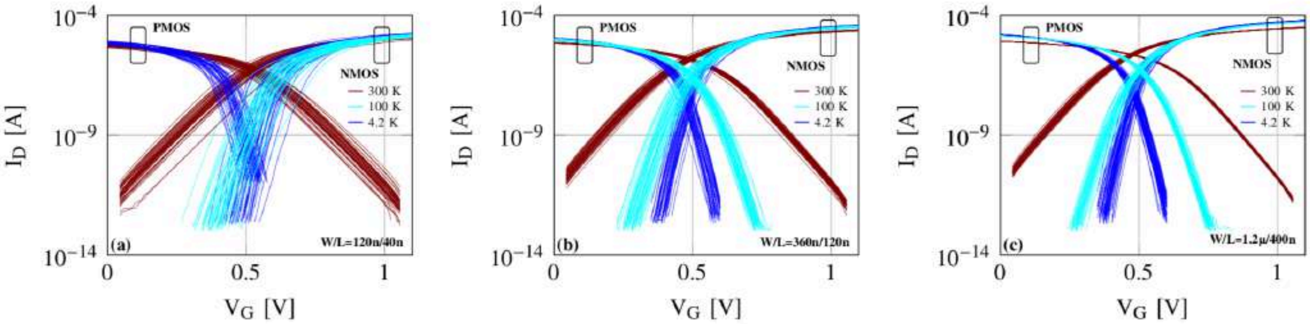


Fig. 1. Die micrograph (*left*) with close-up of a W/L = 1.2 μm/0.4 μm matched pair (*right*).

Mismatch Measurements



48 devices tested
$|V_{DS}|$ = 50mV, V_S=0V (NMOS)
$|V_{DS}|$ = 50mV, V_S=1.1V (PMOS)

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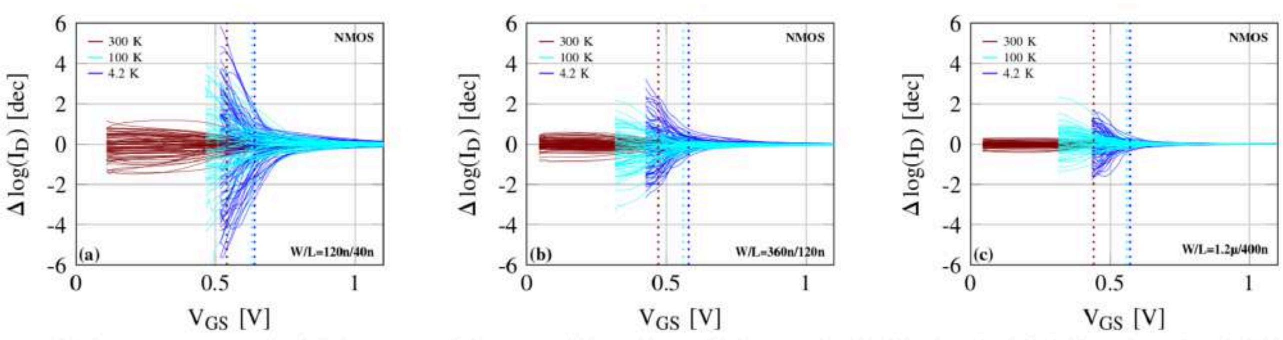
Mismatch Measurements (2)



72 device pairs tested
V_{TH} in dashed lines
$|V_{DS}|$ = 50mV

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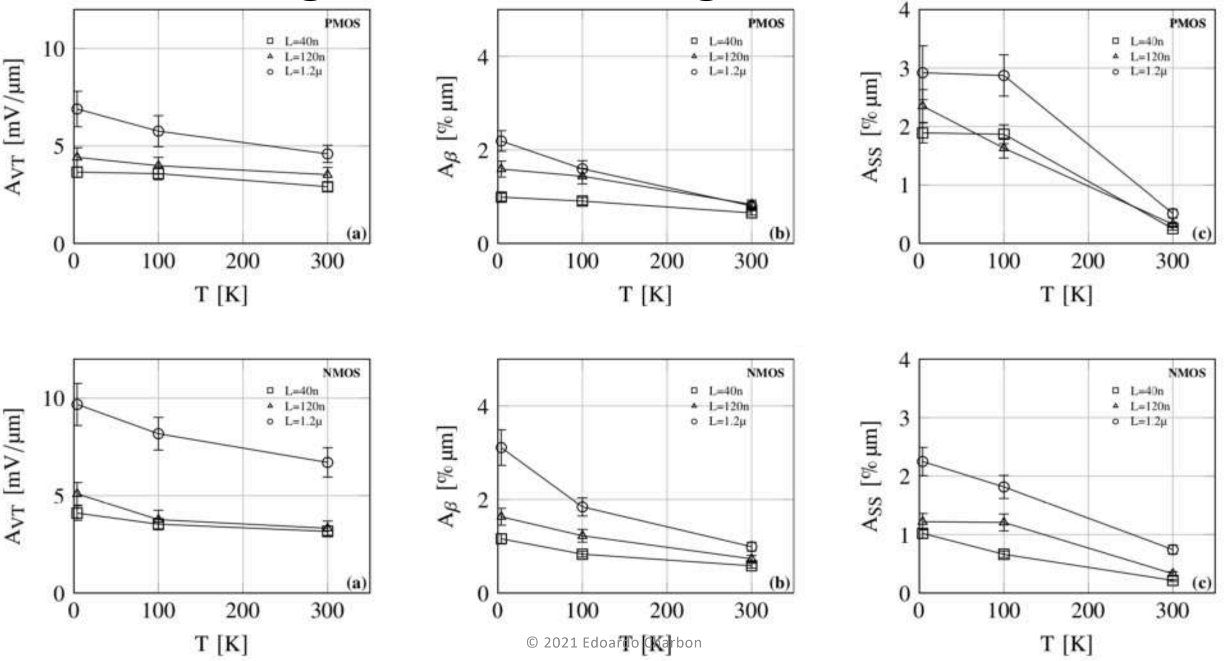
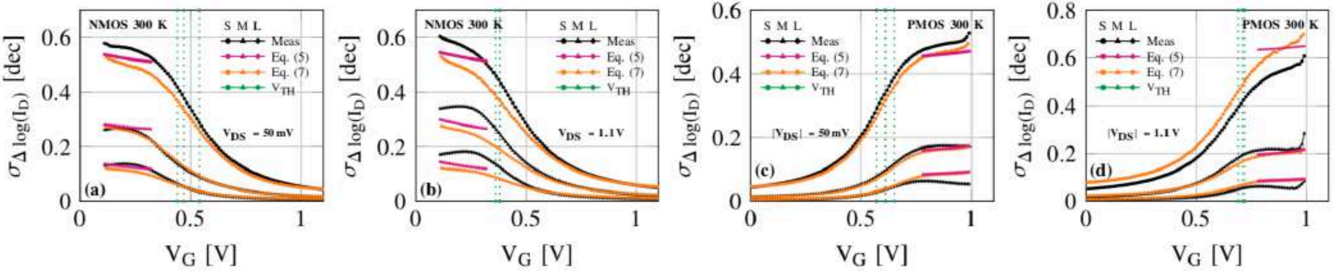
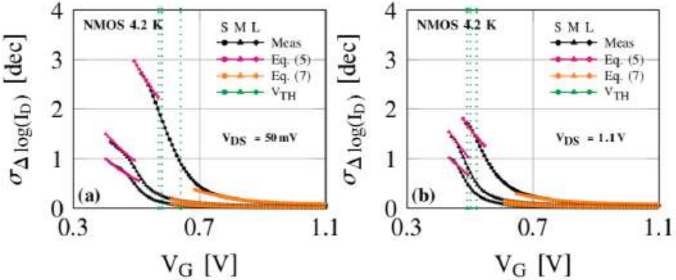
Pelgrom Area Scaling Parameters



Mismatch Modeling





S: W/L = 120nm/40nm
M: W/L = 360nm/120nm
L: W/L=1.2µm/400nm
VS = 0V (NMOS)
VS = 1.1V (PMOS)

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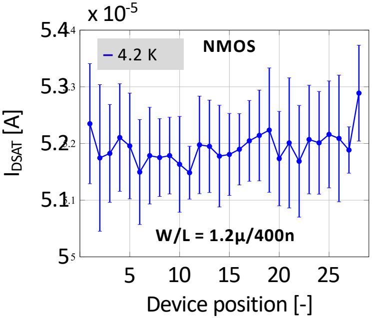
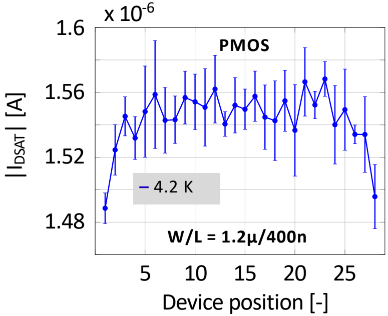
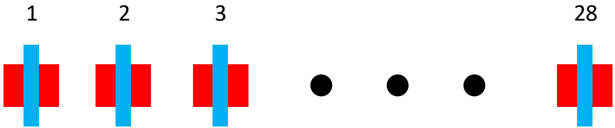
Position Dependence







Summary on Threshold Mismatch

- Cryo-CMOS: mismatch follows Pelgrom and Croon models
- Fixed V_{GS} biasing ➞ matching deteriorates up to 10x
- Fixed G_m/I_D biasing ➞ matching deteriorates “only” 1.1x

Digital Modeling at Cryo

Lowerbound in Digital Design

$$V_{DD,min} \approx 2\frac{kT}{q}\ln(2) = 36\text{mV}$$

CMOS circuits operate in subthreshold wherever this equation holds

$$I_{DS} = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{TH}}{n v_t}} \left(1 - e^{-\frac{V_{DS}}{v_t}}\right);\ I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)v_t^2,$$

n is the sub-threshold slope (SS) factor and $v_t = kT/q$,

The net effect in sub-threshold regimes is a decrease of leakage currents by orders of magnitude, implying a significant increase in the I_{ON}/I_{OFF} ratio

Lowerbound in Digital Design

Assuming an ideal SS factor $n = 1$, at 4.2 K, according to well established room temperature models, one could theoretically achieve $V_{DD,min} \approx 2\ln(2)v_t = 0.48\text{mV}$.

However, at 4.2 K the consensus is that *n≈34.9*. Thus, this fundamental limit is actually *VDD,min*≈ 2.47mV. Additional non-idealities include reverse short-channel effect (RSCE) and inverse narrow-width effect (INWE).

Both effects substantially modulate the threshold voltage.

Latchup

Latch-up has been found to be unpredictable in deep-cryogenic operation. Latch-up immunity typically improves at temperatures lower than RT, thanks to lower well and substrate resistance and to higher base-emitter voltages and lower current gain of parasitic bipolar transistors. However, shallow level impact ionization (SLII), a mechanism for carrier generation, emerges below 50 K

Recommendations

A) create extensive substrate contacts and well-taps, so as to minimize the chance of latch-up at 4.2 K;

B) resize the transistors, so as to reduce INWE and thus maximize V_{TH} modulation;

C) add secondary power rails to enable forward back-biasing, so as to compensate for an increase of V_{TH} at 4.2, in addition use low-V_{TH} transistors;

D) minimize the length of transistors (in contrast to conventional RT sub-threshold standard cell design, where the opposite is generally done);

E) when useful, make the layout aware of mismatch by increasing the overall height of the cells.

Summary of Issues 300K –> 0.1K

- Threshold voltage increases significantly
- A current kink may appear
- Mismatch in passives and actives is more prominent
- The substrate becomes practically floating
- The SS is higher but it saturates around 1K
- Leakage drastically reduces

Trends and Predictions

- How will devices perform in 5 years at 77K?
- How will FinFETs/nanowire FET behave at 77K (Lg<20nm)
- Will ballistic transport affect these devices?
- How different will optimization be at 77K?
- Is there a way to decrease V_T?

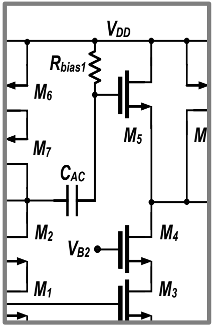
High-Level Modeling at Cryo

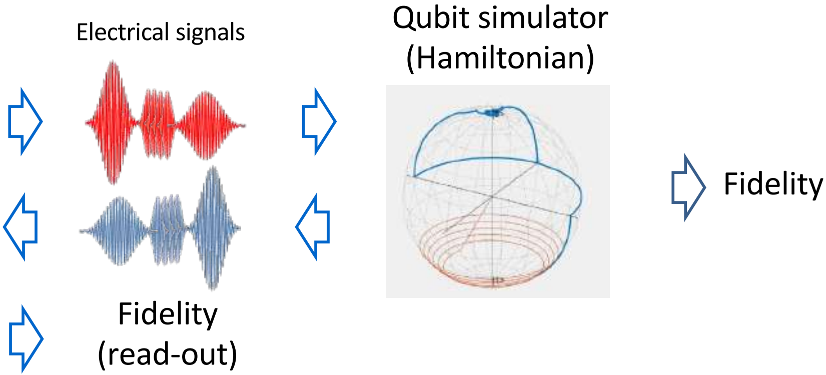
High-Level Modeling: SPINE (SPIN Emulator)

Objectives:

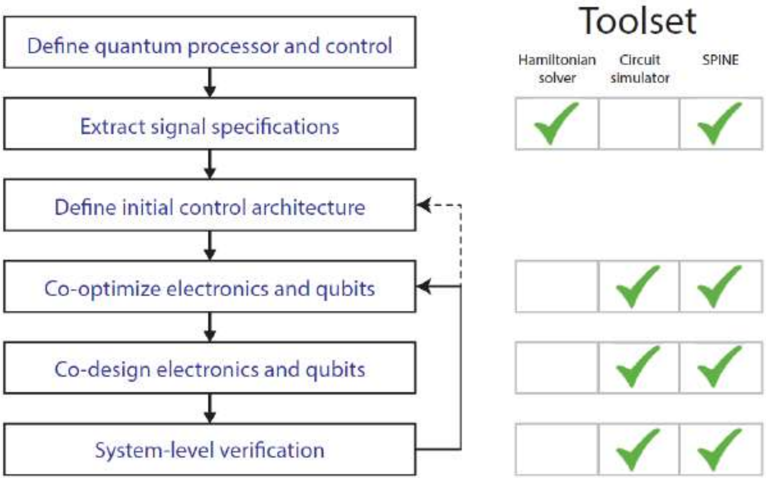
- Enable co-design qubit/electronics
- Derive specifications for Horse Ridge and other components
- Minimize power to achieve wanted fidelity

Circuit simulator





SPINE



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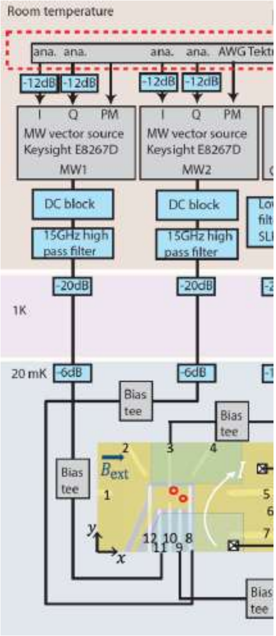
SPINE

- Microwave Carrier: **Keysight E8267D**
  - 22.4 kHz resolution 1 mHz
  - $\mathcal{L}$ (1 MHz) = -106 dBc/Hz >15 dB better
  - S_n = 7.12 nV/√Hz 63 nV/√Hz

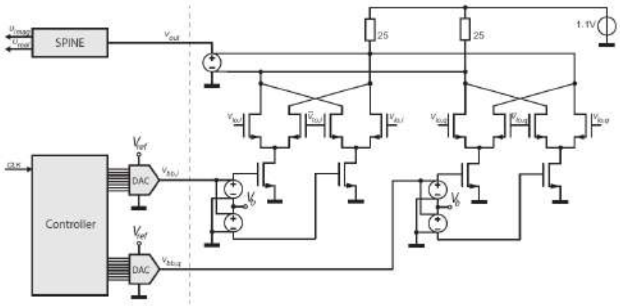
    → > 20 dB attenuation

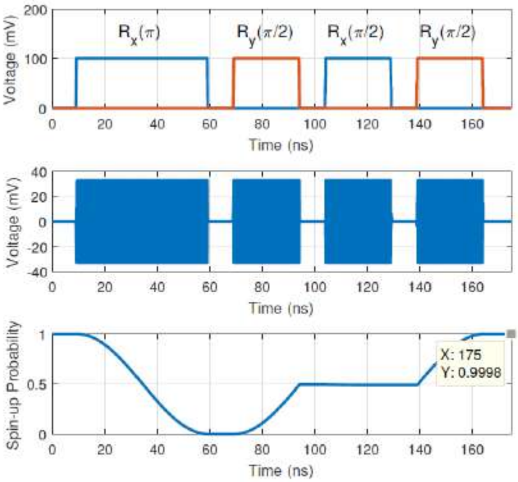
- Microwave Envelope: **Tektronix 5014C**
  - 8-bit resolution 14-bit
  - 140 MS/s 1.2 GS/s
  - 3.56 ns_{rms} 5.0 ps_{rms}
  - 40 dB SNR better

With SPINE we checked that these specs are enough



SPINE





- Example of full simulation:
  - Sequence of rotations
  - Resulting RF signals
  - Qubit response, in terms of spin-up probability
- This involves spin emulation, M/S simulation, RF simulation

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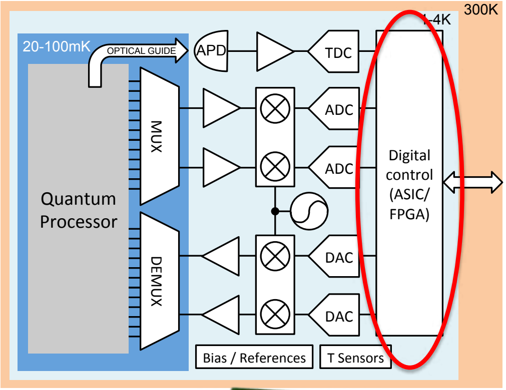
Cryogenic Reconfigurable Hardware

Cryo-FPGAs


300K
4K
20-100mK
OPTICAL GUIDE
APD
TDC
ADC
ADC
DAC
DAC
MUX
DEMUX
Quantum
Processor
Digital
control
(ASIC/
FPGA)
Bias / References
T Sensors


CLK_P
CLK_N
ARTIX-7
XTAL
NPTH
P10
SIG_ADC
CryoFPGA v1.0
FPGA

Cryo-FPGAs

CryoCMOS Hardware Technology
A Classical Infrastructure for a Scalable Quantum Computer

ACM Frontiers in Computing, Como 2016

Harald Homulle[1], Stefan Visser[1], Bishnu Patra[1], Giorgio Ferrari[2], Enrico Prati[3], Carmen G. Almudéver[1], Koen Bertels[1], Fabio Sebastiano[1], Edoardo Charbon[1]

[1]QuTech, Delft University of Technology, Delft, The Netherlands

[2]Politecnico di Milano, Milano, Italy, [3]Consiglio Nazionale delle Ricerche, Milano, Italy

{h.a.r.homulle, f.sebastiano, e.charbon}@tudelft.nl

FPGA functionality

- All FPGA components are working in the cryogenic environment down to 4K
- No modifications required

Component	Functional	Behavior
IOs	✓	
LVDS	✓	
LUTs	✓	Delay change < 5%
CARRY4	✓	Delay change < 2%
BRAM	✓	No corruption (800 kB)
MMCM	✓	Jitter reduction of roughly 20%
PLL	✓	Jitter reduction of roughly 20%
IDELAYE2	✓	Delay change of up to 30%
DSP48E1	✓	No corruption over 400 operations

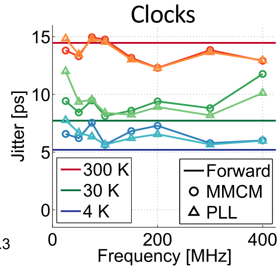
FPGA Performance

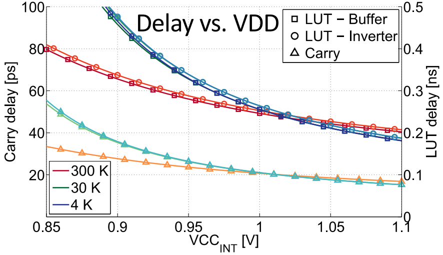
Specs:

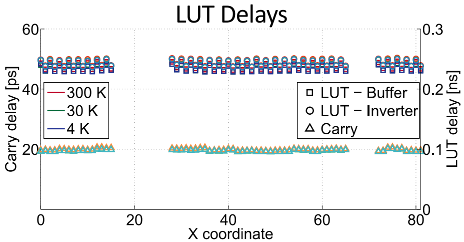
Carry: 20 vs. 8.4 ps at 300 K

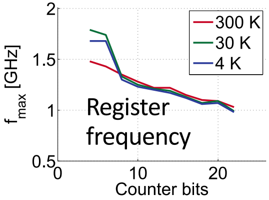
LUTs: 238 vs 235 ps at 300 K

Speed-up 2.4 vs 10.8% toward 300 K









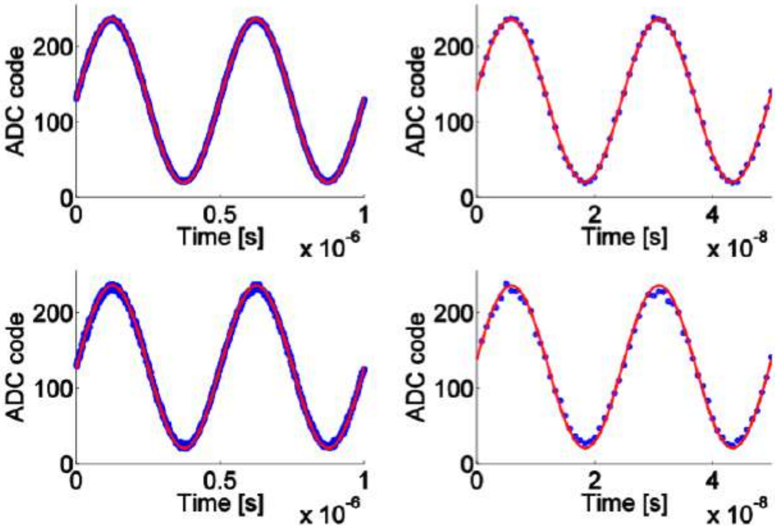
ADC on FPGA (1.2GSa/s)

Signal bandwidth: 2 MHz

Signal bandwidth: 40 MHz

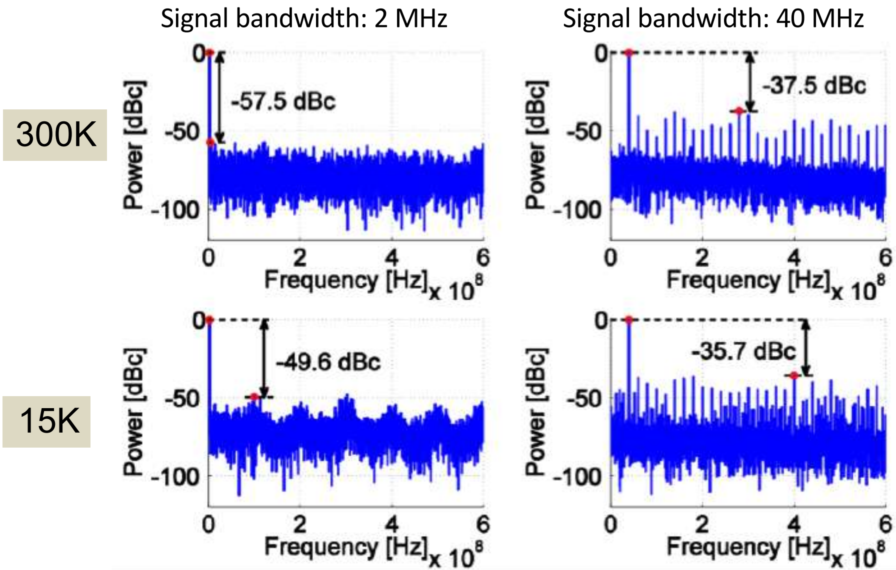
300K

15K



H. Homulle et al., TCAS I, 63(11), 1854-1865, 2016

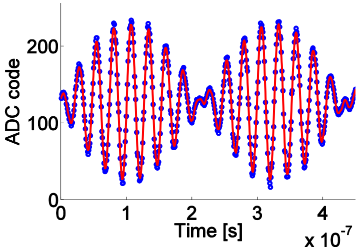
ADC on FPGA

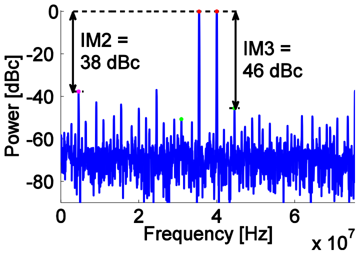


H. Homulle et al., TCAS I, 63(11), 1854-1865, 2016

Distortion (IM2, IM3)

- Two tones: ≈ 36 / 41 MHz
  - IM2 = 38 dB
  - IM3 = 46 dB
- Many secondary harmonics
- Interference with 100 MHz (sampling tone)

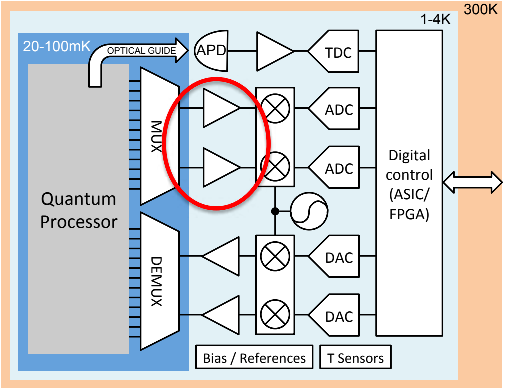


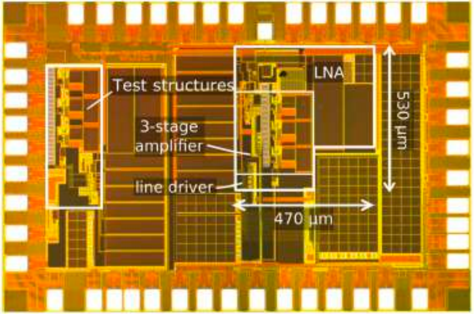


H. Homulle et al., TCAS I, 63(11), 1854-1865, 2016

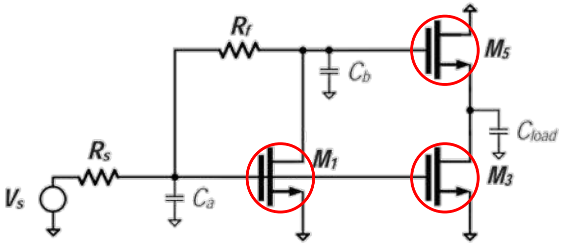
Cryogenic ASICs

Low Noise Amplifiers (Cryo-LNAs)





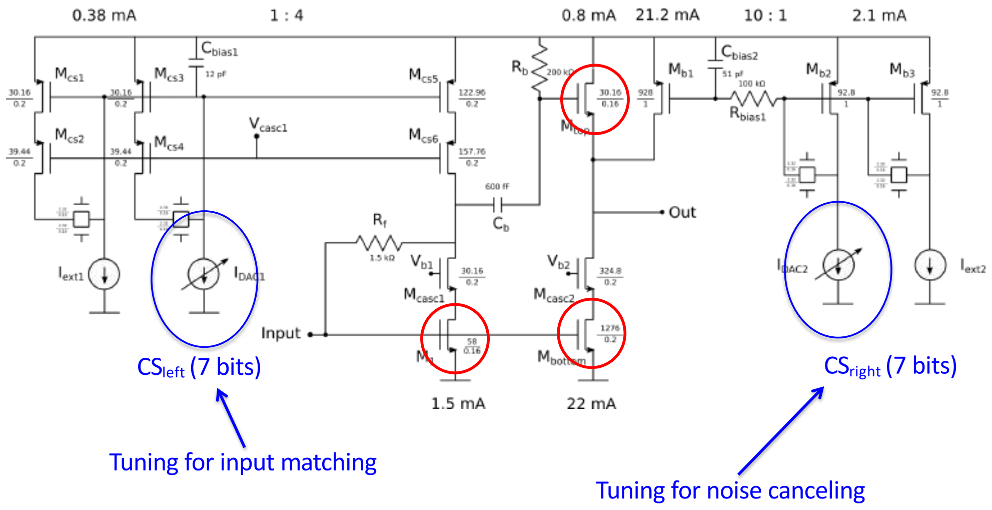
Cryo-LNA



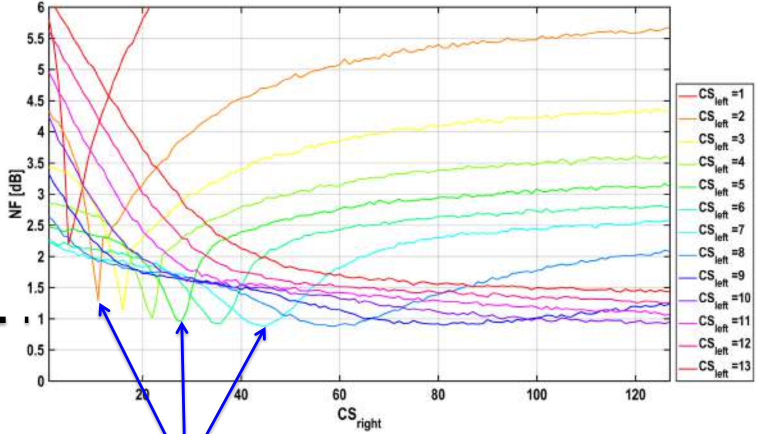
F. Bruccoleri et al., *JSSC* 2004

- Standard 160nm CMOS
- 500 MHz Bandwidth
- 0.1dB Noise figure
- 7K noise-equivalent temperature

Cryo-LNA


0.38 mA
1 : 4
0.8 mA
21.2 mA
10 : 1
2.1 mA
Cbias1
12 pF
Mcs1
Mcs3
Mcs5
Mcs2
Mcs4
Mcs6
Vcasc1
Rb
200 kΩ
Mtop
Mb1
Cbias2
51 pF
100 kΩ
Rbias1
Mb2
Mb3
600 fF
Cb
Out
Rf
1.5 kΩ
Vb1
Mcasc1
Vb2
Mcasc2
Iext1
IDAC1
IDAC2
Iext2
Input
M1
Mbottom
1.5 mA
22 mA
CSleft (7 bits)
CSright (7 bits)
Tuning for input matching
Tuning for noise canceling

Noise Figure at RT

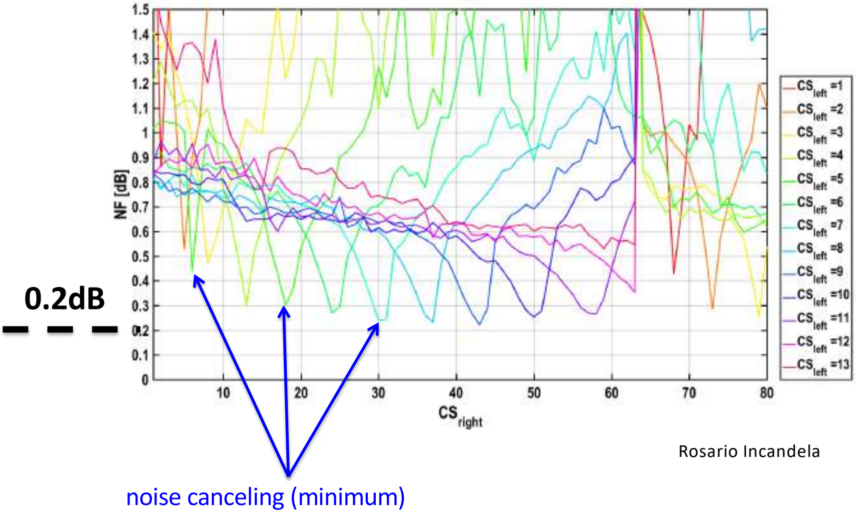


1dB

noise canceling (minimum)

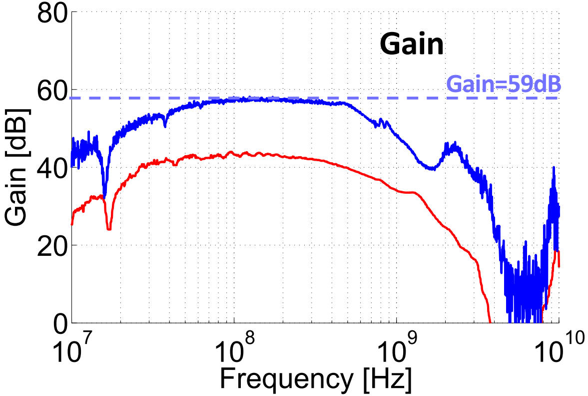
Rosario Incandela

Noise Figure at 4K

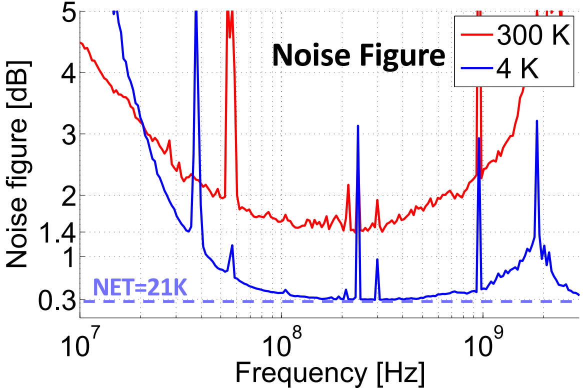


Rosario Incandela

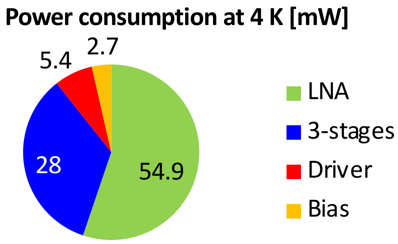
Gain and Noise



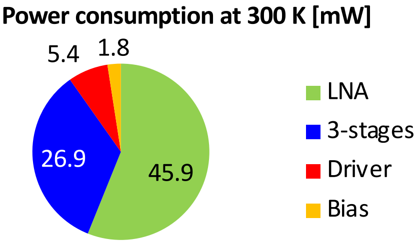
B. Patra, R. Incandela et al, *JSSC* 2018



Power



Measured: **91mW**



Measured: **80mW**

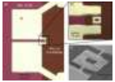
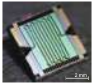
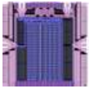
Sharing 150x 1MHz-channels (one channel per qubit)

=

0.61mW per qubit

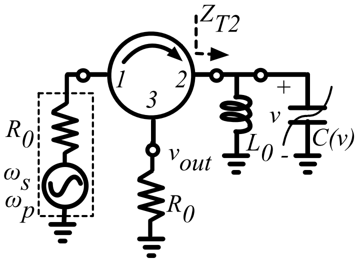
Rosario Incandela

Can We Do Better?

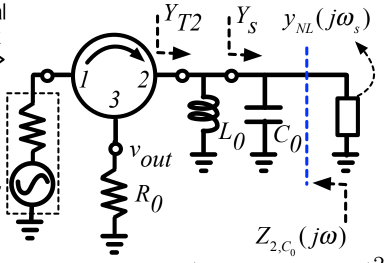
Amplifier Metrics	Cryogenic HEMT 	JPA 	TWPA 1.0 	TWPA 2.0 
Power Dissipation	16 mW	100 pW	1 nW	5 nW
Bandwidth (>15 dB gain)	11 GHz	100 - 200 MHz	6 GHz	5 GHz
1-dB Compression point	0 dBm	-110 dBm (3 qubits)	-95 dBm (20-30 qubits)	-85 dBm (> 100 qubits)
Noise Temperature	5 K	400 mK	400 mK	400 mK
External Hardware	Isolator	Direct. Coupler, Circulator	Direct. Coupler	None

Courtesy: David Hover and Greg Calusine, MIT Lincoln Laboratory

Can We Do Better?



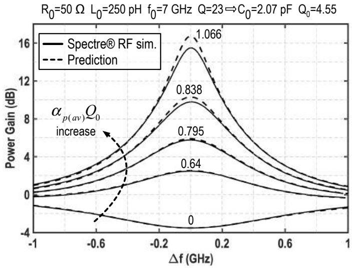
small-signal
framework



$$y_{NL}(j\omega_s) \approx -\omega_s\omega_i(\alpha_p C_0)^2 Z^*_{2,C_0}(j\omega_i)$$

$$\alpha_p \equiv K_1 V_p$$

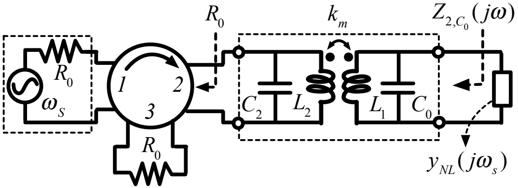
$$G_{T_{\max}}\big|_{Q\to\infty} = \left|\frac{1+(\alpha_p Q_0)^2}{1-(\alpha_p Q_0)^2}\right|^2$$

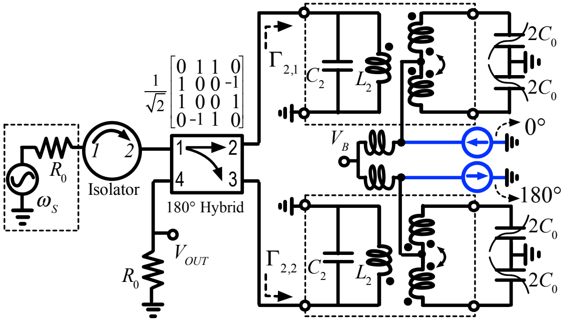


Major challenges:

- Narrowband
- Phase sensitive
- Large pump signal
- T_n limit of 4K @ 4K

CMOS Parametric Amplifier



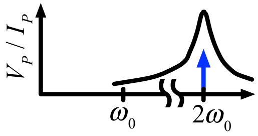


1) Transformer-based parametric amplifier

- ✓ Allow for broadband operation

2) CM impedance peaking

- ✓ Suppress the pump signal leak
- ✓ Reduce pump power consumption

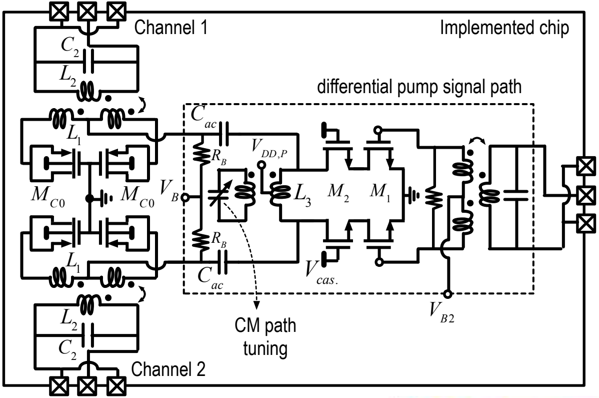


3) "image"–rejection architecture

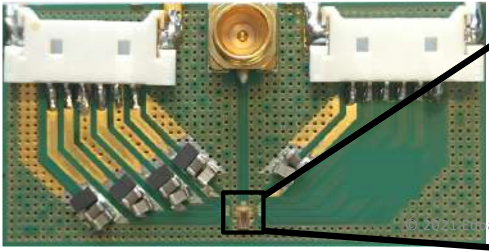
- ✓ Double the usable RF bandwidth
- ✓ Phase-insensitive operation
- ✓ Allow for T_n limit of below 4K

M. Mehrpoo, F. Sebastiano, E. Charbon, M. Babaie, *Solid-State Circuit Letters*, 2020

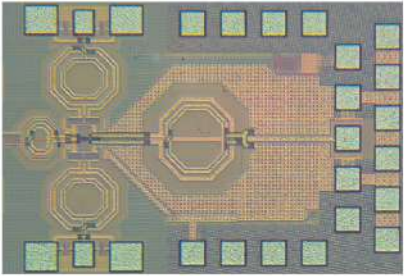
CMOS PA Architecture



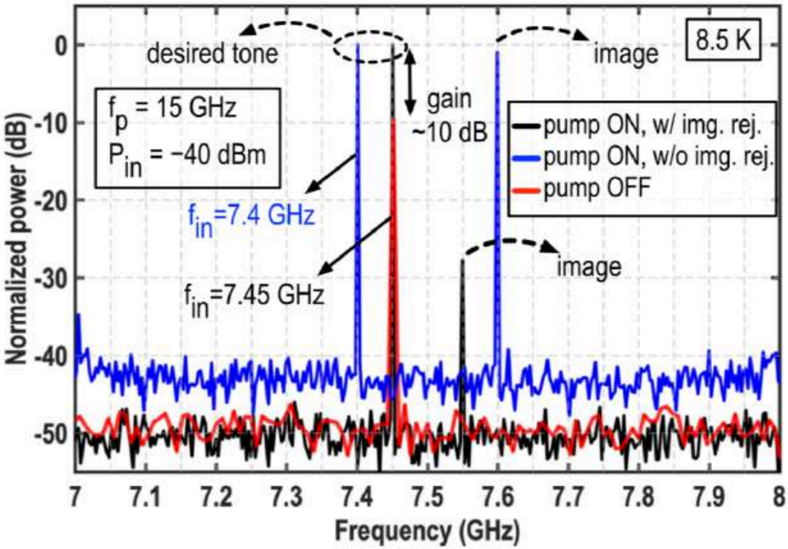
M. Mehrpoo, F. Sebastiano, E. Charbon, M. Babaie, *Solid-State Circuit Letters*, 2020



0.825 mm^2

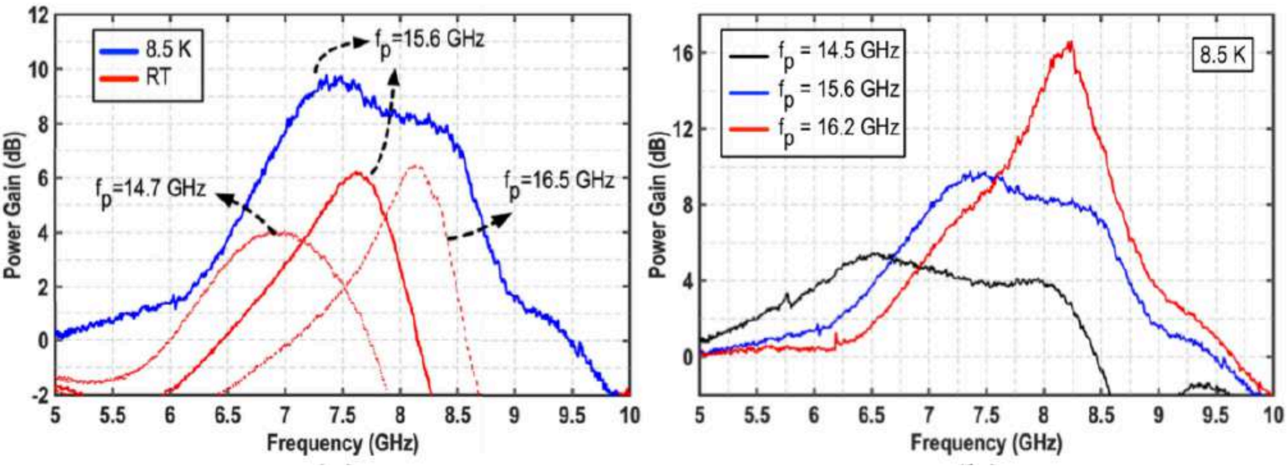


Spectrum of Single Tone



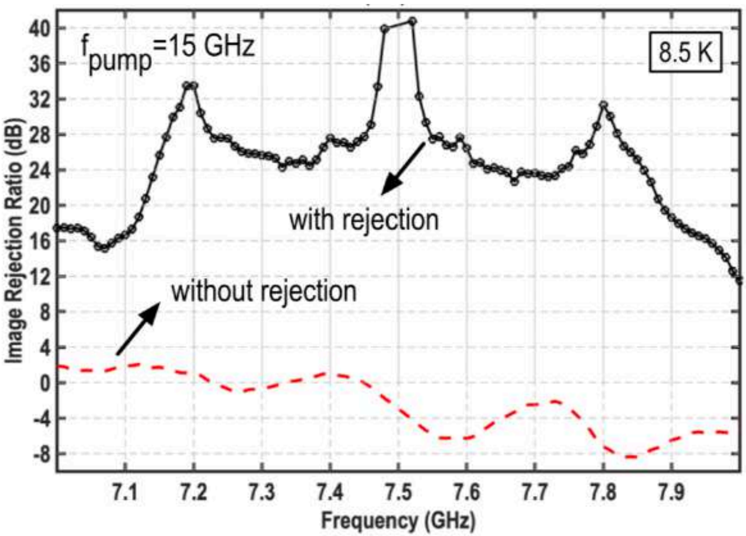
M. Mehrpoo, F. Sebastiano, E. Charbon, M. Babaie, *Solid-State Circuit Letters*, 2020

Power Gain vs. Pump Frequency and Temperature



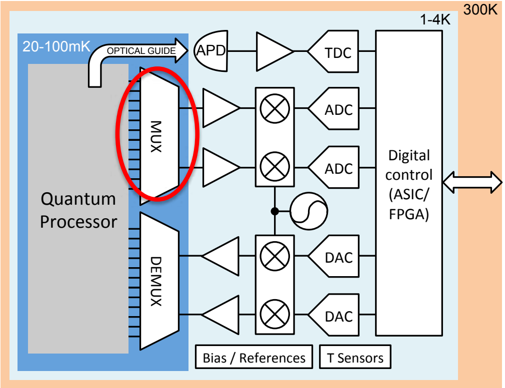
M. Mehrpoo, F. Sebastiano, E. Charbon, M. Babaie, *Solid-State Circuit Letters*, 2020

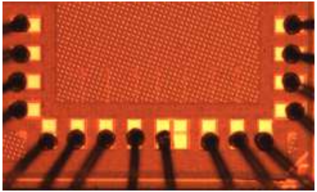
Image Rejection

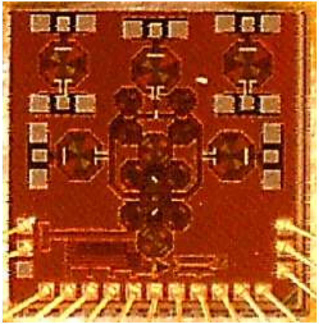


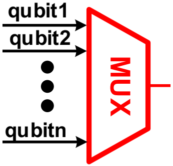
M. Mehrpoo, F. Sebastiano, E. Charbon, M. Babaie, *Solid-State Circuit Letters*, 2020

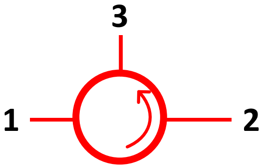
CMOS Passive Circulators & Multiplexers



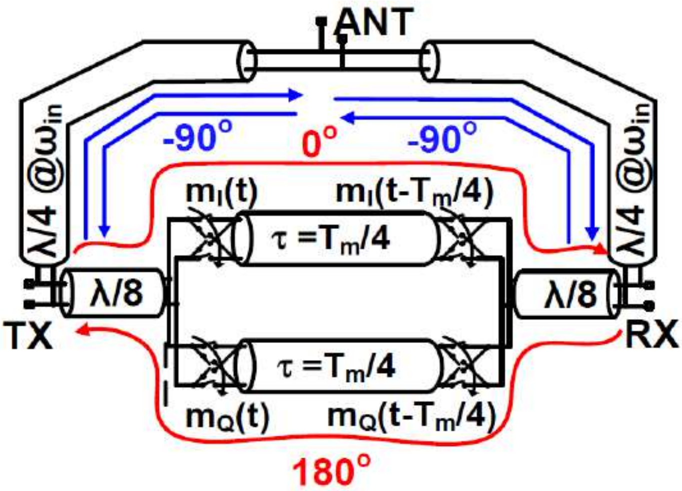


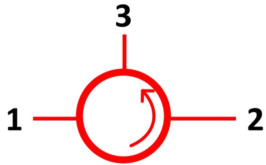






Transmission Line Circulator



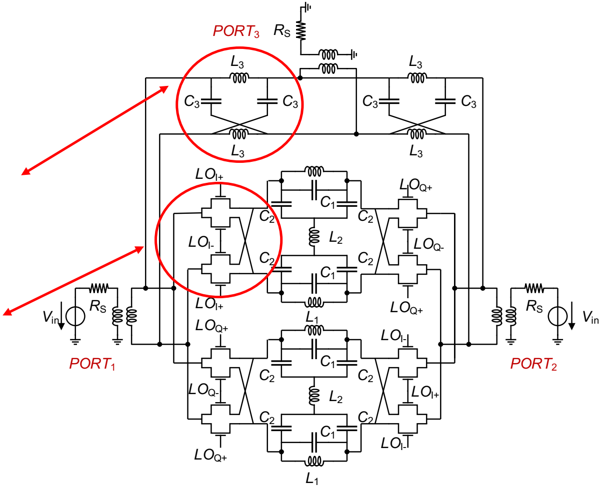


S-parameters at $\omega_{in} = 3\omega_m$

$$S = \begin{bmatrix} 0 & 0 & -1 \\ -j & 0 & 0 \\ 0 & -j & 0 \end{bmatrix}$$

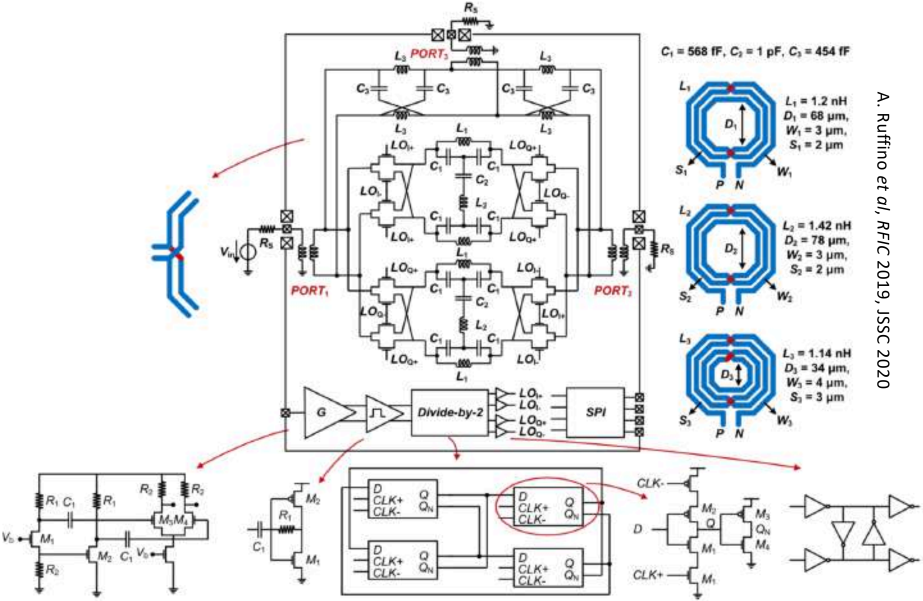
Passive Circulator Architecture

- Non-reciprocal behavior due to staggered commutation
- Passive LC all-pass filters
- Passive mixers with non-overlapping I/Q phases
- On-chip LO divider and I/Q generation
- SPI control for tunability



P_{DC} = 1.7 mW
P_{AUX} = 8 mW

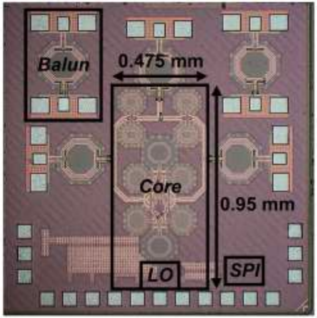
Passive Circulator Architecture



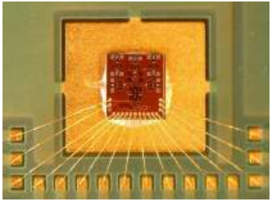
A. Ruffino *et al*, *RFIC* 2019, JSSC 2020

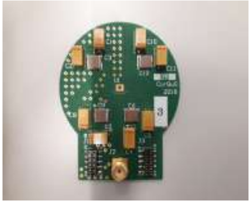
CMOS 40 nm Circulator Prototype

- TSMC CMOS 40 nm technology
- Tape-out, PCB design and measurements at 300 K and 4.2 K
- RF probing with LakeShore CPX probe station

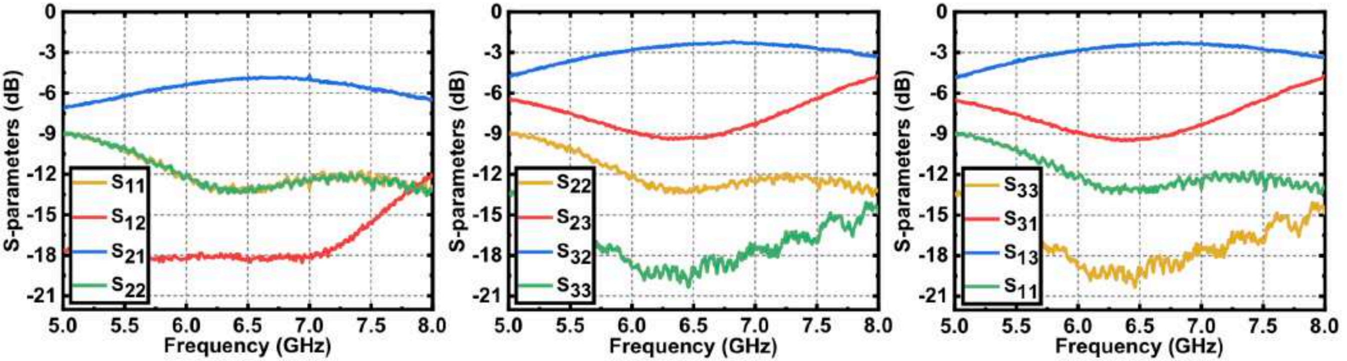


A. Ruffino *et al*, *RFIC* 2019, JSSC 2020



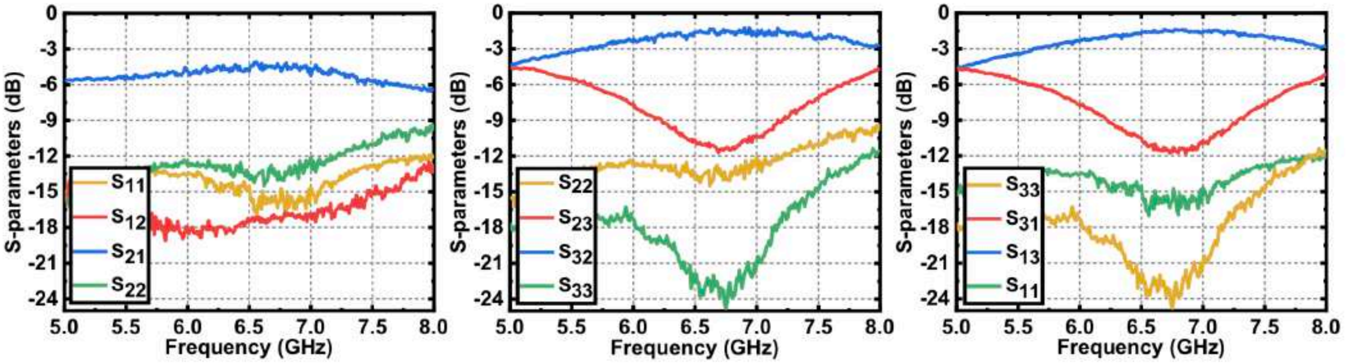


Measured S-parameters (300K)



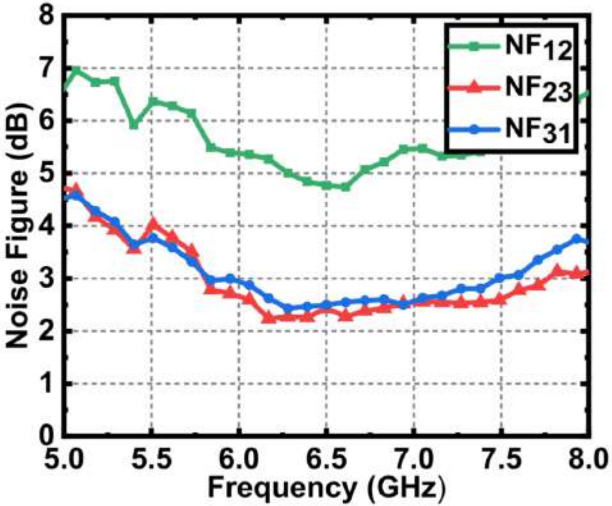
A. Ruffino *et al*, *RFIC* 2019, JSSC 2020

Measured S-parameters (4.2K)



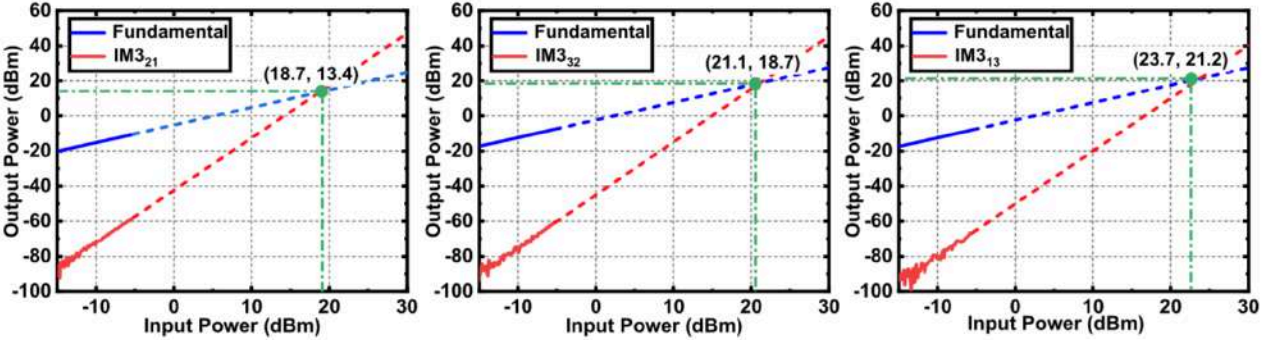
A. Ruffino *et al*, *RFIC* 2019, JSSC 2020

Circulator Noise Figure (300K)



Minimum noise figure of 2.1 dB is measured, consistent with insertion loss measurements.
There is no excess noise from clock generation path.

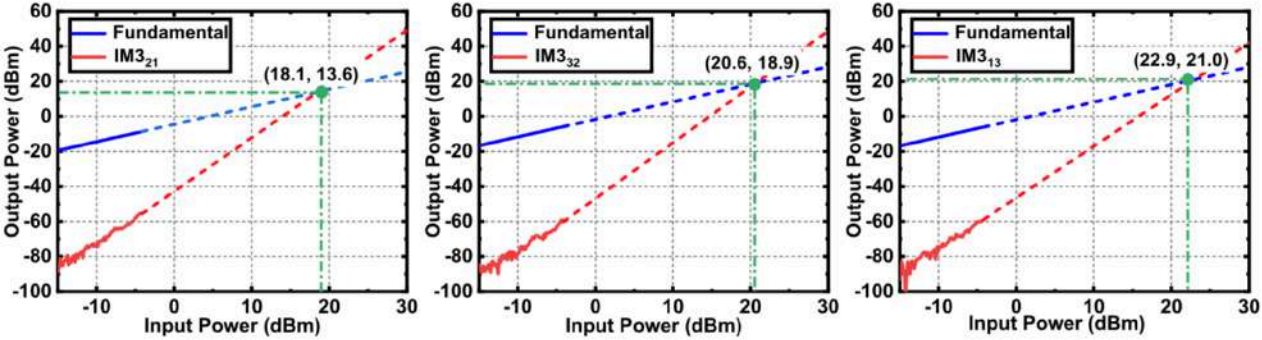
Circulator Linearity (300K)



A. Ruffino *et al*, *RFIC* 2019, JSSC 2020

High linearity is measured in all directions, due to the quasi-passive nature of the circulator.

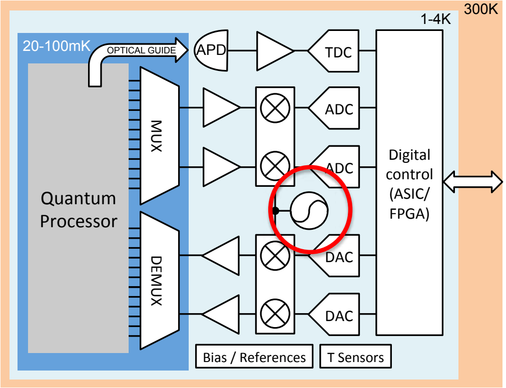
Circulator Linearity (4.2K)

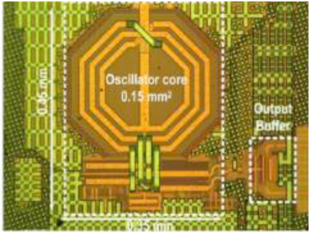


A. Ruffino *et al*, *RFIC* 2019, JSSC 2020

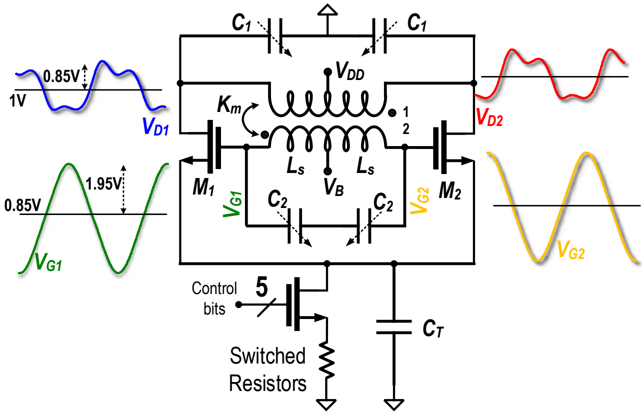
High linearity is measured in all directions, due to the quasi-passive nature of the circulator.

Cryo-Oscillators



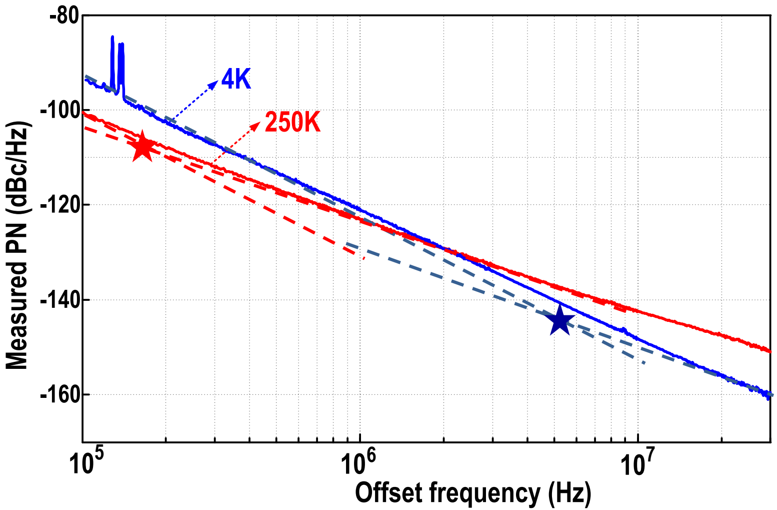


Cryo-Oscillator (Class F)



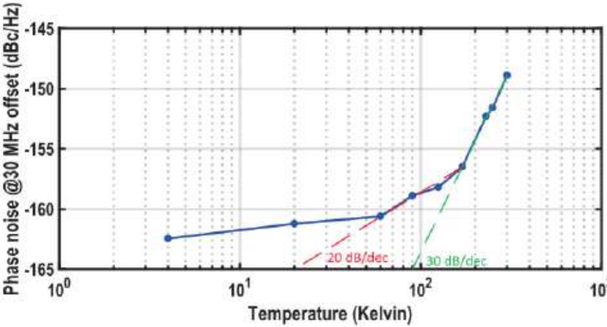
M. Shahmohammadi, *ISSCC* 2015

Phase Noise



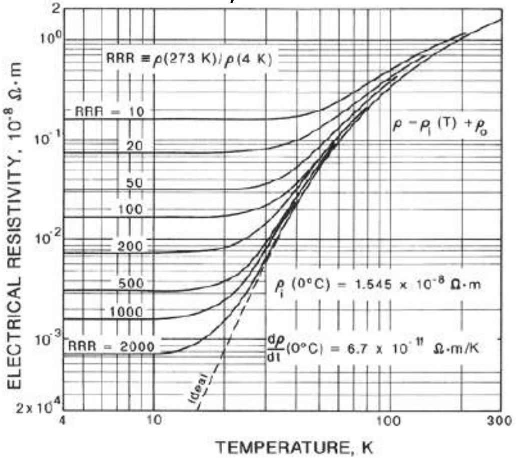
-80
-100
-120
-140
-160
Measured PN (dBc/Hz)
4K
250K
10^5
10^6
10^7
Offset frequency (Hz)

Measured Phase Noise



B. Patra et al, *JSSC* 2018

Curtesy: Masoud Babaie

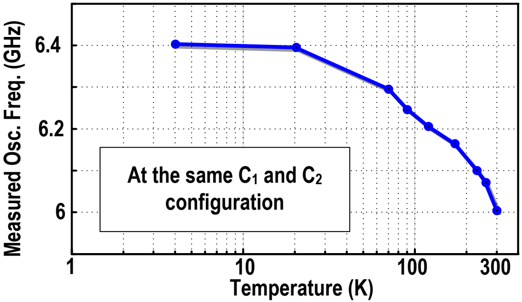


Source: copper.org

Sources of noise:

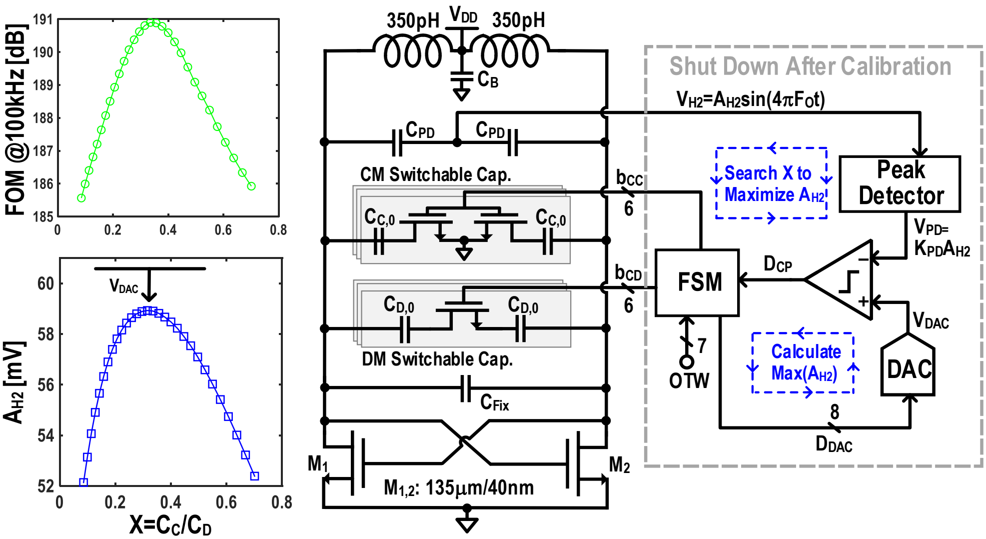
- Thermal noise
- Shot noise
- Impurities in copper

Frequency Stability

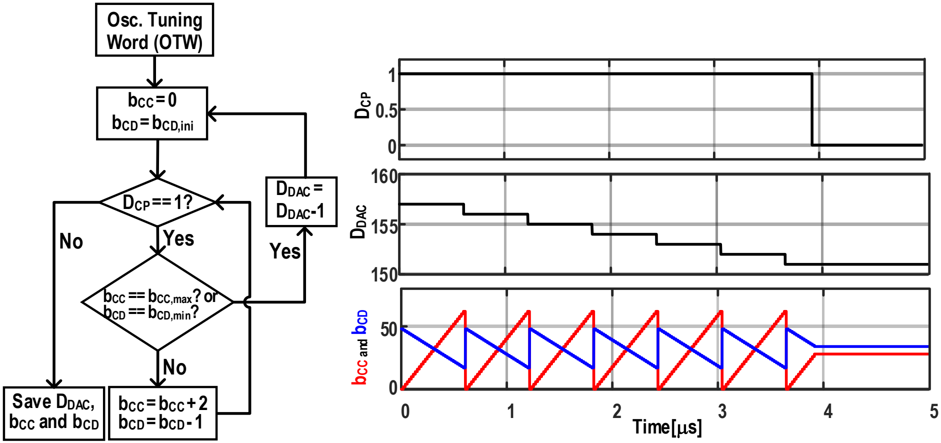


B. Patra et al, *JSSC* 2018

Improving Frequency Stability

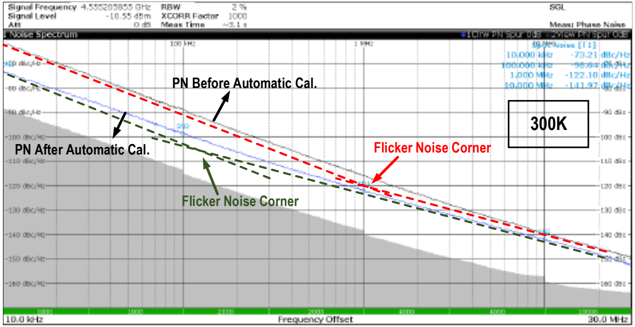


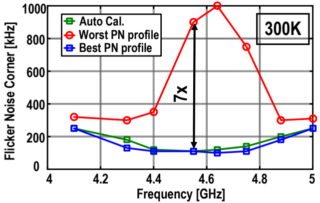
Improving Frequency Stability (2)

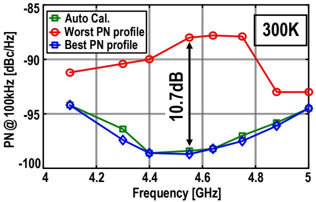


J. Gong, F. Sebastiano, E. Charbon, M. Babaie, *ISSCC* 2020

Phase Noise at 300K

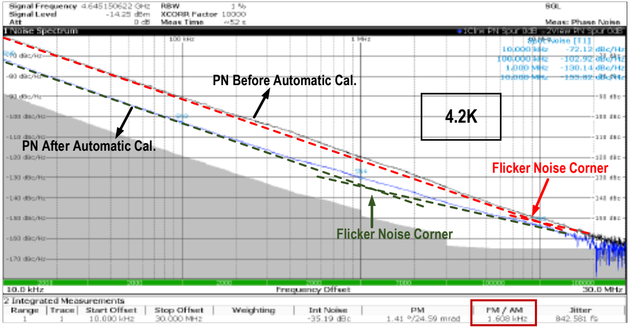


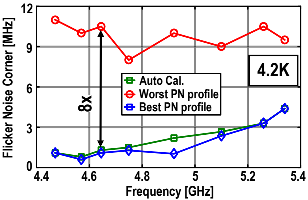


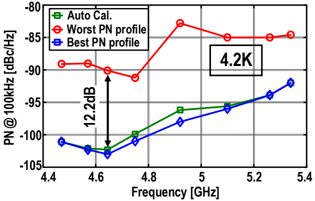


J. Gong, F. Sebastiano, E. Charbon, M. Babaie, *ISSCC* 2020

Phase Noise at 4K

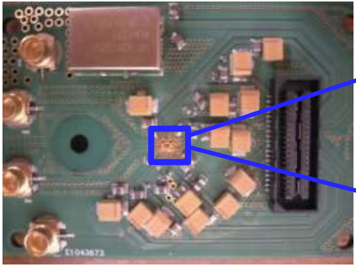


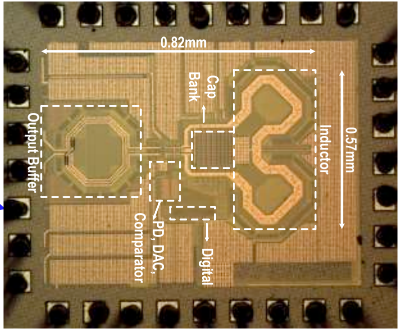




J. Gong, F. Sebastiano, E. Charbon, M. Babaie, *ISSCC* 2020

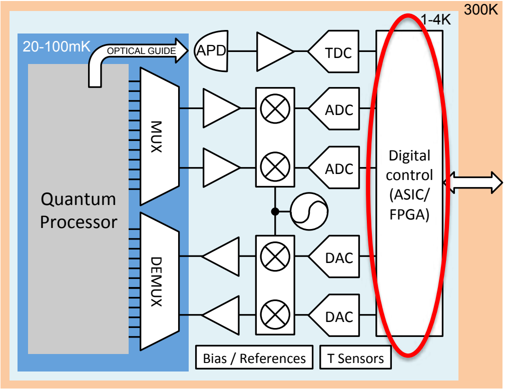
Implementation in 40nm CMOS Node

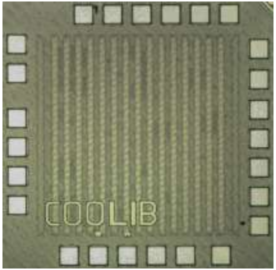


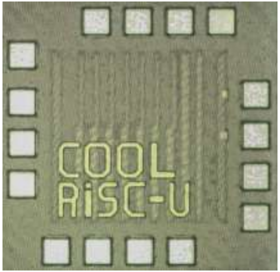


Measurements at RT:
Technology: 40nm CMOS
F_{out}: 4.05-5.16GHz (24.1%)
F_{ref}: 20MHz
Supply: 0.5V (oscillator core)
Power consumption: 3.2mW
PN @10MHz: -141.5dBc/Hz
PN@100kHz:-98.8dBc/Hz

Cryo-Logic


300K
1-4K
20-100mK
OPTICAL GUIDE
APD
TDC
ADC
ADC
DAC
DAC
MUX
DEMUX
Quantum Processor
Digital control (ASIC/ FPGA)
Bias / References
T Sensors

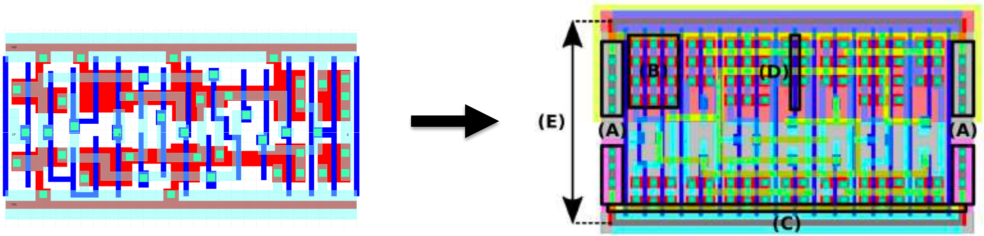

COOLIB


COOL
RiSC-U

Ultra-Low Voltage Library ‘cooLib’

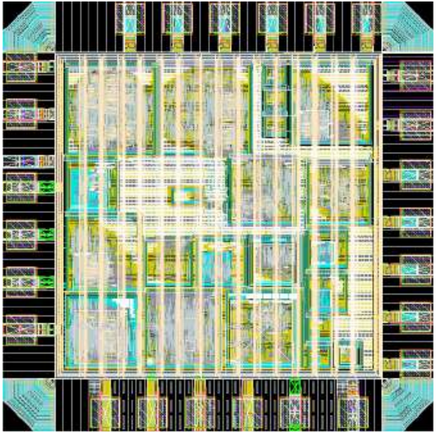
- Digital library optimized for 4K
- Ultra low voltage operation (100s mV)
- Sub-threshold bias of N/P MOS
- Resilient to latchup and hysteresis-free
- Several logic families (static and dynamic CMOS)
- Compatible with commercial P&R tools

D-Flip-flop optimized for 4K (40nm CMOS)



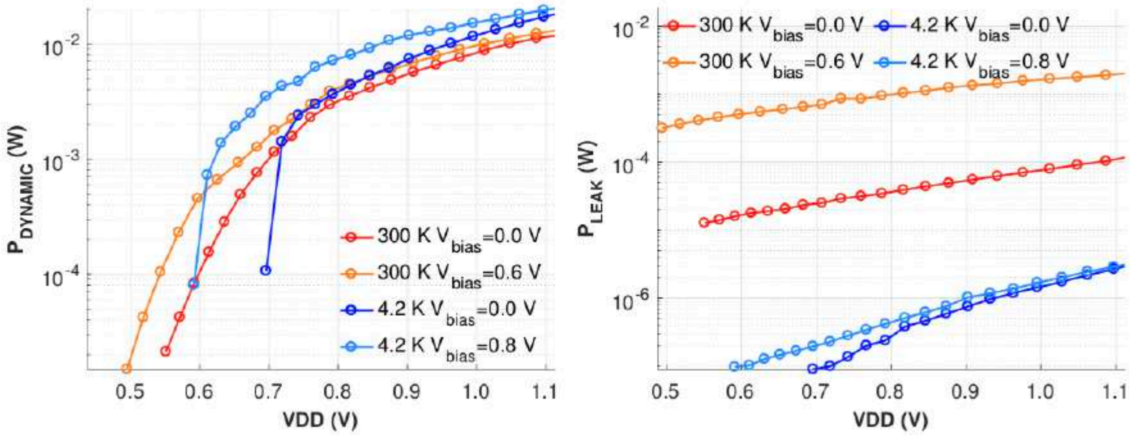
Test Chip Implementation

- Compare 'CooLib' cells to foundry supplied std. cells of TSMC40LP process
- Contains commonly encountered digital circuits
  - i.e. unsigned multiplier
- Four versions per circuit
  - Static 'CooLib'
  - Domino 'CooLib'
  - TSMC40LP, restricted
  - TSMC40LP, unrestricted
- One 'true' domino logic implementation

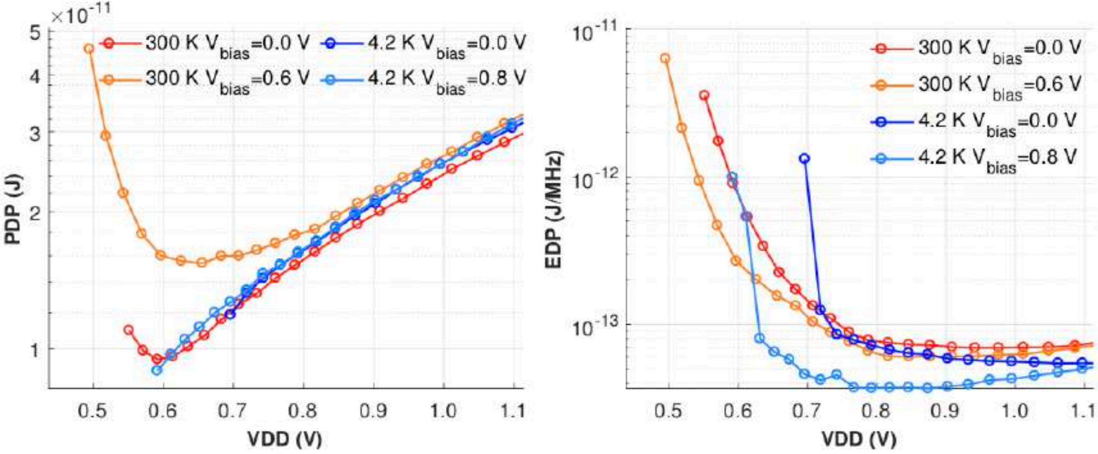


E. Schriek *et al.*, IEEE *Solid-State Circuits Letters* 2020

Dynamic vs. Static Power at Cryo



FOMs



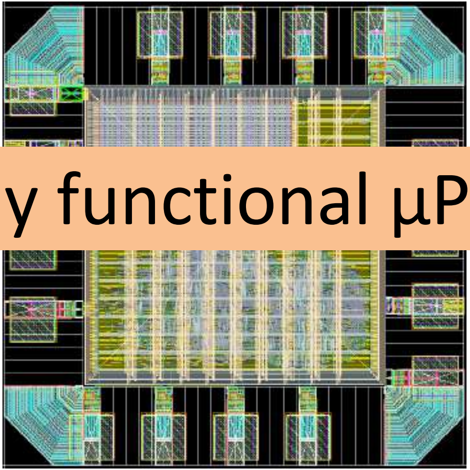
PDP: power-delay product
EDP: energy-delay product

Benchmarking

		$V_{DD,MIN}$ [V]			F_{MAX} @ 0.6 V [MHz]			F_{MAX} @ 0.7 V [MHz]			P_{AVG} @ 100 kHz [μW]		
Benchmark	Temp.	Proposed	A	B	Proposed	A	B	Proposed	A	B	Proposed	A	B
16X16 Multiplier	4.2 K	0.54	0.68	0.68	16.3	-	-	74.2	4.6	2.0	2.34	3.76	3.88
	300 K	0.3	0.49	0.44	100.4	9.7	17.4	145.2	34.0	39.7	0.61	2.68	1.92
EPFL Sine	4.2 K	0.58	0.68	0.68	1.95	-	-	20.9	2.2	1.1	3.91	4.00	4.46
	300 K	0.39	0.34	0.39	15.2	9.2	9.5	29.6	25.5	26.4	3.46	2.11	2.18
EPFL Int-to-Float	4.2 K	0.54	0.68	0.68	51.4	-	-	178.1	42.5	11.7	0.80	1.57	3.41
	300 K	0.24	0.38	0.36	118.5	75.2	73.44	174.2	191.9	158.0	0.08	0.55	0.28
EPFL Round-Robin Arbiter	4.2 K	0.58	0.68	0.68	21.6	-	-	46.6	2.0	1.8	7.89	11.56	11.64
	300 K	0.32	0.32	0.31	33.7	10.0	34.7	59.9	37.3	80.8	1.72	3.20	2.25

E. Schriek *et al.*, IEEE *Solid-State Circuits Letters* 2020

‘CooLib’ RISC-V Implementation



E. Schriek *et al.*, IEEE *Solid-State Circuits Letters* 2020

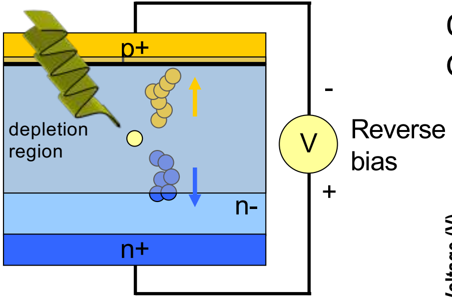
FEATURES

- RISC-V (picorv32, open-source) implemented using ‘CooLib’

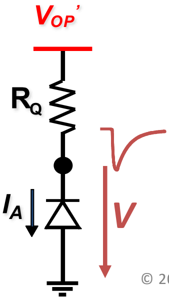
Fully functional µP operating at 4K

  - Interfacing by ‘CooLib’ level-shifters
- UART interface for serial in/output
- JTAG interface for SRAM write/read

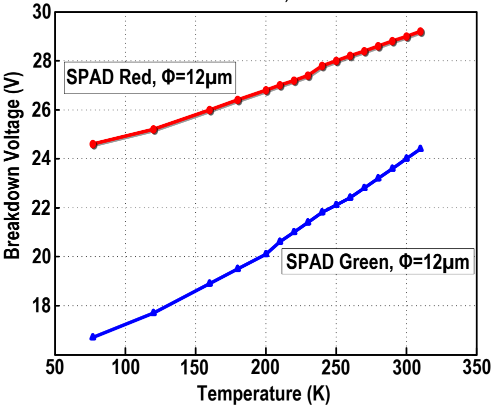
Cryo-Single-Photon APDs (Cryo-SPADs)



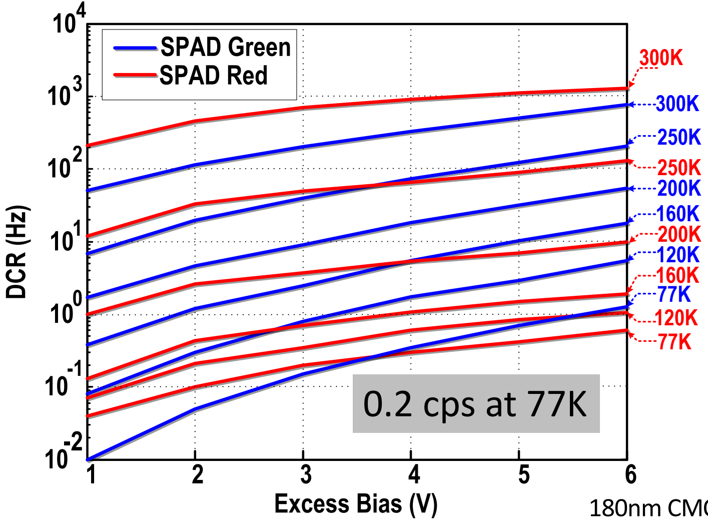
Operation in proportional and Geiger mode (SPAD)



E. Charbon *et al.*, *ISSCC* 2017



Cryo-SPADs

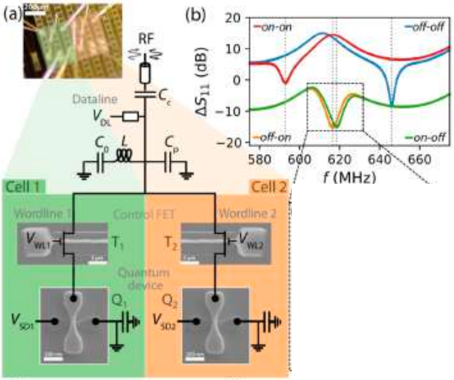


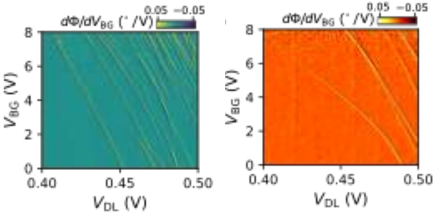
180nm CMOS bulk

B. Patra *et al.*, *JSSC* 2018

Qubits and Control in the Fridge

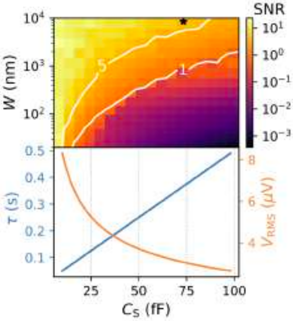
Step 1: Multiplexing Qubits





Two device gate maps measured in an interleaved manner

Approach can be applied down to 100nm scale

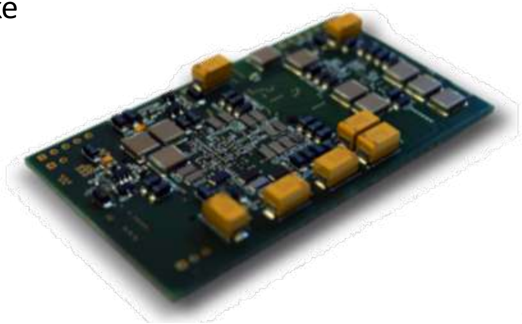


S Schaal *et al.*, arXiv:1809.03894

Step 2: Reading Qubits

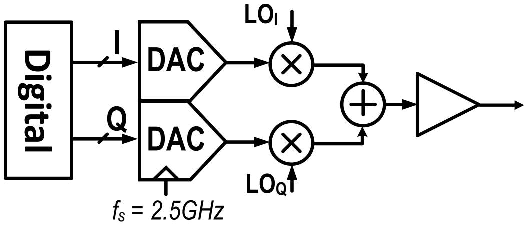
- **Single-shot dispersive readout**
- ***Single electron transistor*** readout
- (limited) use of 3D stacking
- Ideally bring qubits to 1-4K, make them CMOS-compatible

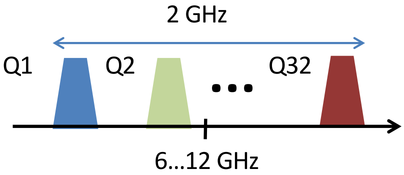
H. Homulle et al., QuRO interface Silicon Quantum Electronics Workshop, 2018



Step 3: Controlling Qubits

- Lower Speed DAC + Mixer





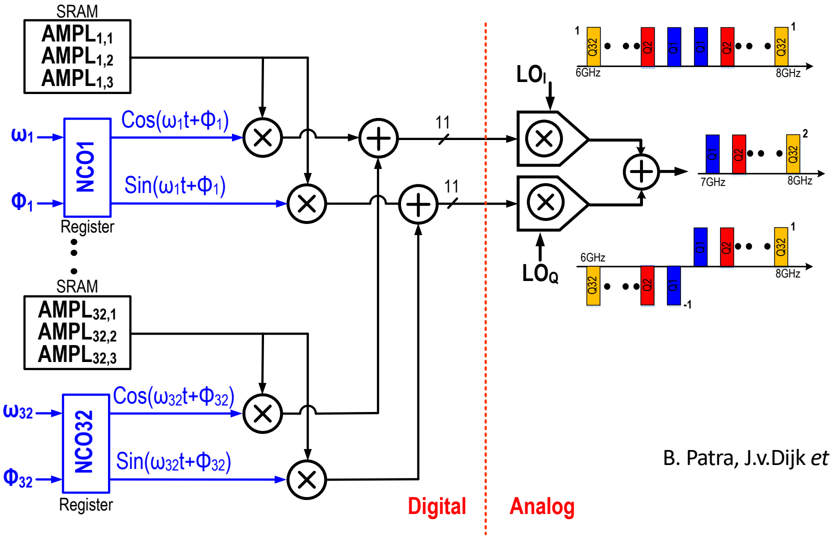
Analog: noise/linearity specifications known + feasible

Controlling Qubits: Specs

- Target fidelity: 99.99% for 1…10 MHz operation
- Analog:

Error Source	*Type*	*Value*	*Contribution*
Microwave frequency	inaccuracy	35.4 kHz	1-F = 12.5 ppm
(nominally 5…13 GHz)	noise	35.4 kHz_{rms}	1-F = 12.5 ppm
Microwave phase	Inaccuracy	0.20 °	1-F = 12.5 ppm
	noise	0.20 °	1-F = 12.5 ppm
Microwave amplitude	inaccuracy	38.3 µV	1-F = 12.5 ppm
(nominally 17 mV, -53 dB)	noise	38.3 μV_{rms}	1-F = 12.5 ppm
Microwave duration	inaccuracy	113 ps	1-F = 12.5 ppm
(nominally 50 ns)	noise	113 ps_{rms}	1-F = 12.5 ppm +
			F = 99.99%

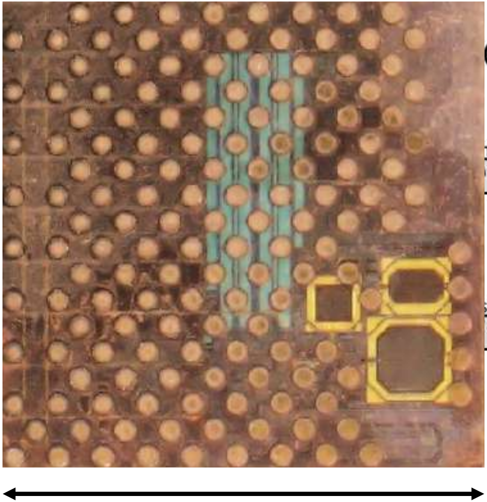
Controller Architecture: Horse Ridge



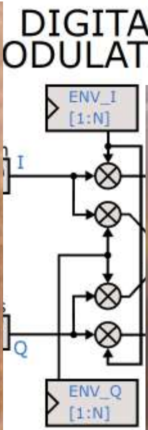
B. Patra, J.v.Dijk *et al.*, *ISSCC* 2020

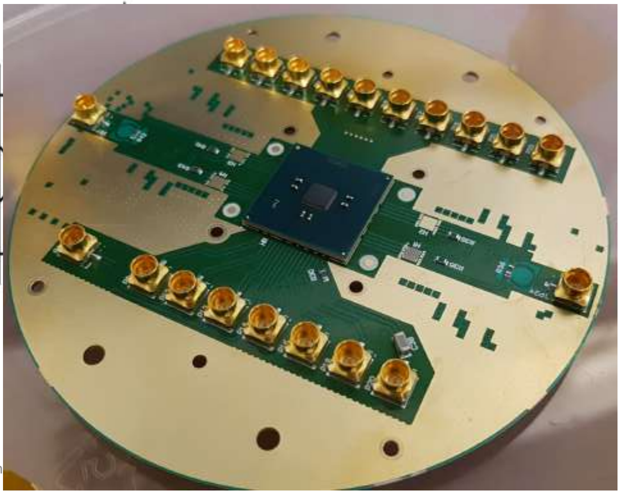
Controller Implementation

B. Patra, J.v.Dijk *et al.*, *ISSCC* 2020

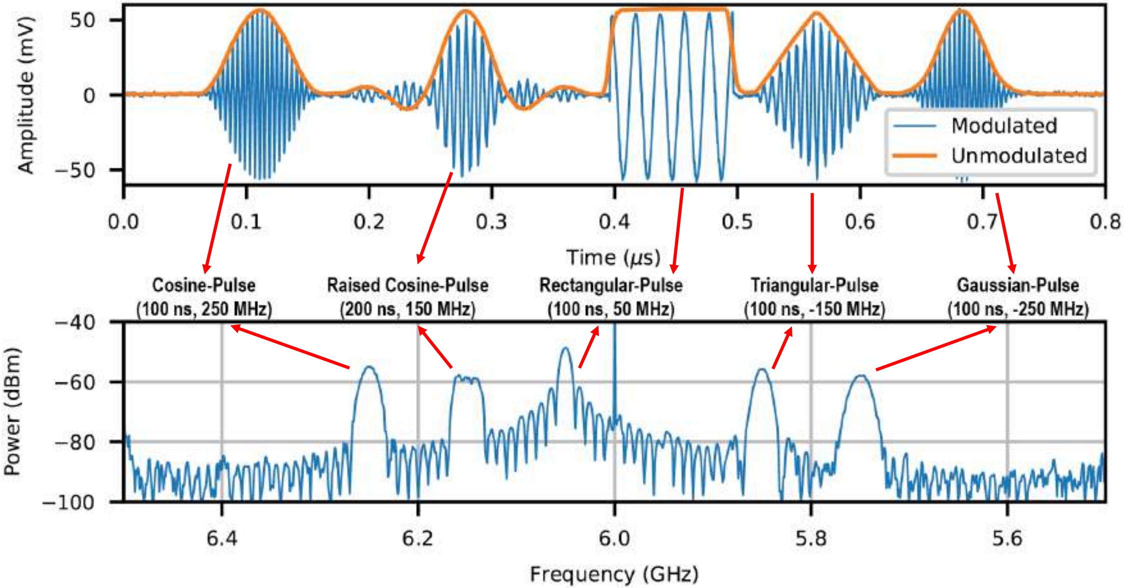


2 mm

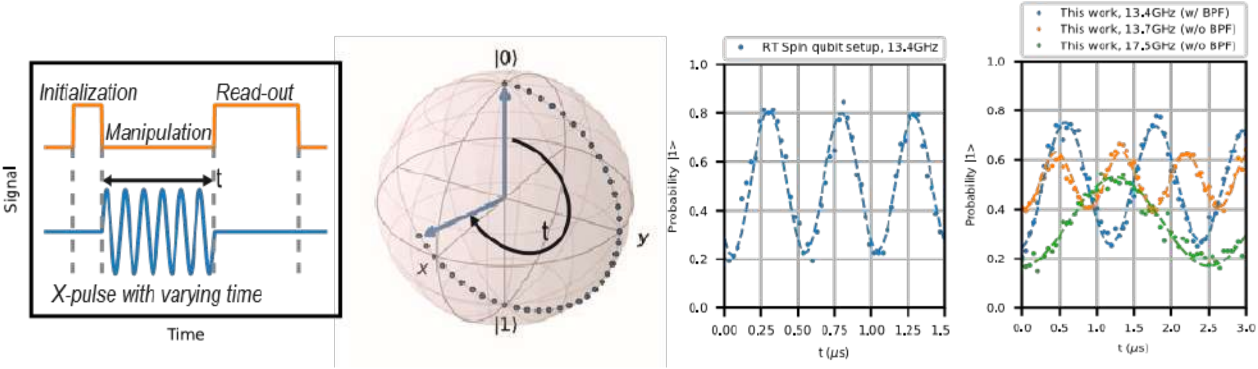




Pulse Shaping

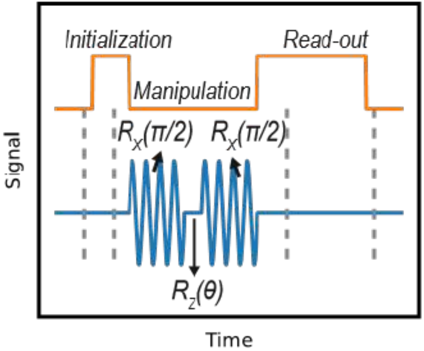


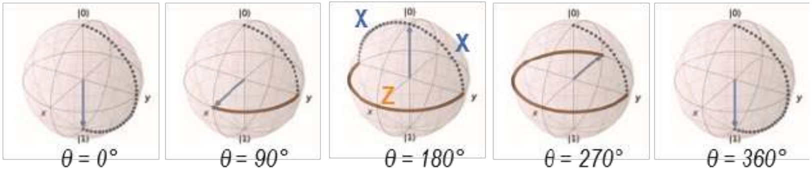
Rabi Experiment

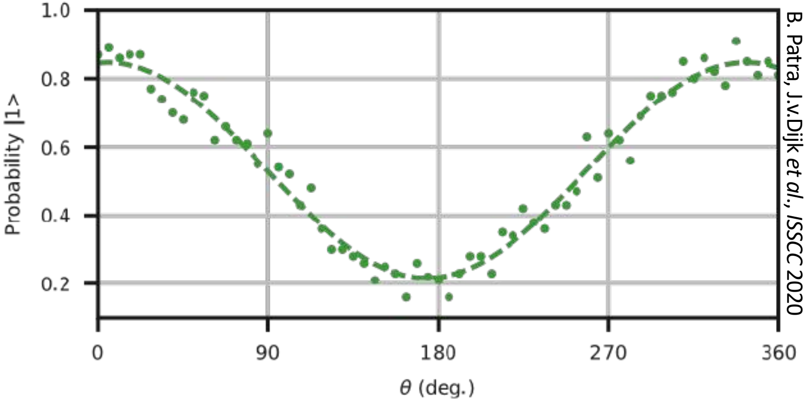


B. Patra, J.v.Dijk *et al.*, *ISSCC* 2020

Qubit Manipulation







B. Patra, J.v.Dijk *et al., ISSCC 2020*

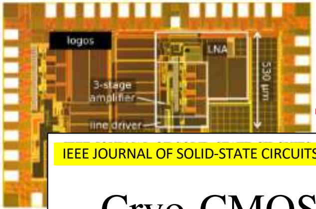
Comparison Table

	Horse Ridge (ISSCC'20)	ISSCC'19	RSI'17	Spin qubit setup
Operating Temperature	3 K	3 K	300 K	300 K
Qubit platform	**Spin qubits + Transmons**	Transmons	Transmons	Spin qubits
Qubit frequency	**2 – 20 GHz**	4 – 8 GHz		< 20 GHz
Channels	**128 (32 per TX)**	1	4	1
FDMA	**Yes, SSB**	No	Yes, SSB	No
Data Bandwidth	1 GHz	400 MHz	960 MHz	520 MHz
Image & LO leakage calibration	**On chip**	Off chip	Yes	
Phase correction	**Yes**	No	No	No
Fidelity (expected)	**99.99%**	-	-	-
Waveform/Instructions	**Upto 40960 pts AWG**	Fixed 22 pts symmetric		16M pts AWG
Instruction set	**Yes**	No	Yes	Yes
Power / TX	Analog: 1.7 mW/qubit * Digital: 330 mW ‡	Analog < 2 mW/qubit # Digital: N/A		850 W
Chip area / TX	4 mm^2	1.6 mm^2	Discrete components	Rack mount
Technology	22 nm FinFET CMOS	28 nm bulk CMOS		

* including LO/Clock driver; only RF-Low active   # does not mention circuits included

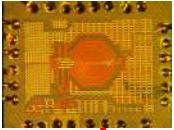
‡ can be reduced with clock gating

In Summa

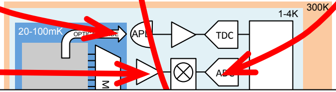


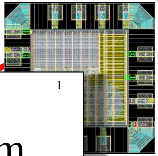
IEEE IEDM 2016

IEEE ISSCC 2017



IEEE IEDM 2016



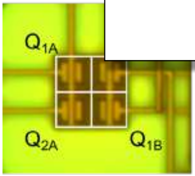


IEEE JOURNAL OF SOLID-STATE CIRCUITS 1

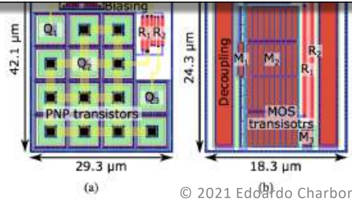
Cryo-CMOS Circuits and Systems for Quantum Computing Applications

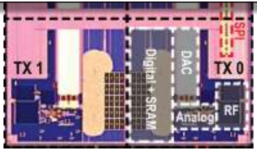
Bishnu Patra, *Student Member, IEEE*, Rosario M. Incandela, *Student Member, IEEE*, Jeroen P. G. van Dijk, Harald A. R. Homulle, Lin Song, Mina Shahmohammadi, *Member, IEEE*, Robert Bogdan Staszewski, *Fellow, IEEE*, Andrei Vladimirescu, *Fellow, IEEE*, Masoud Babaie, *Member, IEEE*, Fabio Sebastiano, *Senior Member, IEEE*, and Edoardo Charbon, *Fellow, IEEE*

ISSCC 2020



IEEE Sensors 2016

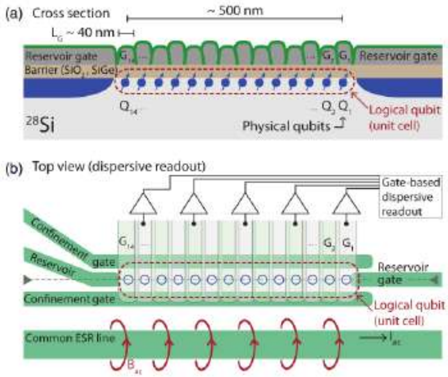




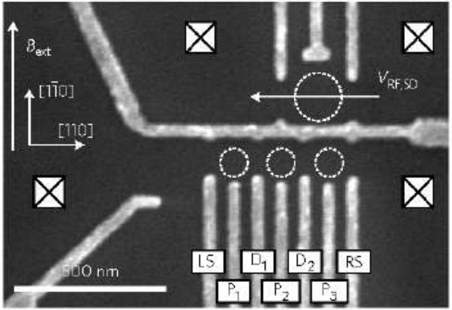
IEEE ISSCC 2020

5. Conclusions

Realizations of 1D Qubit Arrangements

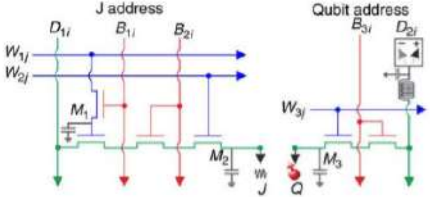


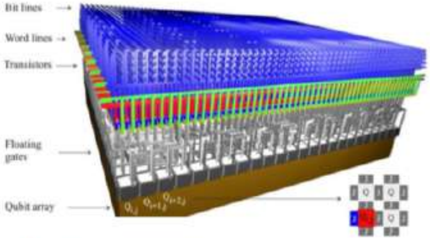
Jones *et al*, PRX 8, 021058 (2018)



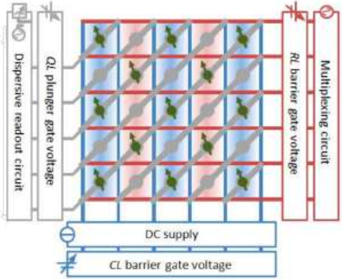
Baart *et al*, Nat Nano (2017)

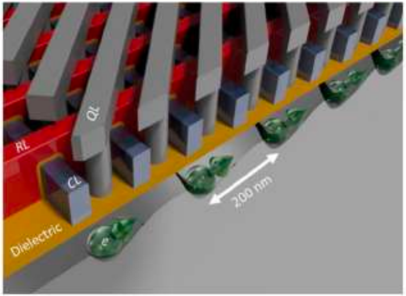
Proposals for Scalable Fault-Tolerant 2D Qubit Arrangements





M. Veldhorst et al. (UNSW), Nature Comm. (2017)



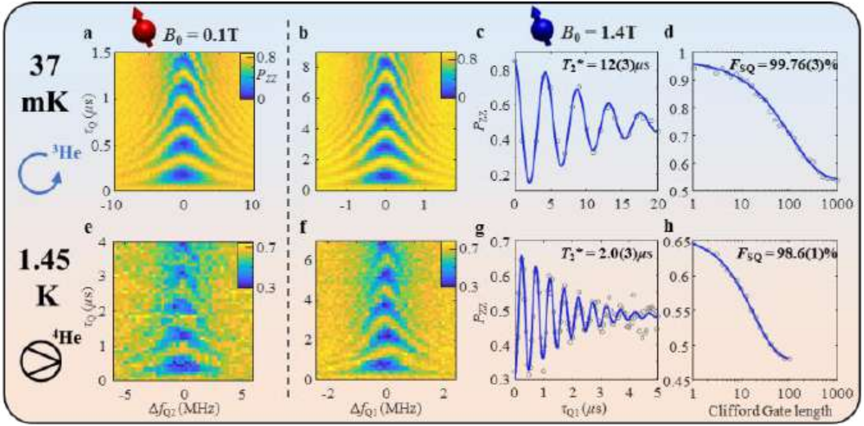


R. Li et al., arXiv 1711.03807 (2017)

SiMOS QD Qubit Operation at 1.5 Kelvin

Silicon quantum processor unit cell operation above one Kelvin

C. H. Yang,[1,*] R. C. C. Leon,[1] J. C. C. Hwang,[1,†] A. Saraiva,[1] T. Tanttu,[1]
W. Huang,[1] J. Camirand Lemyre,[2] K. W. Chan,[1,‡] K. Y. Tan,[1,‡] F. E. Hudson,[1]
K. M. Itoh,[3] A. Morello,[1] M. Pioro-Ladrière,[2,4] A. Laucht,[1] and A. S. Dzurak[1,§]



⇒ 1.5 K performance comparable to ^{nat}Si at 100 mK !

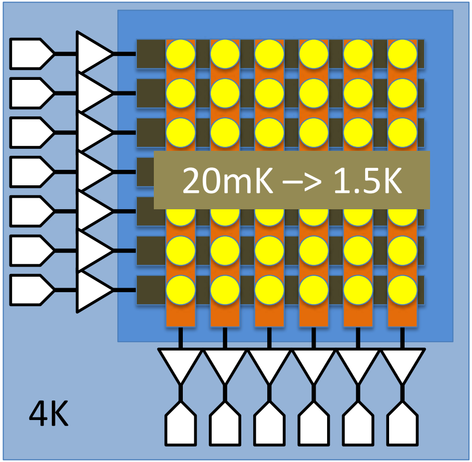
Courtesy: A. Dzurak

H. Yang *et al.*, arXiv:1902.09126

UNSW SYDNEY

Platforms for the 2D Approach

- **Single-shot dispersive readout** could be the core of column readouts
- Use ***imaging sensor*** readout as inspiration
- Use tunneling barriers as selectors
- (limited) use of 3D stacking
- Ideally bring qubits to 1-4K, make them CMOS-compatible



Tradeoffs

1-qubit gate:
Oscillator phase noise
Timing accuracy
…

Fidelity
(99.9%)

2-qubit gate:
Voltage drift
Timing jitter
…

Power
(~ 1 mW/qubit)

Qubit read-out:
Amplitude noise
…

- Fidelity is usually expressed as a percentage, ofter referred to as x9's (e.g. 5 9's = 99.999%)
- Higher fidelity usually requires high power, which is budgeted, espcially at low temperatures (e.g. μW of thermal absorption at mK, while W at 4K)

Quantum Computing

- A quantum computer is a new computing paradigm and as such it holds the promise to handle today’s intractable problems

- A qubit is fragile and thus needs to be constantly corrected to extend its coherence and to maintain fidelity

- Cryogenic electronics for quantum computing ensures compactness and scalability to much larger quantum processors

IceQubes: International Workshop on Cryogenic Electronics for Quantum Systems

June 2021, Neuchâtel - Switzerland